Hall Ticket No | | | | | | | | | | | Question Paper Code: ACS004

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations (Regular) - November, 2018

Regulation: IARE – R16

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **(Common to CSE | IT)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Briefly explain CPU internal organization with neat sketch. **[7M]**
   (b) Show the internal linear organization of an 8X2 ROM chip and explain it. **[7M]**

2. (a) Show the code to perform the computation $X = A + (B * C) + D$ using microprocessors that use the following instruction formats. Do not modify the values of A,B,C and D. If necessary use temporary location T to store intermediate results. **[7M]**
      i. Three- operand instructions
      ii. Two-operand instructions
      iii. One- operand instructions
      iv. Zero-operand instructions
   (b) Discuss about the addressing modes in assembly language in detail. **[7M]**

UNIT – II

3. (a) Explain in detail about RTL and specify a memory for the memory operation in each case. **[7M]**
      i. $R2 \leftarrow M[AR]$
      ii. $M[AR] \leftarrow R3$
      iii. $R5 \leftarrow M[R5]$
   (b) Describe Register transfer and list out the basic symbols for Register transfers. **[7M]**

4. (a) Define the micro instruction format with suitable example. **[7M]**
   (b) Demonstrate the micro programmed control organization. **[7M]**

UNIT – III

5. (a) Describe the instruction formats with neat sketch and Explain different fields of an instruction format. **[7M]**
   (b) Describe an instruction cycle and its various phases with a flow chart. **[7M]**

6. (a) Draw flowchart and explain addition and subtraction of floating point numbers in detail. **[7M]**

   (b) Illustrate BCD adder which contains two four bit binary adders with the block diagram. **[7M]**

UNIT – IV

7. (a) Explain Direct Memory Access Controller functionality with the block diagram. **[7M]**

   (b) A block of data is to be transferred between I/O device and processor, explain how this can be accomplished using DMA operation? **[7M]**

8. (a) Show how virtual address mapped with memory hierarchy with a neat sketch. **[7M]**

   (b) Explain modes of transfer for transferring information from CPU to other devices. **[7M]**

UNIT – V

9. (a) How speed up happens when instructions executed through pipelining? Prove it. **[7M]**

   (b) Explain pipeline processing in instruction stream with an example. **[7M]**

10. (a) Explain in detail about cross bar switching inter connection of multi processor system. **[7M]**

    (b) Discuss semaphore in interprocess communication in proper functionality of multiprocessor system. **[7M]**

– ○ ○ ◯ ○ ○ –