



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations (Supplementary) - July, 2018

Regulation: IARE – R16

Computer Architecture and Organization

Time: 3 Hours

(Common to CSE | IT)

Max Marks: 70

Answer ONE Question from each Unit

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

UNIT – I

1. (a) Explain the comparison between Dynamic RAM (DRAM) and Static RAM (SRAM), highlight the applications chosen for corresponding RAMs . [7M]
(b) Explain different categories of instructions of a relatively simple instruction set architecture. [7M]

2. (a) Define the instruction cycle and explain the various steps involved in execution of a instruction with flow chart. [7M]
(b) Explain different types of ROM chips which are differentiated by how often they are programmed. [7M]

UNIT – II

3. (a) Illustrate the construction of a bus system with three-state buffers. [7M]
(b) Explain different components of a micro program sequencer for control memory. [7M]

4. (a) Explain 4 - bit arithmetic circuit and draw the corresponding arithmetic circuit function table. [7M]
(b) Explain the general configuration of a microprogrammed control unit with the help of diagram. [7M]

UNIT – III

5. (a) Write the flowchart of decimal arithmetic unit with an example. [7M]
(b) Show the implementation of slt instruction , for the following ; 08M slt rd, rs, rt where rd = 1 if rs < rt, and rd = 0 otherwise inputs rs and rt can represent high-level language input variables A and B, the following implication: $A < B \Rightarrow A - B < 0$ [7M]

6. (a) Explain addition and subtraction algorithm with neat sketch. [7M]
(b) Explain about any three addressing modes with example. [7M]

UNIT – IV

7. (a) Briefly explain about RAM and ROM with block diagrams. [7M]
(b) Explain the cache coherence and how the performance of the processor is effected with respect to the cache hits and misses. [7M]

8. (a) Explain about direct associative and set associative memories with example. [7M]

(b) Explain the implementation of synchronized DRAM with a clock signal. [7M]

UNIT – V

9. (a) Draw the arithmetic pipeline diagram and explain different pipelining techniques. [7M]

(b) Write about multicomputers and multiprocessors. And also write about the characteristics of multiprocessors. [7M]

10. (a) Explain about inter process communication and synchronization in detail with neat sketch. [7M]

(b) Write about mutual exclusion mechanism to proper functioning of multiprocessor system. [7M]

