Hall Ticket No | | | | | | | | | | | Question Paper Code: ACS004

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Regular) - December, 2017

Regulation: IARE – R16

COMPUTER ORGANIZATION AND ARCHITECTURE

(Common for CSE | IT)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Explain about instruction cycle & draw the flowchart for instruction cycle. **[7M]**
   (b) Write an assembly language code for the expression X=(A+B)*(C+D) by using various instruction types. **[7M]**
2. (a) Briefly explain about Bus interconnection architecture. **[7M]**
   (b) Draw & explain about instruction format and explain what happened when (mode field) I = 0 or 1 in the instruction format. **[7M]**

UNIT – II

3. (a) List different logic operations that can be performed with two binary variables and show construction of one stage circuit that generates the four basic logic microoperations. **[8M]**
   (b) Explain the process of decoding the micro coding operations. **[6M]**
4. (a) Explain the general configuration of a microprogrammed control unit with the help of diagram. **[6M]**
   (b) Explain the block diagram of a control memory and the associated hardware needed for selecting the next microinstruction address. **[8M]**

UNIT – III

5. (a) Write about various addressing modes with example. **[6M]**
   (b) Show the implementation of BNE, for the following implication. **[8M]**
   A - B = 0 $\Rightarrow$ A = B .
6. (a) Write an algorithm for adding & subtracting numbers in signed-2's complement representation. **[7M]**
   (b) Illustrate specific types of overflow and underflow encountered in standard FP representation. **[7M]**

UNIT – IV

7. (a) Write about memory mapping techniques. **[7M]**

   (b) What is an Auxiliary Memory? Write about Magnetic Disks. **[7M]**

8. (a) Briefly explain about block diagram of DMA controller. **[7M]**

   (b) What is the advantage of two-wired hand shaking method and detailed about data transfer between source & destination. **[7M]**

UNIT – V

9. (a) Distinguish the internal organization of attached array processor and SIMD array processor. **[7M]**

   (b) Explain in detail about crossbar switch used in multiprocessor organization. **[7M]**

10. (a) Explain different steps needed to process each instruction and discuss the reasons for pipelining not performing at its maximum rate. **[8M]**

    (b) Calculate theoretical maximum speed up of a pipeline if cycle time is 20 ns, number of segments is 4 and number of tasks is 100. **[6M]**

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