INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

INFORMATION TECHNOLOGY

COURSE DESCRIPTOR

Course Title	ANALOG AND DIGITAL ELECTRONICS				
Course Code	AECB05				
Programme	B.Tech				
Semester	III	IT			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	0	3	3	1.5
Chief Coordinator	Ms M Saritha, Assistant professor.				
Course Faculty	Ms C Devisupraja, Assistant professor.				

I. COURSE OVERVIEW:

This course provides the basic knowledge over the construction and functionality of the basic electronic devices such as diodes and transistors. It also provides the information about the uncontrollable and controllable electronic switches and the flow of current through these switches in different biasing conditions and also will make them to learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AHSB13	II	Semiconductor Physics	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Data Structures	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz – Online Examination:

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT)

AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	1	Presentation on real-world problems
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Seminar
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Term Paper
PO 9	**Individual and Team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	3	Seminar/ Term Paper
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage independent and life-long learning in the broadest context of technological change.	2	Seminar

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand, analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based systems of varying complexity.	1	Seminar

PSO 2	**Problem-Solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	2	Open ended experiments
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES :

The course should enable the students to:	
I	Introduce components such as diodes, BJTs and FETs.
II	Know the applications of components.
III	Understand common forms of number representation in logic circuits
IV	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
V	Understand the concepts of combinational logic circuits and sequential circuits.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Acquire knowledge of electrical characteristics of ideal and practical diodes under forward and reverse bias to analyze and design diode application circuits such as rectifiers	CLO 1	Understand and analyze diodes operation and their characteristics in order to design basic form circuits
		CLO 2	Explain half wave rectifier for the given specifications.
		CLO 3	Design full wave rectifier for the given specifications
		CLO 4	Design rectifier with capacitive filter for the given specifications
CO 2	Utilize operational principles of bipolar to derive appropriate small-signal models and use them for the analysis of basic circuits.	CLO 5	Understand the different parameters of transistors such as depletion width and channel width for understanding the functioning and design of this component.
		CLO 6	Estimate the performance of BJT on the basis of their operation and working.
		CLO 7	Explain the operation of Operating Point and Load Line Analysis
		CLO 8	Explain the operation of CB,CE,CC I/O Characteristics
		CLO 9	Understand the importance of h-parameter model
CO 3	Understand the basic concept of number systems, Boolean algebra principles and	CLO 10	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.
		CLO 11	Explain the complements of Binary & Decimal number systems

	minimization techniques for Boolean algebra	CLO 12	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.
		CLO 13	Illustrate the switching algebra theorems and apply them for reduction of Boolean function.
		CLO 14	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
CO 4	Analyze Combination logic circuit such as multiplexers, adders, decoders	CLO 15	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
		CLO 16	Design Gate level minimization using KMaps and realize the Boolean function using logic gates.
		CLO 17	Analyze the design procedures of Combinational logic circuits like adders,Subtractors.
		CLO 18	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit.
CO 5	Understand about synchronous and asynchronous sequential logic circuits.	CLO 19	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops
		CLO 20	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
		CLO 21	Implement the synchronous& asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB05.01	CLO 1	Understand and analyze diodes operation and their characteristics in order to design basic form circuits	PO1	1
AECB05.02	CLO 2	Explain half wave rectifier for the given specifications.	PO3	2
AECB05.03	CLO 3	Design full wave rectifier for the given specifications	PO3	2
AECB05.04	CLO 4	Design rectifier with capacitive filter for the given specifications	PO3	2
AECB05.05	CLO 5	Understand the different parameters of transistors such as depletion width and channel width for understanding the functioning and design of this component.	PO3	2
AECB05.06	CLO 6	Estimate the performance of BJT on the basis of their operation and working.	PO3	2
AECB05.07	CLO 7	Explain the operation of Operating Point and Load Line Analysis	PO3	2
AECB05.08	CLO 8	Explain the operation of CB,CE,CC I/O Characteristics	PO4	3
AECB05.09	CLO 9	Understand the importance of h-parameter model	PO4	3
AECB05.10	CLO 10	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.	PO1	1
AECB05.11	CLO 11	Explain the complements of Binary & Weighted codes & Non-weighted codes.	PO1	1

AECB05.12	CLO 12	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.	PO3	2
AECB05.13	CLO 13	Illustrate the switching algebra theorems and apply them for reduction of Boolean function.	PO3	2
AECB05.14	CLO 14	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	PO1, PO3	2
AECB05.15	CLO 15	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	PO3	2
AECB05.16	CLO 16	Design Gate level minimization using K-Maps and realize the Boolean function using logic gates.	PO3	2
AECB05.17	CLO 17	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	PO1, PO3	2
AECB05.18	CLO 18	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit.	PO1, PO3	2
AECB05.19	CLO 19	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops	PO3	2
AECB05.20	CLO 20	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	PO4	2
AECB05.21	CLO 21	Implement the synchronous& asynchronous counters using design procedure of sequential circuit .	PO9	3

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course outcomes	PO1	PO3	PO4	PO9	PSO1	PSO2
CO 1	1	2			1	
CO 2		2	3			2
CO 3	1	2			1	
CO 4	1	2				2
CO 5		2	3	3		2

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XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CLOs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	1												1		
CLO 2			2												

CLO 3			2												
CLO 4			2										1		
CLO 5			2												
CLO 6			2											2	
CLO 7			2												
CLO 8				3										2	
CLO 9				3											
CLO 10	1												1		
CLO 11	1														
CLO 12			2												
CLO 13			2										1		
CLO 14	1		2												
CLO 15			2											2	
CLO 16			2												
CLO 17	1		2											2	
CLO18	1		2												
CLO19			2												
CLO20				3										2	
CLO21									3						

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO1, PO3, PO4,PO9, PSO1,PSO2	SEE Exams	PO1, PO3, PO4,PO9, PSO1,PSO2	Assignments	-	Seminars	PO9, PSO2.
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO1, PO2, PO4,PSO1						

XIV. ASSESSMENT METHODOLOGIES – INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

Module-I	**DIODE AND APPLICATIONS**
Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times. Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive Filter	
Module-II	**BIPOLAR JUNCTION TRANSISTOR (BJT)**
Principle of Operation and characteristics - Common Emitter, Common Base, Common Collector Configurations, Operating point, DC & AC load lines, Transistor Hybrid parameter model, Determination of h-parameters from transistor characteristics, Conversion of h-parameters.	
Module-III	**NUMBER SYSTEMS**
Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code. Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.	
Module-IV	**MINIMIZATION OF BOOLEAN FUNCTIONS**
Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method, Combinational Logic Circuits: Adders, Subtractors, comparators, Multiplexers, De-multiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations	
Module-V	**SEQUENTIAL CIRCUITS FUNDAMENTALS**
Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another. Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.	
Text Books:	
1. Electronic Devices and Circuits "Jacob Millman", McGraw Hill Education, 2017 2. Electronic Devices and Circuits theory "Robert L. Boylestead, Louis Nashelsky",11th Edition, Pearson, 2009. 3. Switching and Finite Automata Theory, "Zvi Kohavi & Niraj K. Jha, 3rd Edition", Cambridge, 2010. 4. Modern Digital Electronics, "R. P. Jain, 3rd Edition", Tata McGraw-Hill, 2007.	
Reference Books:	
1. Pulse, Digital and Switching Waveforms, "J. Millman, H. Taub and Mothiki S. Prakash Rao", 2 Ed., McGraw Hill, 2008. 2. Electronic Devices and Circuits, "S. Salivahanan, N.Suresh Kumar, A Vallvaraj, 2nd Edition", TMH. 3. Digital Design, "Morris Mano", PHI, 4th Edition,2006. 4. Introduction to Switching Theory and Logic Design, "Fredriac J. Hill, Gerald R. Peterson", 3rd Ed, John Wiley & Sons Inc.	

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Introduction to semiconductors, Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis.	CLO 1	T2:1.1-1.8, 2.2
6-7	Diffusion and Transition Capacitances, Diode Applications, Switch-Switching times	CLO 1	T2:1.10
8	Design Rectifier - Half Wave Rectifier & problems	CLO 2	T2:2.7
9-10	Design Full Wave Rectifier & problems	CLO 3	T2:2.8
11-12	Design Bridge Rectifier, Rectifiers with Capacitive Filter	CLO 4	T2:2.8
15-16	Understand the concepts of Transistor operation	CLO 6	T2:3.1-3.2
17-18	characteristics of CB,CE,CC	CLO 8	T2:3.3-3.7
19-21	Operating point, DC & AC load line Analysis & problems	CLO 7	T2:4.2,7.1-7.4
22-25	Transistor Hybrid parameter model, Determination of h-parameters from transistor characteristics, Conversion of h-parameters.	CLO 9	T2: 7.6 7.7, 8.9-8.10
26-27	Understand the need for digital systems, review of number systems, number base conversion	CLO 10	T3:1.1 R3:1.1-1.4
28-30	Complements of numbers, Weighted codes & Non-weighted codes.	CLO 11	T3:1.1-1.2 R3:1.5-1.7
31-32	error detecting and correcting codes, Digital Logic Gates	CLO 12	T3:1.3 R3:1.7,7.4
33-35	Basic Theorems and Properties, Algebraic Simplification,	CLO 13	T3:3.1-3.4 R3:2.1-2.4
36-37	Canonical and Standard Form	CLO 14	T3:3.3-3.5 R3:2.6
38-39	Universal Gates, Multilevel NAND/NOR realizations.	CLO 16	T3:5.1-5.3 R3:2.8,3.7-3.8
40-43	Identify basic building blocks of digital systems and Minimization using three variable; four variable; five variable K-Maps; Don‘t Care Conditions.	CLO 15	T4:5.1.-5.10 R3:3.6
44-45	Understand Tabular Method	CLO 15	T3:4.4-4.6 R3:3.10
46-47	Design Combinational Logic Circuits adders, subtractors.	CLO 17	T4:6.1,6.4 R3:4.1-4.5
48-49	Design different combinational logic circuits comparators Multiplexers, Demultiplexer.	CLO 14	T4:6.2-6.3,6.7 R3:4.8,4.11
50-51	Encoders ,Decoders	CLO 18	T4:6.3,6.10 R3:4.9-4.10
52-54	Code converters, Hazards & Hazard Free Relations	CLO 18	T4:6.9,5.12
55	Combinational and sequential circuits, the binary cell, the Fundamentals of sequential machine operation, SR-Latch	CLO 19	T4:7.1 R3:5.2-5.3
56-57	Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops.	CLO 19	T4:7.2-7.6 R3:5.4-5.5
58-60	Timing & Triggering, Excitation tables of Flip-flops, Conversion from one type of Flip-Flop to another	CLO 19	T4:7.7-7.10 R3:5.5
61	Shift Registers	CLO 20	T4:8.1-8.3
62	Synchronous, Asynchronous Counters	CLO 21	T4:8.4-8.7 R3:6.3-6.5

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S no	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Practical use of number systems	Seminars / NPTEL	PO 1, PO 4	PSO 1
2	Applications of flip-flops and latches	Seminars / NPTEL	PO 1, PO 4	PSO 1
3	Designing of circuits using flip-flops and latches.	Guest Lecture	PO 4, PO 9	PSO 2

Prepared by:
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