Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC006

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech IV Semester End Examinations (Regular) - May, 2018

Regulation: IARE – R16

PULSE AND DIGITAL CIRCUITS

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Derive an expression for the output voltages of high pass RC circuit excited by symmetrical square input. Draw the output for different time constants. **[7M]**

   (b) With the help of neat circuit diagram explain the operation of clipping at two different levels. **[7M]**

2. (a) Explain the operation of negative clamper with the neat circuit diagram and waveforms. **[7M]**

   (b) A square wave whose peak - to - peak amplitude is 2V extends ±1V with respect to ground. The duration of the positive section is 0.1sec and that of the negative section is 0.2sec. If this waveform is impressed upon an RC integrating circuit whose time constant is 0.2sec. What are the steady state maximum and minimum values of the output wave form? **[7M]**

UNIT – II

3. (a) What is monostable multivibrator? Explain the operation of collector coupled monostable multivibrator. **[7M]**

   (b) Design a bistable multivibrator to meet the following specifications, $V_{CC} = V_{BB}$= 12V, I_C(sat) = 6mA, h_{FE} (min)= 25, maximun triggering frequency = 25KHz. Assume V_{CE}(sat) = 0.4V, V_{BE}(sat)= 0.8V, I_B(ON) = 1.5I_B(min). **[7M]**

4. (a) Explain how the astable multivibrator circuit can act as a voltage to frequency converter. **[7M]**

   (b) Design a Schmitt trigger circuit using npn transistor for the following specifications V_{CC} = 15V, I_C(sat) =2mA, U_{TP} = 8V , L_{TP} = 5V, h_{FE}(min) = 25. Assume V_Γ = 0.5V. **[7M]**

UNIT – III

5. (a) Explain the effects of control voltage on gate output of a unidirectional diode gate with neat sketches. **[7M]**

   (b) What are the methods of generating time base waveforms. Derive an expression for sweep speed error of exponential sweep circuit. **[7M]**

6. (a) Discuss the working of transistor boot strap sweep circuit with neat circuit diagram relevant equations. **[7M]**

   (b) Design a UJT sweep circuit with RB_1= RB_2= 0Ω. The sweep amplitude is to be 10V. The sweep duration is 1ms and sweep speed error is to be 10%, the valley point voltage is 3V. Specify reasonable values for V_{BB}, V_{YY}, R and C. **[7M]**

UNIT – IV

7. (a) What do you mean by relaxation circuit. Explain the principle of operation of sweep generator using UJT with neat sketches. **[7M]**

   (b) With the help of circuit diagram and waveforms explain frequency division by an astable multivibrator. **[7M]**

8. (a) Describe the method involved in synchronization of a sweep circuit with symmetrical signals with neat sketches. **[7M]**

   (b) With the neat sketch, explain the sine wave frequency division with a sweep circuit. **[7M]**

UNIT – V

9. (a) Draw and explain the two input TTL NAND gate with totem pole output. What are the advantages and disadvantages of totem pole. **[7M]**

   (b) Explain the operation of ECL OR gate with a neat diagram. What are the drawbacks of ECL family. **[7M]**

10. (a) Describe the operation of DTL NAND gate. Clearly mention the purpose served by the diodes D1 and D2. What are the conditions to be fulfilled for the output to be in saturation. **[7M]**

    (b) Draw the circuit of CMOS NOR gate and explain its operation . Mention the advantages over other digital logic families. **[7M]**

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