Hall Ticket No | | | | | | | | | | |  Question Paper Code: AEC006

# INSTITUTE OF AERONAUTICAL ENGINEERING

**(Autonomous)**

B.Tech IV Semester End Examinations (Regular / Supplementary) - May, 2019

**Regulation: IARE – R16**

## PULSE AND DIGITAL CIRCUITS

**Time: 3 Hours** **(ECE)** **Max Marks: 70**

**Answer ONE Question from each Unit**
**All Questions Carry Equal Marks**
**All parts of the question must be answered in one place only**

### UNIT – I

1. (a) Deduce an expression for the percentage tilt of the output of a high-pass RC circuit with large time constant excited by a symmetrical square wave with zero average value. **[7M]**

   (b) For the circuit shown in Figure 1 an input voltage $V_i$ varies linearly from 0 to 150V. Sketch the output waveform $V_0$ to the same time scale. Assume ideal diodes. **[7M]**

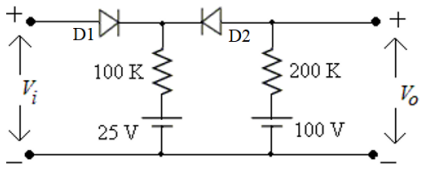


Figure 1

2. (a) Explain the operation of a biased negative clamper with neat sketch. **[7M]**

   (b) Design a clipping circuit with ideal components, which can give the following waveform shown in Figure 2 for a sinusoidal input. Assume necessary data. **[7M]**

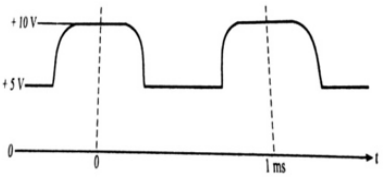


Figure 2

### UNIT – II

3. (a) Identify and apply appropriate multi-vibrating technique to convert sinusoidal signal to square signal, using two transistors. **[7M]**

   (b) Determine the frequency of oscillations and duty cycle for an astable multivibrator with $R_1 = 15$ kΩ , $R_2$=10 kΩ, $C_1$= 0.01 μF and $C_2$= 0.015 μF . **[7M]**

4. (a) What do you understand by hysteresis? What is hysteresis voltage? Explain how hysteresis can be eliminated in a Schmitt trigger. **[7M]**

   (b) The self-biased bistable multivibrator uses silicon transistors with $h_{FE(min)} = 20$. The junction voltages and $I_{CBO}$ may be neglected. Design the circuit subject to the condition $V_{CC} = 18$ V, $R_1 = R_2$, $I_{C(max)} = 10$ mA. The base current of ON transistor is twice the minimum base current, and $V_{BE}$ of the off transistor is equal to – 1 V. **[7M]**

## UNIT – III

5. (a) Define the terms slope error, displacement error and transmission error. How are they related for an exponential sweep circuit? Define the relation between them **[7M]**

   (b) Calculate sweep interval of a UJT sweep circuit for following specifications. $\eta = 0.68$, $V_{BB} = 12$V, $V_v = 0.8$V, $V_p = 6$V. **[7M]**

6. (a) Demonstrate the working of two-diode sampling gate with necessary diagrams and equations. **[7M]**

   (b) A transistor bootstrap ramp generator is to produce a 15 V, 5 ms output to a 2 k load resistor. The ramp is to be linear within 2%. Design a suitable circuit using $V_{CC} = 22$ V, $-V_{EE} = -22$ V and transistor with $h_{fe}$(min) = 25. The input pulse has an amplitude of – 5 V, pulse width = 5 ms and space width = 2.5 ms. **[7M]**

## UNIT – IV

7. (a) What is the need of synchronization and explain the method of synchronization of a sinusoidal oscillator with pulses. **[7M]**

   (b) Frequency division of 6:1 is obtained with an astable multivibrator, negative pulses are applied simultaneously to both bases of the n-p-n transistors. The OFF time of $Q_1(V_1)$ is twice that of $Q_2(V_2)$. Sketch the wave shapes at base terminals. **[7M]**

8. (a) What do you mean by relaxation circuit. Explain the principle of operation of sweep generator using UJT with neat sketches. Explain the concept of stability of relaxation devices. **[7M]**

   (b) Design a relaxation oscillator to have 3KHz output frequency using UJT and a 20V supply. Calculate the sweep amplitude. The specifications from the data sheet are given as $\eta$=0.7, $I_p$= 2$\mu A$, $I_v$=1$\mu A$, and $V_{BEsat}$=3V. **[7M]**

## UNIT – V

9. (a) Describe in detail the working of transistor inverter logic using circuit diagram. Discuss the function of two-input ECL OR/NOR gate with neat diagram. **[7M]**

   (b) Design a transistor inverter circuit (NOT gate) with the following specifications: $V_{CC} = V_{BB} =$ 10V, $I_{Csat} = 10$mA, $h_{fe}$(min) = 30. The input is varying between 0 and 10V. Assume typical junction voltages of npn silicon transistor **[7M]**

10. (a) Draw and explain the circuit of two-input TTL NAND with totem pole output. Implement NAND gate using CMOS logic **[7M]**

    (b) The two-input diode AND circuit shown uses diodes with $R_f$= 200Ω, $R_r$= 1M Ω and the currents in $D_1$ and $D_2$ are each 2 mA & 6 mA respectively. Then calculate the output voltage when one input diode is cut-off. **[7M]**

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