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# INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech IV Semester End Examinations (Regular) - May, 2018

Regulation: IARE – R16

## DIGITAL AND PULSE CIRCUITS

Time: 3 Hours

(EEE)

Max Marks: 70

Answer ONE Question from each Unit

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

### UNIT – I

1. (a) Generate a 7 bit even parity Hamming code for the given 4 bit message 1011 and rewrite the entire message with Hamming code. [7M]
- (b) Simplify the following Boolean expressions to minimum no. of literals. [7M]
  - i.  $xy' + y'z' + x'z'$
  - ii.  $xyz + yyz + y'z + xy'$
  - iii.  $(a + c)(a + c')(a + b + c'd)$
  - iv.  $x'z' + y + yz' + xyz$
2. (a) Convert the following [7M]
  - i.  $877_{10} = ()_{16}$
  - ii.  $408.93_{10} = ()_8$
  - iii.  $ABC_{16} = ()_{10}$
  - iv.  $292_{10} = ()_2$
- (b) Subtract the following using 2's complement method. [7M]
  - i.  $1011_2 - 1000_2$
  - ii.  $46_{10} - 12_{10}$

### UNIT – II

3. (a) Design a 4 bit BCD to Excess-3 Code Converter and realize using logic gates. [7M]
- (b) Implement the following function using logic gates  $F(x, y, z) = \sum m(0, 4, 5, 7)$ . [7M]
4. (a) What are the universal gates? Design a full adder using universal gates. [7M]
- (b) Using tabular method obtain the minimal expression for  $F(a, b, c, d) = \sum m(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ . [7M]

### UNIT – III

5. (a) Convert S-R flip-flop to J-K flip-flop and draw its logic circuit. [7M]  
(b) Draw the logic diagram of 4 bit ring counter using D flip flops and explain its operation with the help of bit pattern. [7M]
6. (a) Draw the logic diagram of a D flip flop and using excitation table, explain its operation. [7M]  
(b) Design a Mod-9 synchronous counter using T Flip-Flop with a neat sketch. [7M]

### UNIT – IV

7. (a) Draw the circuit diagram of voltage series feedback and derive expressions for input resistance and output resistance. [7M]  
(b) What are the types of feedback? Mention the characteristics of a Negative feedback amplifier. [7M]
8. (a) With neat diagram, explain the working of Hartley oscillator using BJT and derive an expression for frequency of oscillation. [7M]  
(b) What do you mean by oscillators and state the conditions for oscillations. [7M]

### UNIT – V

9. (a) Draw the simplified h-parameter model of CE configuration and derive the expression for  $A_I$ ,  $R_I$ ,  $A_v$  and  $R_0$ . [7M]  
(b) State and prove millers theorem and dual of millers theorem. [7M]
10. (a) Draw the circuit diagram of Darlington emitter follower and derive an expression for  $A_I$ ,  $R_I$ ,  $A_v$  and  $R_0$ . [7M]  
(b) Six identical stages are coupled, each amplifier having  $f_l = 100$  Hz and  $f_h = 100$  KHz. Determine the overall upper cut-off frequency, the overall lower cut off frequency for the six stages. What is cascading? derive the expression for  $A_I$ ,  $R_I$ . [7M]

