INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech IV Semester End Examinations (Supplementary) - July, 2018

Regulation: IARE – R16

DIGITAL AND PULSE CIRCUITS

Time: 3 Hours   (EEE)   Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) State and prove De Morgan's theorem for 3 variables. **[7M]**

   (b) Perform the following operations **[7M]**

   i) $(20.6875)_{10} = (\ ? \ )8$

   ii) $(DF8.28)_{16} = (\ ? \ )10$

   iii) $(2536)_{10} = (\ ? \ )16$

2. (a) Perform the following operation using 2's complement method. **[7M]**

   i) $(10.0101)_2$ - $(101.111)_2$

   ii) $(28)_{10}$- $(19)_{10}$

   (b) Solve the following boolean function and represent it in minterm and maxterm canonical form.
   $f(x, y, z) = (XY + X'Z)' + YZ.$ **[7M]**

UNIT – II

3. (a) Simplify the following function using Karnaugh map $Y = f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$ **[7M]**

   (b) Draw the logic daigram for 2:4 decoder with an active low enable and active high data outputs. Construct a truth table and identify the data inputs, enable input and the output. Describe the circuit function. **[7M]**

4. (a) Realize the following boolean function $f(w, x, y, z) = \sum m(0, 1, 4, 6, 7, 9, 11, 14, 15)$ using logic gates. **[7M]**

   (b) Perform the following to design a full subtractor **[7M]**

   i. Construct the truth table and simplify the output equations

   ii. Draw the resulting logic diagram.

UNIT – III

5. (a) What is the difference between a flip flop and a latch. Explain the operation of SR latch with a logic diagram and excitation table. **[7M]**

   (b) Design a synchronous Mod-6 counter uisng D flip flop and draw its logic diagram. **[7M]**

6. (a) Explain the operation of positive edge triggered JK flip flop with neat timing diagram. **[7M]**

    (b) Design a 3-bit binary ripple counter using T flip flop. **[7M]**

UNIT – IV

7. (a) Explain the effects of feedback on output impedance for current series and input impedance for current shunt feedback amplifier. **[7M]**

    (b) In a transistorized Hartely oscillator $L_1 = 0.5$mH , $L_2 = 0.5$µH while the frequency has been changed from 100kHz to 2000kHz. Determine the range of capacitor. Assume mutual inductance is negligible. **[7M]**

8. (a) Derive the expression for frequency of a RC phase shift oscillator and also explain its principle of operation. **[7M]**

    (b) A voltage series feedback amplifier has A = - 100, $R_i = 25$KΩ, $R_0 = 10$KΩ and feedback factor β= - 0.1 **[7M]**

    i. Determine overall gain, input impedance and output impedance of feedback amplifier.

    ii. If the gain has been reduced to -2.5, what will be the feedback factor.

UNIT – V

9. (a) Draw and explain the two stage transformer coupled common emitter amplifier circuit. **[7M]**

    (b) In common collector configuration a transistor has the following parameters: $h_{ic} = 1.5$Ω, $h_{rc} = 1$, $h_{fc} = $-55, $h_{oc} = 50$ x 10^{-6}, $R_s = 1.5$kΩ and $R_L = 2$KΩ. Determine the current gain, voltage gain, input impedance and output impedance. **[7M]**

10. (a) Explain the operation of emitter follower circuit using darlington connection. Derive the current gain expression of the same using small ac equivalent circuit. **[7M]**

    (b) Explain the effect of bypass capacitor at a low frequency response on a single stage CE amplifier. **[7M]**

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