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# INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Supplementary) February, 2018

**Regulation: IARE – R16**

**DIGITAL LOGIC DESIGN**

(Common to CSE / IT)

**Time: 3 Hours**

**Max Marks: 70**

Answer ONE Question from each Unit

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

### UNIT – I

1. (a) Demonstrate the usage of binary variables and the applications of binary logic with the help of simple switching circuits. [7M]
- (b) Given the two binary numbers  $x = 1010100$  and  $Y = 1000011$ , perform the subtraction. [7M]  
 a)  $X - Y$  and                      b)  $Y - X$  using 2's complements.
2. (a) Illustrate the procedure of converting from octal to hexadecimal numbers [7M]
- (b) Give the logic circuit representation of logical operations AND, OR and NOT and discuss the input-output signals for the corresponding gates. [7M]

### UNIT – II

3. (a) What is Product of Maxterms? Express the boolean function  $F = xy + x'z$  in a product of maxterm form. [7M]
- (b) Implement the following function with NAND gates. [7M]

$$F(x,y,z) = \sum m(0,6)$$

4. (a) Express the following Boolean functions in the following [7M]  
 i.  $F = XY + X'Z$  in standard sum of products  
 i.  $F = A + B'C$  in standard product of sums
- (b) List different steps in obtaining a multilevel NAND diagram from a boolean expression and demonstrate the same for the following boolean function.

$$F = A + (B' + C)(D' + BE')$$

### UNIT – III

5. (a) Write the logic diagram of a BCD-to-excess-3-code converter for the following expressions [7M]  
 $Z = D'$   
 $Y = CD + C'D' = CD + (C + D)'$   
 $X = B'C + B'D + BC'D' = B'(C + D) + BC'D'$   
 $W = A + BC + BD = A + B(C + D)$

- (b) Show the construction of a 2-to-4-line decoder with an enable input constructed with NAND gates. Construct the corresponding truth table for the same. [7M]
6. (a) Consider an example of multiplication of two numbers, say A and B (2 bits each),  $C = A \times B$ , design the logic diagram to compute the same [7M]
- (b) Enumerate the implementation of full-adder using two half-adders and an OR gate, for the following boolean expressions: [7M]
- $$S = x'y'z + x'yz' + xy'z' + xyz$$
- $$C = xy + xz + yz$$

#### UNIT – IV

7. (a) What is racing condition in JK flip flop? Explain how to eliminate it. [7M]
- (b) Design a BCD Ripple Counter using T Flip flops. [7M]
8. (a) Design the 3-bit binary synchronous counter and write the excitation table based on D-flipflops. [7M]
- (b) Write the toggle flip-flop characteristic table and characteristic equation when  $T=0, Q(t+1)=Q$  and  $T=1, Q(t+1)=Q'$ . [7M]

#### UNIT – V

9. (a) Calculate the utilization factor of tape, if the gap length is 0.5 in, the storage density  $S=3000$  bytes in and data storage capacity is 6 k bytes? [7M]
- (b) Design a Binary to Gray code converter and implement using suitable PLA. [7M]
10. (a) A computer uses RAM chips of 1024 x 1 capacity.
- i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
- ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [7M]
- (b) Distinguish between SRAM and DRAM [7M]

