Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB03

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

Four Year B.Tech III Semester End Examinations(Regular) - November, 2019
Regulation: IARE – R18
DIGITAL ELECTRONICS

Time: 3 Hours   **(EEE)**   Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Define the following terms
   i) Fan in
   ii) Power Dissipation
   iii) Propagation delay   **[7M]**
   (b) Construct 7 bit Hamming code using even parity for the message 0110.   **[7M]**

2. (a) Explain the operation of TTL NAND gate.   **[7M]**
   (b) Add $(600)_{10} + (612)_{10}$ using BCD Arithmetic.   **[7M]**

UNIT – II

3. (a) Design half adder and half subtracter circuit using NAND gates.   **[7M]**
   (b) Minimize the following function using K-map.
   F (A, B,C, D) = $\sum$ m(1,3,5,7,9,10,11,12,15)   **[7M]**

4. (a) Differentiate between BCD and Gray code converters. Design BCD to gray code converter.
                                                                                     [7M]
   (b) Implement the following function with 8x1 MUX
   F(A, B, C)=$\sum$m(0,2,6,7)   **[7M]**

UNIT – III

5. (a) With the help of circuit diagram and functional table, explain the working of D flip-flop. **[7M]**
   (b) Design a Mod-10 Asynchronous Counter using JK flip-Flop.   **[7M]**

6. (a) Compare the asynchronous and synchronous counters.   **[7M]**
   (b) Draw the logic circuit of clocked SR flip-flop using NAND gates and explain its operation. **[7M]**

UNIT – IV

7. (a) Discuss the various specifications of digital to analog Converter.   **[7M]**
   (b) Explain the operation of successive approximation ADC with necessary diagrams. **[7M]**

8. (a) Explain the working of Sample and Hold circuit? **[7M]**

   (b) With the help of circuit diagram and functional table, explain the working of Parallel Comparator A/D converter. **[7M]**

UNIT – V

9. (a) Demonstrate the organization of ROM and illustrate the features of a ROM cell? **[7M]**

   (b) Implement the combinational circuit with a PLA having 3 inputs,4 product terms and 2 outputs for the functions.

$F1 = \sum m(3,5,6,7); F2 = \sum m(0,2,4,7)$ **[7M]**

10. (a) Explain PLA with the help of block diagram. Mention the advantages of programmable logic devices.

[7M]

   (b) What is PROM? Implement full adder using PROM. **[7M]**