Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB07

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech III Semester End Examinations(Regular) - November, 2019

Regulation: IARE – R18

DIGITAL SYSTEM DESIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) State any four Boolean Laws and Demorgan's laws. **[7M]**
   (b) Indicate following numbers into base given
   i) $(152)_8=()_{10}$
   ii) $(34.26)_{10}=()_2$
   iii)Reproduce the given binary 110101 to Grey code **[7M]**

2. (a) Subtract the following decimal numbers using 8 bit 1's complement method.
   i) 52-17
   ii) 27-75 **[7M]**
   (b) Minimize the given function using K-Map method and implement in a Universal logic.
   F(A,B,C,D)= $\sum$m (0,1,2,3,5,7,8,9,10,12,13). **[7M]**

UNIT – II

3. (a) Integrate 4*16 decoder by using two 3*8 decoders. **[7M]**
   (b) Implement Full adder using two Half adders and one OR gate. **[7M]**

4. (a) Design 8 *3 Encoder with Logic gates. **[7M]**
   (b) Implement the function
   f(A,B,C,D)=$\sum$m(1,2,5,8,10,14,15) using 8:1Mux,4:1 Mux(Multiplexer) . **[7M]**

UNIT – III

5. (a) Design JK flipflop using NAND gates and explain its operation and obtain its characteristic equation. **[7M]**
   (b) Design MOD-6 Asynchronous upcounter. **[7M]**

6. (a) Convert SR flip flop to JK flip flop. **[7M]**
   (b) Develop ASM chart and state table for sequence detector that detects 1011. **[7M]**

UNIT – IV

7. (a) Define TTL and design NAND gate using TTL logic family. **[7M]**

   (b) Explain data flow style and behavioral style of modeling in VHDL for the expression $Y = \overline{A}B + AC$. Develop suitable VHDL code. **[7M]**

8. (a) Define CMOS logic. Draw the circuit diagram of a basic CMOS Inverter and explain its operation? **[7M]**

   (b) Realize the function f(x_2, x_1, x_0)= $\sum$ m(1,3,5,7) using PLA and PROM. **[7M]**

UNIT – V

9. (a) Explain the different types of datatypes in VHDL. **[7M]**

   (b) Explain the VHDL code for full adder using structural level and data flow modelling. **[7M]**

10. (a) What are the features of VHDL? Explain the VHDL objects. **[7M]**

    (b) Explain the VHDL code for full subtractor using structural level and dataflow modelling. **[7M]**