INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL SYSTEM DESIGN**				
Course Code	AECB07				
Programme	B.Tech				
Semester	III	ECE			
Course Type	Core				
Regulation	R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	3	1	4	-	-
Chief Coordinator	Dr. V Vijay, Associate Professor				
Course Faculty	Dr. P Munaswamy, Professor Dr. Lalit Kumar Kaul, Professor				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits. They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
-	-	-	-

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital System Design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

Alternative Assessment Tool (AAT)

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Lectures, Assignments and Exercises
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Seminars and Lab related exercises
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	1	Assignments

PO 4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Five minute videos

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Lectures and Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	1	Seminars
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur	2	Guest lectures

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Understand common forms of number representation in logic circuits.
II	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
III	Understand the concepts of combinational logic circuits and sequential circuits.
IV	Understand the Realization of Logic Gates Using Diodes & Transistors.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the logic simplification and combinational logic design.	CLO 1	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.
		CLO 2	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
		CLO 3	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
CO 2	Explore the MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU.	CLO 4	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder
		CLO 5	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.
		CLO 6	Analyze Barrel shifter and ALU
CO 3	Understand the building blocks like FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts.	CLO 7	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
		CLO 8	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
		CLO 9	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
		CLO 10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
		CLO 11	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CO 4	Understand the Logic Families And Semiconductor Memories	CLO 12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.
		CLO 13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,

COs	Course Outcome	CLOs	Course Learning Outcome
		CLO 14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.
CO 5	Explore the VHDL Design entry and Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	CLO 15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,
		CLO 16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,
		CLO 17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB07.01	CLO 1	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	PO 1 PO 2	2
AECB07.02	CLO 2	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	PO 1 PO 2	2
AECB07.03	CLO 3	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	PO 2	2
AECB07.04	CLO 4	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder	PO 2	2
AECB07.05	CLO 5	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.	PO 1 PO 2	2
AECB07.06	CLO 6	Analyze Barrel shifter and ALU	PO 2 PO 4	1
AECB07.07	CLO 7	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.	PO 4	1
AECB07.08	CLO 8	Analyze and apply the design procedures	PO 3	1

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
		of small sequential circuits to build the gated latches.		
AECB07.09	CLO 9	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	PO 3	1
AECB07.10	CLO 10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 2	2
AECB07.11	CLO 11	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 3	1
AECB07.12	CLO 12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.	PO 3	1
AECB07.13	CLO 13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,	PO 3	1
AECB07.14	CLO 14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.	PO 2	2
AECB07.15	CLO 15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,	PO 3	1
AECB07.16	CLO 16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,	PO 2	2
AECB07.17	CLO 17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	PO 2	2

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)						
	PO 1	PO 2	PO 3	PO 4	PSO 1	PSO 2	PSO 3
CO 1	3	2	3		1		
CO 2	3		3				1
CO 3	3	2				1	
CO 4		2	3				1
CO 5	3	2		2	1		

3 = High; 2 = Medium; 1 = Low

XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2												1	
CLO 2	3	2												1	
CLO 3		2												1	
CLO 4		2											3		
CLO 5	3	2												1	
CLO 6		2		1										1	
CLO 7				1										1	
CLO 8			1												
CLO 9			1												
CLO 10		2												1	
CLO 11			1											1	
CLO 12			1											1	
CLO 13			1										3		
CLO 14		2												1	
CLO 15			1												2

CLO 16		2												2
CLO 17		2											1	

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 2 PO3, PO 4	SEE Exams	PO 1, PO 2 PO 3, PO 4	Seminar and Term Paper	PO 1, PO 2 PO 3
Viva	-	Mini Project	-	Laboratory Practices	-

XIV. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS:

Module - I	**LOGIC SIMPLIFICATION AND COMBINATIONAL LOGIC DESIGN**
Review of Boolean Algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh maps up to 6 variables, Binary codes, Code Conversion.	
Module - II	**MSI DEVICES**
MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU	
Module - III	**SEQUENTIAL LOGIC DESIGN**
Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Ripple and Synchronous counters, Shift registers. Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation	
Module - IV	**LOGIC FAMILIES AND SEMICONDUCTOR MEMORIES**
TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS families and their interfacing, Memory elements, Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.	
Module - V	**VLSI DESIGN FLOW**
Design entry: Schematic, FSM & HDL, different modeling styles in VHDL, Data types and objects, Dataflow, Behavioral and Structural Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	

Text Books:
1. R.P. Jain, "Modern digital Electronics", Tata McGraw Hill, 4th Edition, 2009. 2. Douglas Perry, "VHDL", Tata McGraw Hill, 4th Edition, 2002. 3. W.H. Gothmann, "Digital Electronics- An introduction to theory and practice", PHI, 2nd Edition, 2006.
Reference Books:
1. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989 2. Charles Roth, "Digital System Design using VHDL", Tata McGraw Hill 2nd Edition 2012.
Web References:
1. mcsbzu.blogspot.com 2. http://books.askvenkat.com 3. http://worldclassprogramme.com 4. http://www.daenotes.com 5. http://nptel.ac.in/courses/117106086/1
E-Text Books:
1. https://books.google.co.in/books/about/Switching_Theory_and_Logic_Design 2. https://www.smartzworld.com/notes/switching-theory-and-logic-design-stld 3. https://www.researchgate.net/.../295616521_Switching_Theory_and_Logic_Design 4. https://books.askvenkat.com/switching-theory-and-logic-design-textbook-by-anand-kumar/ 5. http://www.springer.com/in/book/9780387285931

XVI. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topics to be covered	Reference
1-3	Number systems, base conversion methods.	T1:1.1 to 1.5 R1:3.1 to 3.5
4-6	Complements of numbers, codes- binary codes, BCD code and its properties.	T1:2.1 to 2.6 R2:2.8 to 3.5
7-9	Unit distance code, alphanumeric codes, and error detecting and correcting codes.	T1:4.1 to 4.9 R2:2.1 to 2.4
10-13	Basic theorems and its properties, switching functions, canonical and standard form.	T1:6.1 to 6.5 R2:7.1 to 7.7
14-16	Algebraic simplification of digital logic gates, properties of XOR gates.	T2:5.1 to 5.4 R2:4.1 to 4.8
17-20	Universal gates, Multilevel NAND/NOR realizations.	T1:2.8 R2:3.3 to 3.7
21-24	Combinational design, arithmetic circuits- adders, subtractors.	T3:3.7 to 3.8 R2: 2.7 to 2.9

Lecture No	Topics to be covered	Reference
25-28	Serial adder, 1's complement subtractor, 2's complement subtractor.	T1:4.1 to 4.9
29-32	Combinational and sequential circuits, the binary cell, the fundamentals of sequential machine operation.	T1:5.1 to 5.2 R1:3.1 to 3.5
32-36	Flip-flop, D-Latch Flip-flop, "Clocked T" Flip-flop, "Clocked JK "flip-flop.	T1:5.3 to 5.5 R2:5.1 to 5.8
37-40	Design of a clocked flip-flop conversion from one type of flip-flop to another.	T1:4.9 to 4.2 R1:8.1 to 8.5
41-42	Registers and counters	T1:1.1 to 1.5 R1:3.1 to 3.5
43-44	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.	T1:6.1 to 6.5 R2:7.1 to 7.7
45-46	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,	T2:5.1 to 5.4 R2:4.1 to 4.8
47-48	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.	T1:2.8 R2:3.3 to 3.7
49-50	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,	T1:6.1 to 6.5 R2:7.1 to 7.7
51-55	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,	T2:5.1 to 5.4 R1:4.1 to 4.8
56-60	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	T1:2.8 R2:3.3 to 3.7

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY/PROFESSION REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Gate level Minimization.	Seminars / NPTEL	PO 1, PO 2, PO 4
2	Design of combinational circuits using universal gates.	Seminars / Guest Lectures / NPTEL	PO 2, PO 3, PO 4
3	Verilog programming for combinational and sequential circuits.	Laboratory Practices	PO 1, PO 3, PO 4

Prepared By:
Dr. V Vijay, Associate Professor

HOD, ECE