INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

Course Title	**ANALOG AND PULSE CIRCUITS**				
Course Code	AECB11				
Programme	B.Tech				
Semester	IV	ECE			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Dr. V Vijay, Associate Professor				
Course Faculty	Mrs. KS Indrani, Assistant Professor, ECE Ms. N Anusha, Assistant Professor, ECE Mr. S Lakshmanachari, Assistant professor, ECE				

COURSE OUTCOMES (COs):

CO 1: Discuss the frequency response and analysis of multistage amplifiers and transistor at high frequency

CO 2: Analyze the effect of feedback on Amplifier characteristics in feedback amplifiers

CO 3: Discuss the frequency response of various oscillators and analyze the large signal and tuned amplifiers

CO 4: Understand the linear wave shaping and different types of sampling gates with operating principles using diodes, transistors

CO 5: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using Transistors

COURSE LEARNING OUTCOMES (CLOs):

Students who complete the course will have demonstrated the ability to do the following.

AECB07.01	Understand the classification of amplifiers, distortions in amplifiers and different coupling schemes used in amplifiers.
AECB07.02	Analyze various multistage amplifiers such as Darlington, Cascade etc.
AECB07.03	Understand and remember the concept of Hybrid - model of Common Emitter transistor.
AECB07.04	Analyze the importance of positive feedback and negative feedback in connection in electronic circuits.
AECB07.05	Analyze various types of feedback amplifiers like voltage series, voltage shunt, current series and current shunt.
AECB07.06	Understand the condition for Oscillations and various types of Oscillators.
AECB07.07	Design various sinusoidal Oscillators like RC Phase shift, Wien bridge, Hartley and Colpitts oscillator for various frequency ranges.

AECB07.08	Design different types of power amplifiers for practical applications of desired specifications like efficiency, output power, distortion, etc.
AECB07.09	Design the tuned circuits used in single tuned amplifiers and understand its frequency response.
AECB07.10	Analyze the response of high pass RC to different non sinusoidal inputs with different time constants and identify RC circuit's applications.
AECB07.11	Understand the basic operating principle of sampling gates.
AECB07.12	Analyze the response of low pass RC circuits to different non sinusoidal inputs with different time constants and identify RC circuit's applications.
AECB07.13	Illustrate the Bistable multivibrator with various triggering methods and apply design procedures to different bistable multivibrator circuits.
AECB07.14	Analyze the Monostable, Astable multivibrator circuits with applications and evaluate time, frequency parameters.
AECB07.15	Evaluate triggering points, hysteresis width of Schmitt trigger circuit and also design practical Schmitt trigger circuit.

SYLLABUS

MODULE-I	**MULTISTAGE AMPLIFIERS**	**Classes: 08**
Classification of Amplifiers, Distortion in amplifiers, Different coupling schemes used in amplifiers, Frequency response and Analysis of multistage amplifiers, Cascade amplifier, Darlington pair. Transistor at High Frequency: Hybrid - model of Common Emitter transistor model, f_α, β and MODULEy gain bandwidth, Gain band width product.		
MODULE-II	**FEEDBACK AMPLIFIERS**	**Classes: 10**
Concepts of feedback – Classification of feedback amplifiers – General characteristics of Negative feedback amplifiers – Effect of Feedback on Amplifier characteristics – Voltage series, Voltage shunt, Current series and Current shunt Feedback configurations.		
MODULE-III	**OSCILLATORS AND LARGE SIGNAL AMPLIFIERS**	**Classes: 08**
Condition for Oscillations, RC type Oscillators-RC phase shift and Wien-bridge Oscillators, LC type Oscillators –Generalized analysis of LC Oscillators, Hartley and Colpitts Oscillators, Frequency and amplitude stability of Oscillators, Crystal Oscillator. Class A Power Amplifier- Series fed and Transformer coupled, Conversion Efficiency, Class B Power Amplifier- Push Pull and Complimentary Symmetry configurations, Conversion Efficiency, Principle of operation of Class AB and Class C Amplifiers. Tuned Amplifiers: Single Tuned Amplifiers – Q-factor, frequency response of tuned amplifiers, Concept of stagger tuning and synchronous tuning.		
MODULE-IV	**LINEAR WAVE SHAPING AND SAMPLING GATES**	**Classes: 10**
Linear wave shaping circuits: High pass RC and low pass RC circuits, response to step and square inputs with different time constants, high pass RC circuit as a differentiator, low pass RC circuit as an integrator. Sampling gates: basic operating principle of sampling gate, uni and bi directional sampling gates.		
MODULE-V	**MULTIVIBRATORS**	**Classes: 09**
Multivibrators: Bistable multivibrator, unsymmetrical triggering, symmetrical triggering; Schmitt trigger; Monostable multivibrator, Astable multivibrator.		

Text Books:

1. Jacob Millman, Christos C Halkias, "Integrated Electronics" McGraw Hill Education, 2nd Edition, 2010.
2. B.N.Yoganarasimhan, "Pulse and Digital Circuits", 2nd Edition, 2011.
3. A. Anand Kumar, "Pulse and Digital Circuits", PHI learning, 2nd Edition, 2005.

Reference Books:

1. David A. Bell, “Electronic Devices and Circuits”, Oxford, 5th Edition, 1986.
2. Robert L. Boylestead, Louis Nashelsky, “Electronic Devices and Circuits Theory”, Pearson Education, 11th Edition, 2009.

Web References:

1. www.nptel.ac.in
2. notes.specworld.in/pdc-pulse-and-digital-circuits
3. http:// www.introni.it/pdf/Millman-Taub- Pulse and Digital Switching Waveforms 1965.pdf
4. https://www.jntubook.com/pulse-digital-circuits-textbook-free-download/

E-Text Books:

1. https://www.jntubook.com/electronic-circuit-analysis-textbook
2. http://tradownload.com/results/neamen-electronic-circuit-analysis-and-design-.htm
3. http://www.igniteengineers.com
4. http://www.ocw.nthu.edu.tw

MODULE I

MULTISTAGE AMPLIFIERS

Transistors at High Frequencies

At low frequencies it is assumed that transistor responds instantaneously to changes in the input voltage or current i.e., if you give AC signal between the base and emitter of a Transistor amplifier in Common Emitter configuraii6n and if the input signal frequency is low, the output at the collector will exactly follow the change in the input (amplitude etc.,). If '1' of the input is high (MHz) and the amplitude of the input signal is changing the Transistor amplifier will not be able to respond.

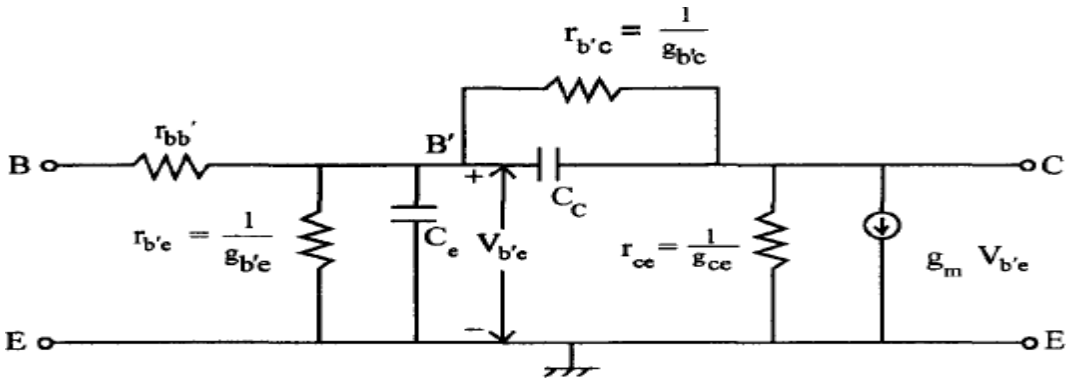
It is because; the carriers from the emitter side will have to be injected into the collector side. These take definite amount of time to travel from Emitter to Base, however small it may be. But if the input signal is varying at much higher speed than the actual time taken by the carries to

respond, then the Transistor amplifier will not respond instantaneously. Thus, the junction capacitances of the transistor, puts a limit to the highest frequency signal which the transistor can handle. Thus depending upon doping area of the junction etc, we have transistors which can respond in AF range and also RF range.

To study and analyze the behavior of the transistor to high frequency signals an equivalent model based upon transmission line equations will be accurate. But this model will be very complicated to analyze. So some approximations are made and the equivalent circuit is simplified. If the circuit is simplified to a great extent, it will be easy to analyze, but the results will not be accurate. If no approximations are made, the results will be accurate, but it will be difficult to analyze. The desirable features of an equivalent circuit for analysis are simplicity and accuracy. Such a circuit which is fairly simple and reasonably accurate is the Hybrid-pi or Hybrid-π model, so called because the circuit is in the form of π.

Hybrid - π Common Emitter Transconductance Model

For Transconductance amplifier circuits Common Emitter configuration is preferred. Why? Because for Common Collector (hrc< 1). For Common Collector Configuration, voltage gain Av < 1. So even by cascading you can't increase voltage gain. For Common Base, current gain is hib< 1. Overall voltage gain is less than 1. For Common Emitter, hre>>1. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used. The Hybrid-x or Giacoletto Model for the Common Emitter amplifier circuit (single stage) is as shown below.



Analysis of this circuit gives satisfactory results at all frequencies not only at high frequencies but also at low frequencies. All the parameters are assumed to be independent of frequency.

Where B’ = internal node in base

$r_{bb'}$ = Base spreading resistance

$r_{b'e}$ = Internal base node to emitter resistance r_{ce}

= collector to emitter resistance

C_e = Diffusion capacitance of emitter base junction

$r_{b'c}$ = Feedback resistance from internal base node to collector node g_m

= Transconductance

C_C= transition or space charge capacitance of base collector junction

Circuit Components

B' is the internal node of base of the Transconductance amplifier. It is not physically accessible. The base spreading resistance rbb is represented as a lumped parameter between base B and internal node B'. $g_m V_{b'e}$ is a current generator. Vb'e is the input voltage across the emitter junction. If Vb'e increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is proportional to Vb'e. This results in small signal current since we are taking into account changes in Vb'e. This effect is represented by the current generator $g_m V_{b'e}$. This represents the current that results because of the changes in Vb'e' when C is shorted to E.

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by gb'e. As recombination increases, base current increases. Minority carrier storage in the base is represented by C_e the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. Base width will be modulated according to the voltage variations between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. I_E changes and I_C changes. This feedback effect [IE on input side, I_C on output side] is taken into account by connecting gb'e between B', and C. The conductance between Collector and Base is gce.Cc represents the collector junction barrier capacitance.

Hybrid - n Parameter Values

Typical values of the hybrid-n parameter at I_C = 1.3 rnA are as follows:

g_m= 50 mA/v

rbb' = 100 Ω

rb'e = 1 kΩ

ree = 80 kΩ

Cc = 3 pf Ce

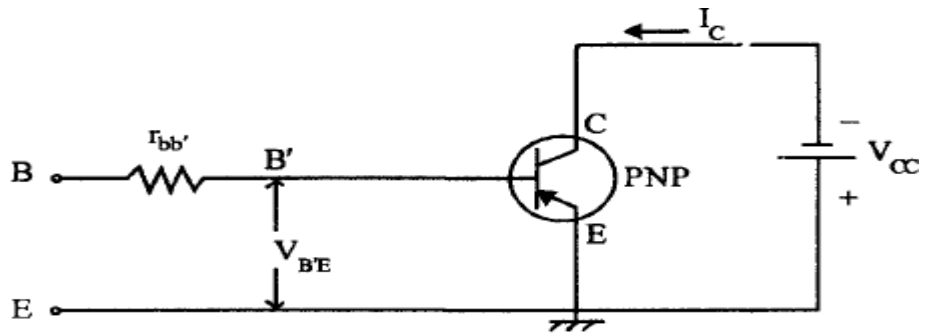
= 100 pf rb'c

= 4 MΩ

These values depend upon:1. Temperature 2. Value of I_C

Determination of Hybrid-x Conductances

1. Trans conductance or Mutual Conductance (gm)



The above figure shows PNP transistor amplifier in Common Emitter configuration for AC purpose, Collector is shorted to Emitter.

$$I_C = I_{C0} - \alpha_0 \cdot I_E$$

I_{CO} opposes I_E. I_E is negative. Hence $I_C = I_{CO} - \alpha 0 IE$ $\alpha 0$ is the normal value of α at room temperature.

In the hybrid - π equivalent circuit, the short circuit current = $g_m V_{b'e}$

Here only transistor is considered, and other circuit elements like resistors, capacitors etc are not considered.

$$g_m = \left.\frac{\partial I_C}{\partial V_{b'e}}\right|_{V_{CE} = K}$$

Differentiate (l) with respect to Vb'e partially. I_{CO} is constant

$$g_m = 0 - \alpha_0 \frac{\partial I_E}{\partial V_{b'e}}$$

For a PNP transistor, $V_{b'e} = -V_E$ Since, for PNP transistor, base is n-type. So negative voltage is given

$$g_m = \alpha_0 \frac{\partial I_E}{\partial V_E}$$

If the emitter diode resistance is r_e then

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$g_m = \frac{\alpha_0}{r_e}$$

$$r = \frac{\eta . V_T}{I} \quad \eta = 1, \qquad I = I_E \qquad r = \frac{V_T}{I_E}$$

$$g_m = \frac{\alpha_0 . I_E}{V_T} \qquad \alpha_0 \simeq 1, \qquad I_E \simeq I_C$$

$$I_E = I_{C0} - I_C$$

$$g_m = \frac{I_{C0} - I_C}{V_T}$$

Neglect I_{C0}

$$g_m = \frac{|I_C|}{V_T}$$

g_m is directly proportional to I_C is also inversely proportional to T. For PNP transistor, I_C is negative

$$\boxed{g_m = \frac{-I_C}{V_T}}$$

At room temperature i.e. $T=300^0K$

$$g_m = \frac{|I_C|}{26}, \; I_C \text{ is in mA.}$$

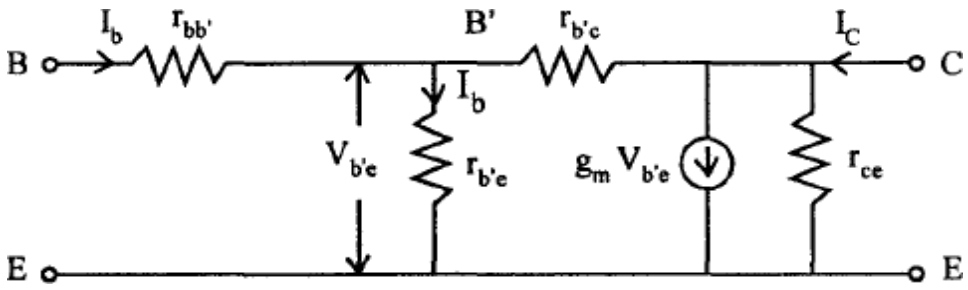
If $I_C = 1.3$ mA, $g_m = 0.05$ A/V

If $I_C = 10$ mA, $g_m = 400$ mA/V

Input Conductance (gb'e):

At low frequencies, capacitive reactance will be very large and can be considered as Open circuit. So in the hybrid-π equivalent circuit which is valid at low frequencies, all the capacitances can be neglected.

The equivalent circuit is as shown in Fig.



The value of rb'c» rb'e (Since Collector Base junction is Reverse Biased)So I_b flows into rb'e only. [This is lb' (IE - I_b)will go to collector junction]

$$V_{b'e} \simeq I_b \cdot r_{b'e}$$

The short circuit collector current,

$$I_C = g_m . V_{b'e}; \qquad V_{b'e} = I_b . r_{b'e}$$

$$I_C = g_m . I_b . r_{b'e}$$

$$h_{fe} = \left.\frac{I_C}{I_B}\right|_{V_{CE}} = g_m . r_{b'e}$$

$$\boxed{r_{b'e} = \frac{h_{fe}}{g_m}}$$

$$g_m = \frac{|I_C|}{V_T}$$

$$r_{b'e} = \frac{h_{fe} . V_T}{|I_C|}$$

$$g_{b'e} = \boxed{\frac{|I_C|}{h_{fe} V_T}} \text{ or } \boxed{\frac{g_m}{h_{fe}}}$$

Feedback Conductance (gb' c)

hre = reverse voltage gain, with input open or $I_b = 0$ hre

=Vb'e/Vce = Input voltage/Output voltage

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

[With input open, i.e., $I_b = 0$, V_{ce} is output. So it will get divided between $r_{b'e}$ and $r_{b'c}$ only]

or $$h_{re}\,(r_{b'e} + r_{b'c}) = r_{b'e}$$

$$r_{b'e}\,[1 - h_{re}] = h_{re}\, r_{b'c}$$

But $$h_{re} \ll 1$$

$\therefore$ $$r_{b'e} = h_{re}\ \ r_{b'c}\,; \quad r_{b'c} = \frac{r_{b'e}}{h_{re}}$$

or $$\boxed{g_{b'c} = h_{re}\ \ g_{b'e}} \quad \frac{1}{r_{b'c}} = g_{b'c} \quad = \frac{h_{re}}{r_{b'e}}$$

$$h_{re} = 10^{-4}$$

$\therefore$ $$r_{b'c} \gg r_{b'e}$$

Base Spreading Resistance (r bb')

The input resistance with the output shorted is hie. If output is shorted, i.e., Collector and Emitter arejoined; $r_{b'e}$ is in parallel with $r_{b'c}$.

$$h_{ie} = r_{bb'} + r_{b'e} \qquad r_{b'e} = \frac{h_{fe}.V_T}{|I_C|}$$

$$\boxed{r_{bb'} = h_{ie} - r_{b'e}}$$

$$h_{ie} = r_{bb'} + r_{b'e} \qquad h_{ie} = r_{bb'} + \frac{h_{fe}.V_T}{|I_C|}$$

Output Conductance (gce)

This is the conductance with input open circuited. In h-parameters it is represented as hoe. For $I_b = 0$, we have,

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m \; V_{b'e}$$

$$h_{re} = \frac{V_{b'e}}{V_{ce}} \qquad \therefore \qquad V_{b'e} = h_{re}.\, V_{ce}$$

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m.\, h_{re}.V_{ce}$$

$$h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \cdot h_{re}$$

$$= g_{ce} + g_{b'c} + g_m\, h_{re}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$g_m = g_{b'e} \cdot h_{fe}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \approx \frac{r_{b'e}}{r_{b'c}} = \frac{g_{b'c}}{g_{b'e}}$$

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'e}\, h_{fe} \cdot \frac{g_{b'c}}{g_{b'e}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) \cdot g_{b'c}$$

$$h_{fe} >> 1,\ \ 1 + h_{fe} \approx h_{fe}$$

$$\boxed{\mathbf{g_{ce} = h_{oe} - h_{fe} \cdot g_{b'c}}}$$

$$g_{b'c} = h_{re} \cdot g_{b'e}$$

$$g_{ce} = h_{oe} - h_{fe} \cdot h_{re} \cdot g_{b'e}$$

Hybrid - π Capacitances

In the hybrid - π equivalent circuit, there are two capacitances, the capacitance between the Collector Base junction is the C_C or $C_{b'e'}$. This is measured with input open i.e., $I_E = 0$, and is specified by the manufacturers as C_{Ob}. 0 indicates that input is open. Collector junction is reverse biased.

$$C_C \alpha \frac{1}{(V_{CE})^n}$$

$$n = \frac{1}{2} \quad \text{for abrupt junction}$$

$$= 1/3 \quad \text{for graded junction.}$$

C_e = Emitter diffusion capacitance C_{De} + Emitter junction capacitance C_{Te}

C_T = Transition capacitance.

C_D = Diffusion capacitance.

$C_{De} >> C_{Te}$

$C_e \simeq C_{De}$

$C_{De} \alpha I_E$ and is independent of Temperature T.

Validity of hybrid-π model

The high frequency hybrid Pi or Giacoletto model of BJT is valid for frequencies less than the MODULE gain frequency.

High frequency model parameters of a BJT in terms of low frequency hybrid parameters

The main advantage of high frequency model is that this model can be simplified to obtain low frequency model of BJT. This is done by eliminating capacitance's from the high frequency model so that the BJT responds without any significant delay (instantaneously) to the input signal. In practice there will be some delay between the input signal and output signal of BJT which will be very small compared to signal period (1/frequency of input signal) and hence can be neglected. The high frequency model of BJT is simplified at low frequencies and redrawn as shown in the figure below along with the small signal low frequency hybrid model of BJT.

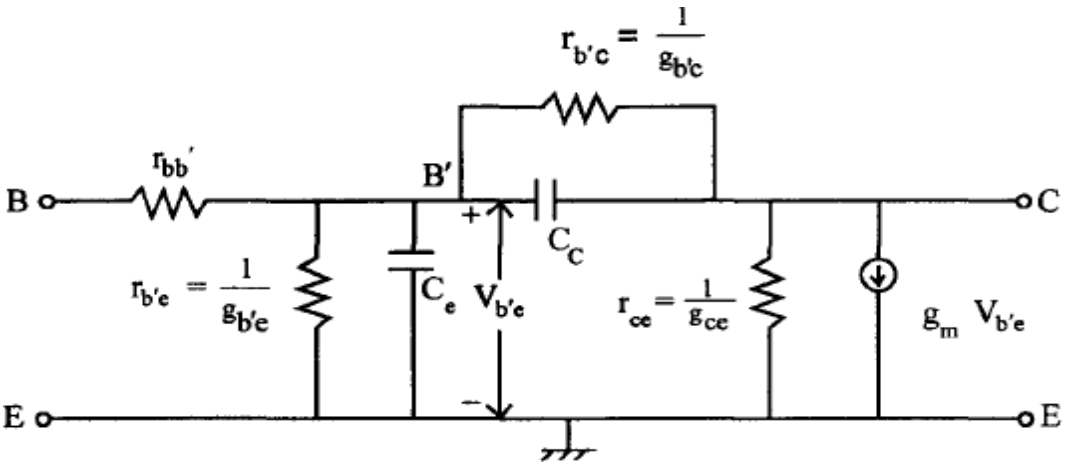


Fig. high frequency model of BJT at low frequencies

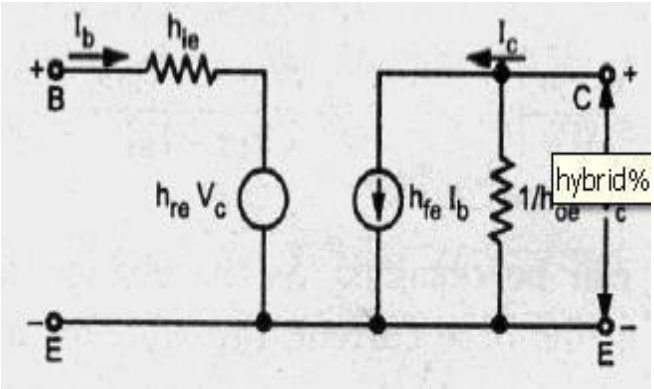


Fig hybrid model of BJT at low frequencies

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters are given below:

Transconductance $g_m = I_c/V_t$

Internal Base node to emitter resistance $r_{b'e} = h_{fe}/ g_m = (h_{fe}* V_t)/ I_c$

Internal Base node to collector resistance $r_{b'e} = (h_{re}* r_{b'c}) / (1- h_{re})$ assuming $h_{re} << 1$ it reduces to $r_{b'e} = (h_{re}* r_{b'c})$

Base spreading resistance $r_{bb'} = h_{ie} – r_{b'e} = h_{ie} – (h_{fe}* V_t)/ I_c$

Collector to emitter resistance $r_{ce} = 1 / (h_{oe} – (1+ h_{fe})/r_{b'c})$

Collector Emitter Short Circuit Current Gain

Consider a single stage Common Emitter transistor amplifier circuit. The hybrid-1t equivalent circuit is as shown:

$$I_L = - g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

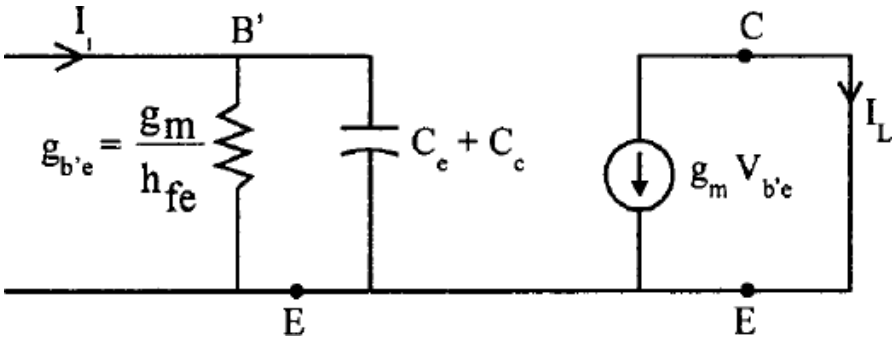
But $$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\,2\pi . g_m . f}{2\pi f_T}}$$

$\therefore$ $$A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

If the output is shorted i.e. $R_L = 0$, what will be the flow response of this circuit? When $R_L = 0$, $V_o = 0$. Hence $A_V = 0$. So the gain that we consider here is the current gain I_L/I_c. The simplified equivalent circuit with output shorted is,



A current source gives sinusoidal current I_c. Output current or load current is $I_L \cdot g_{b'c}$ is neglected since $g_{b'c} \ll g_{b'e}$, g_{ce} is in shunt with short circuit $R = 0$. Therefore g_{ce} disappears. The current is delivered to the output directly through C_e and $g_{b'c}$ is also neglected since this will be very small.

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But $$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\,2\pi . g_m . f}{2\pi f_T}}$$

$\therefore$ $$A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

$$= \frac{-h_{fe}}{1 + j\, h_{fe}\left(\frac{f}{f_T}\right)}$$

$$A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}$$

$$\frac{f_T}{h_{fe}} = f_\beta$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

Where $$f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_C)}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$\therefore$ $$f_\beta = \frac{g_m}{h_{fe}\, 2\pi(Ce + C_c)}$$

At $f = f_\beta$, $A_i = \frac{1}{\sqrt{2}} = 0.707$ of h_{fe}.

Current Gain with Resistance Load:

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

Considering the load resistance R_L

$V_{b'e}$ is the input voltage and is equal to V_1

V_{ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{ce}}{V_{b'e}}$$

This circuit is still complicated for analysis. Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

K = Voltage gain. It will be >> 1

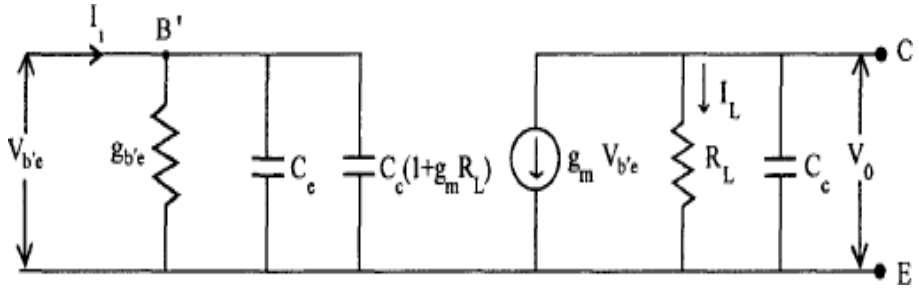
$$g_{b'c}\left(\frac{K-1}{K}\right) \simeq g_{b'c}$$

$g_{b'c} < g_{ce}$ $\because$ $r_{b'c} \simeq 4\ M\Omega$, $r_{ce} = 80\ K$ (typical values)

So $g_{b'c}$ can be neglected in the equivalent circuit. In a wide band amplifier RL will not exceed 2KΩ. If R_L is small f_H is large.

$$f_H = \frac{1}{2\pi C_s (R_C \| R_L)}$$

Therefore g_{ce} can be neglected compared with R_L. Therefore the output circuit consists of current generator gm $V_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig.



$$K = \frac{V_{ce}}{V_{b'e}} = -g_m R_L ; \qquad g_m = 50 \text{ mA\V}, \qquad R_L = 2K\Omega \text{ (typical values)}$$

$$K = -100$$

Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K, the same effect can be had by removing Z and connecting an impedance Z_i at the input =Z/(1-K) and Zo across the output = ZK/(K-1)

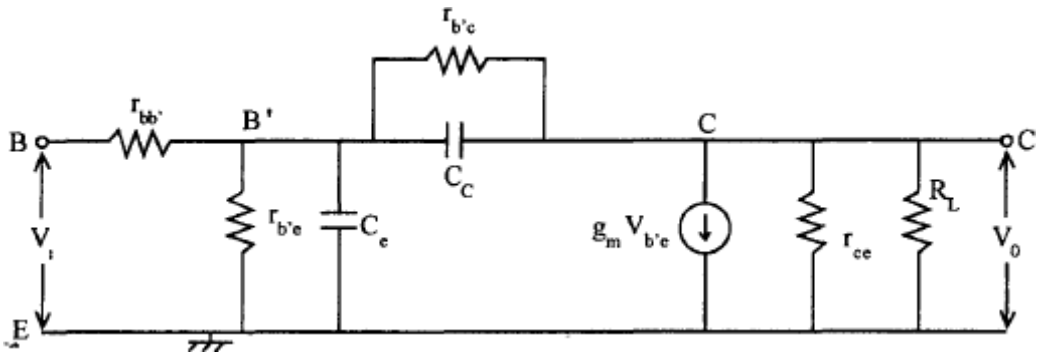


Fig. High frequency equivalent circuit with resistive load R_L

Therefore high frequency equivalent circuit using Miller's theorem reduces to

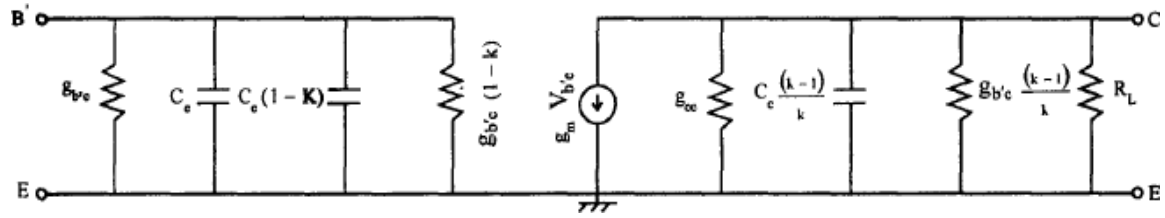


Fig. Circuit after applying Millers' Theorem

$$K = \frac{V_{ce}}{V_{b'e}}$$

$$V_{ce} = - I_C \ . R_L$$

$$K = \frac{-I_C . R_L}{V_{b'e}}$$

$$\frac{I_C}{V_{b'e}} = g_m$$

$$K = -g_m . R_L$$

The Parameters f_T

f$_T$ is the frequency at which the short circuit Common Emitter current gain becomes MODULEy.

The Parameters f_β

$$A_i = 1, \quad \text{or} \quad \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}} = 1$$

$$f = f_T, \quad A_i = 1$$

$$h_{fe} = \sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}$$

$$(h_{fe})^2 = 1 + \left(\frac{f_T}{f_\beta}\right)^2 \cong \left(\frac{f_T}{f_\beta}\right)^2$$

$$h_{fe} \simeq \frac{f_T}{f_\beta} \quad \text{when Ai} = 1$$

$$\boxed{f_T \simeq h_{fe} \cdot f_\beta}$$

$$f_\beta = \frac{g_m}{h_{fe}\{C_e + C_c\}}$$

$$f_T = f_\beta . h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

$$C_e >> C_c$$

$$\boxed{f_T \simeq \frac{g_m}{2\pi C_e}}$$

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

Dividing by $g_{b'e}$, Numerator and Denominator,

$$A_i = \frac{-g_m / g_{b'e}}{1 + \frac{j2\pi f(C_e + C_c)}{g_{b'e}}}$$

we know that $g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore$ $\frac{g_m}{g_{b'e}} = h_{fe}$

$$A_i = \frac{-h_{fe}}{1 + jf\left[\frac{2\pi(C_e + C_C)}{g_{b'e}}\right]}$$

But we know that $A_i = \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}}$

Comparing, $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)}$ $\because$ $g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore$ $\boxed{f_\beta = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)}}$

$\boxed{f_T = \frac{g_m}{2\pi(C_e + C_c)}}$

Gain - Bandwidth (B.W) Product

This is a measure to denote the performance of an amplifier circuit. Gain - B. W product is also referred as Figure of Merit of an amplifier. Any amplifier circuit must have large gain and large bandwidth. For certain amplifier circuits, the mid band gain Am maybe large, but not Band width or Vice - Versa. Different amplifier circuits can be compared with thus parameter

1.1 MULTISTAGE AMPLIFIERS

Multistage Amplifiers : Classification of amplifiers, methods of coupling**, c**ascaded transistor amplifier and its analysis, analysis of two stage RC coupled amplifier, high input resistance transistor amplifier

circuits and their analysis-Darlington pair amplifier, Cascode amplifier, Boot-strap emitter follower, Analysis of multi stage amplifiers using FET, Differential amplifier using BJT.

Classification of amplifiers

Depending upon the type of coupling, the multistage amplifiers are classified as :

1. Resistance and Capacitance Coupled Amplifiers (RC Coupled)
2. Transformer Coupled Amplifiers
3. Direct Coupled DC Amplifiers
4. Tuned Circuit Amplifiers.

Based upon the B. W. of the amplifiers, they can be classified as :

1. Narrow hand amplifiers
2. Untuned amplifiers

Narrow hand amplifiers: Amplification is restricted to a narrow band of frequencies around a centre frequency. There are essentially tuned amplifiers.

Untuned amplifiers: These will have large bandwidth. Amplification is desired over a considerable range of frequency spectrum.

Untuned amplifiers are further classified w.r.t bandwidth.

I. DC amplifiers (Direct Coupled) DC to few KHz
2. Audio frequency amplifiers (AF) 20 Hz to 20 KHz
3. Broad band amplifier DC to few MHz
4. Video amplifier 100 Hz to few MHz

The gain provided by an amplifier circuit is not the same for all frequencies because the reactance of the elements connected in the circuit and the device reactance value depend upon

the frequency. Bandwidth of an amplifier is the frequency range over which the amplifier stage gain is reasonably constant within ± 3 db, or O. 707 of AV Max Value.

Resistance and Capacitance Coupled Amplifiers (RC Coupled)

This type of amplifier is very widely used. It is least expensive and has good frequency response. In the multistage resistive capacitor coupled amplifiers, the output of the first stage is coupled to the next through coupling capacitor and R_L. In two stages Resistor Capacitor coupled amplifiers, there is no separate R_L between collector and ground, but Reo the resistance between collector and V cc (R_C) itself acts as R_L in the AC equivalent circuit.

Transformer Coupled Amplifiers

`Here the output of the amplifier is coupled to the next stage or to the load through a transformer. With this

overall circuit gain will be increased and also impedance matching can be achieved. But such transformer

coupled amplifiers will not have broad frequency response i.e., (f_2-f_1) is small since inductance of the

transformer windings will be large. So Transformer coupling is done for power amplifier circuits, where impedance matching is critical criterion for maximum power to be delivered to the load.

Direct Coupled (DC) Amplifiers

Here DC stands for direct coupled and not (direct current). In this type, there is no reactive element. L or C used to couple the output of one stage to the other. The AC output from the collector of one stage is directly given to the base of the second stage transistor directly. So type of amplifiers is used for large amplification of DC and using low frequency signals. Resistor Capacitor coupled amplifiers cannot be used for amplifications of DC or low frequency signals since Xc the capacitive reactance of the coupling capacitor will be very large or open circuit for DC

Tuned Circuit Amplifiers

In this type there will be one RC or LC tuned circuit between collector and V_{CC} in the place of Re. These amplifiers will amplify signals of only fixed frequency.fo which is equal to the resonance frequency of the tuned circuit LC. These are also used to amplify signals of a narrow band of frequencies centered on the tuned frequency f_0.

Distortion in Amplifiers

If the input signal is a sine wave the output should also be a true sine wave. But in all the cases it may not be so, which we characterize as distortion. Distortion can be due to the nonlinear characteristic of the device, due to operating point not being chosen properly, due to large signal swing of the input from the operating point or due to the reactive elements Land C in the circuit. Distortion is classified as:

(a) *Amplitude distortion:*

This is also called non linear distortion or harmonic distortion. This type of distortion occurs in large signal amplifiers or power amplifiers. It is due to then on linearity of the characteristic of the device. This is due to the presence of new frequency signals which are not present in the input. If the input signal is of 10 KHz the output signal should also be 10 KHz signal. But some harmonic terms will also be present. Hence the amplitude of the signal (rms value) will be different Vo = Ay Vi.

(b) *Frequency distortion:*

The amplification will not be the same for all frequencies. This is due to reactive component in the circuit.

(c) *Phase - shift delay distortion:*

There will be phase shift between the input and the output and this phase shift will not be the same for all frequency signals. It also varies with the frequency of the input signal. In the output signal, all these distortions may be present or anyone may be present because of which the amplifier response will not be good.

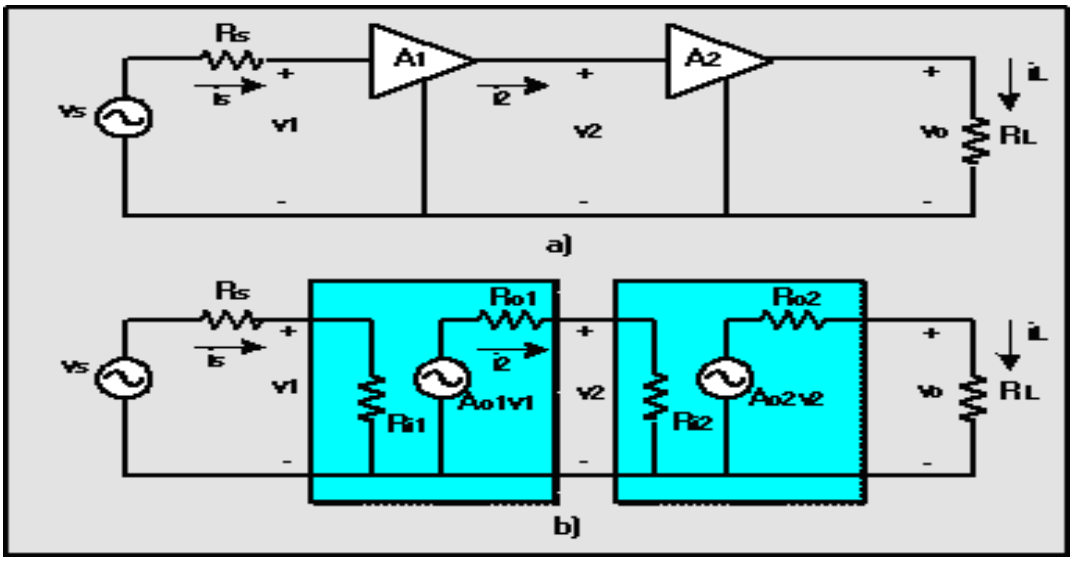
The performance obtainable from a single stage amplifier is often insufficient for many applications; hence several stages may be combined forming a multistage amplifier. These stages may be combined forming a multistage amplifier. These stages are connected in cascade, i.e. output of the first stage is connected to form input of second stage, whose output becomes input of third stage, and so on. The overall gain of a multistage amplifier is the product of the gains of the individual stage (ignoring potential loading effects):

Gain (A) = A1 * A2 * A3 * A4 * …… *An.

Alternately, if the gain of each amplifier stage is expressed in decibels (dB), the total gain is the sum of the gains of the individual stages

Gain in dB (A) = A1 + A2 + A3 + A4 + …… + An.

When we want to achieve higher amplification than a single stage amplifier can offer, it is a common practice to cascade various stages of amplifiers, as it is shown in Fig.1.a. In such a structure the input performance of the resulted multistage amplifier is the input performance of the first amplifier while the output performance is that of the last amplifier. It is understood that combining amplifiers of various types we can create those characteristics that are necessary to fulfill the specifications of a specific application. In addition, using feedback techniques in properly chosen multistage amplifiers can further increase this freedom of the design.



According to the small signal equivalent circuit of a two stage amplifier shown in Fig., we can calculate the ac performance of the circuit.

Voltage amplification

$$A_v = \frac{V_o}{V_1} = \frac{V_o}{V_2} \cdot \frac{V_o}{V_1} = A_{v2} \cdot A_{v1}$$

Current amplification

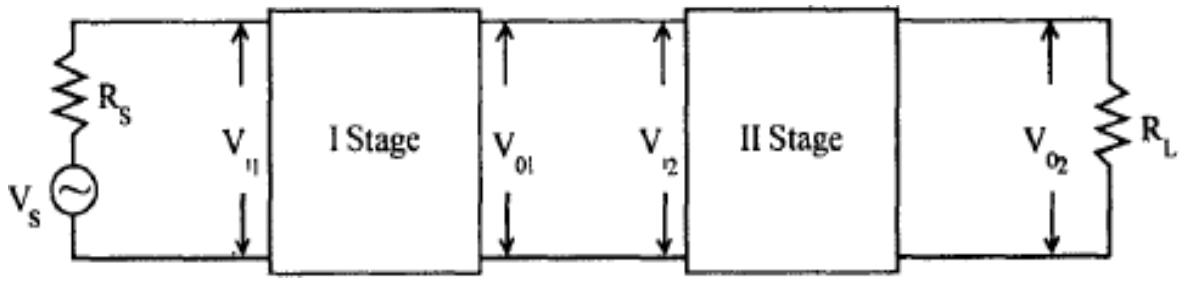
$$A_i = \frac{i_L}{i_s} = \frac{i_L}{i_2} \cdot \frac{i_2}{i_s} = A_{i2} \cdot A_{il}$$

Power amplification

$$A_p = A_v \cdot A_i = (A_{v2} \cdot A_{12}) \cdot (A_{vl} \cdot A_{il}) = A_{p2} \cdot A_{pl}$$

Cascading Transistor Amplifiers

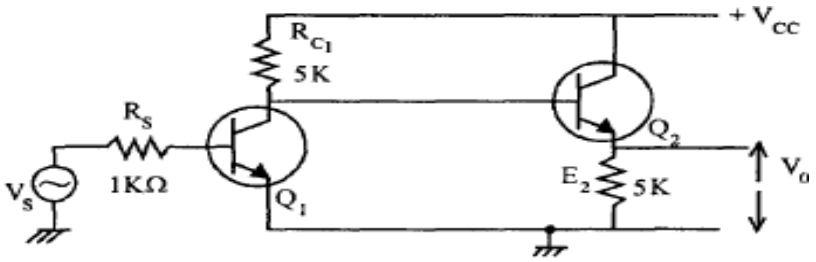
When the amplification of a single transistor is not sufficient for a particular purpose (say to deliver output to the speaker or to drive a transducer etc) or when the input or output impedance is not of the correct magnitude for the desired application, two or more stages may be connected in cascade. Cascade means in series i.e. the output of first stage is connected to the input of the next stage.



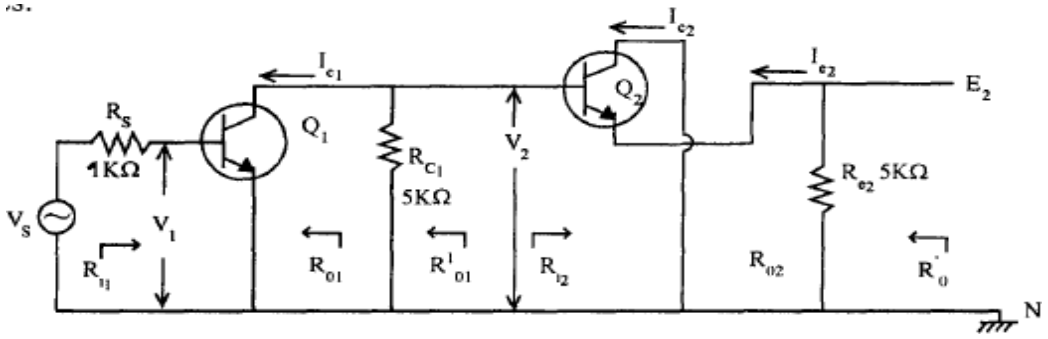
Let us consider two stage cascaded amplifier. Let the first stage is in common emitter configuration. Current gain is high and let the II stage is in common collector configuration to provide high input impedance and low output impedance. So what are the expressions for the total current gain A_I of the entire circuit (i.e. the two stages), Z_i, A_V and Y_O? To get these expressions, we must take the h-par ammeters of these transistors in that particular configuration. Generally manufactures specify the h-parameters for a given transistor in common emitter configuration. It is widely used circuit and also A_I is high. To get the transistor h-parameters in other configurations, converts ion formulae are used.

The Two Stage Cascaded Amplifier Circuit

The Transistor Q1 is in Common Emitter configuration. The second Transistor Q2 is in Common Collector (CC) configuration. Output is taken across 5K, the emitter resistance. Collector is at ground potential in the A.C. equivalent circuit. Biasing resistors are not shown since their purpose in only to provide the proper operating point and they do not affect the response of the amplifier. In the low frequency equivalent circuit, since the capacitors have large value, and so is X_C low, and can be neglected. So the capacitive reactance is not considered, and capacitive reactance X_C is low when C is large and taken as short circuit.



The small signal Common Emitter configuration circuit reduces as shown in Fig. In this circuit Q2 collector is at ground potential, in AC equivalent circuit. It is in Common Collector configuration and the output is taken between emitter point E2 and ground. So the circuit is redrawn as shown in Figure indicating voltages at different stages and input and output resistances.



Choice of Transistor in a Cascaded Amplifier Configuration

By connecting transistor in cascade, voltage gain gets multiplied. But what type of configuration should be used? Common Collector(CC) or Common Base(CB) or Common

Emitter(CE)? To get voltage amplification and current amplification, only Common Emitter (CE) configuration is used. Since it is Common Collector amplifier, the voltage gain is less than one for each stage. So the overall amplification is less than 1.

Common Base Configuration is also not used since Al is less than 1.

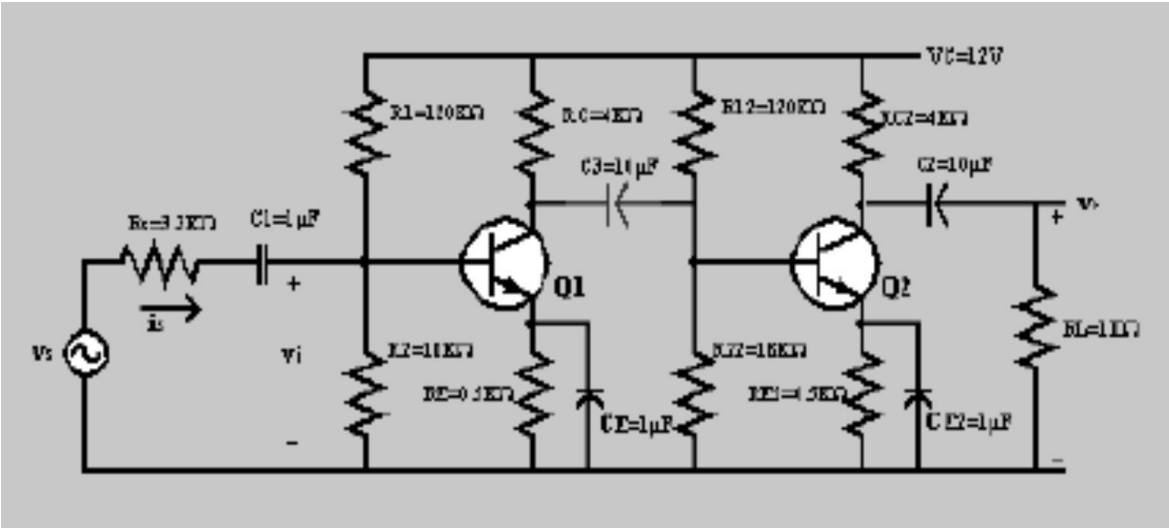
$$A_V = A_I \times \frac{R_L}{R_i}$$

Effective load resistance R_L is parallel combination of R_C and R_i of the following stage, (next stage) (since in multi stage connection, the output of one stage is the input to the other stage). This parallel combination is less than R_i. Therefore $R_L/R_i < 1$.

The current gain A_I in common base configurations is hib< 1 or =1.Therefore overall voltage gain = 1. Therefore Common Base configuration is not used for cascading. So only Common Emitter configuration is used (hfe>> I).Therefore overall voltage gain and current gains are> 1 in Common Emitter configuration.

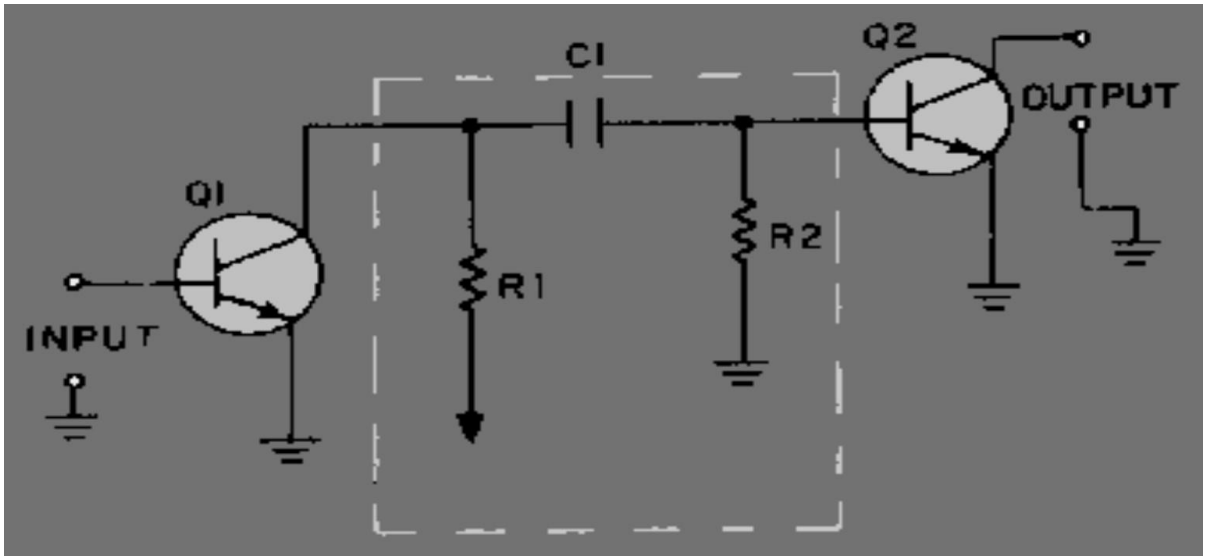
Two stage RC coupled amplifier

One way to connect various stages of a multistage amplifier is via capacitors, as indicated in the two-stage amplifier in Figure. Where two stages of common emitter amplifier are coupled to each other by the capacitor C3.



In RC-coupled amplifiers:

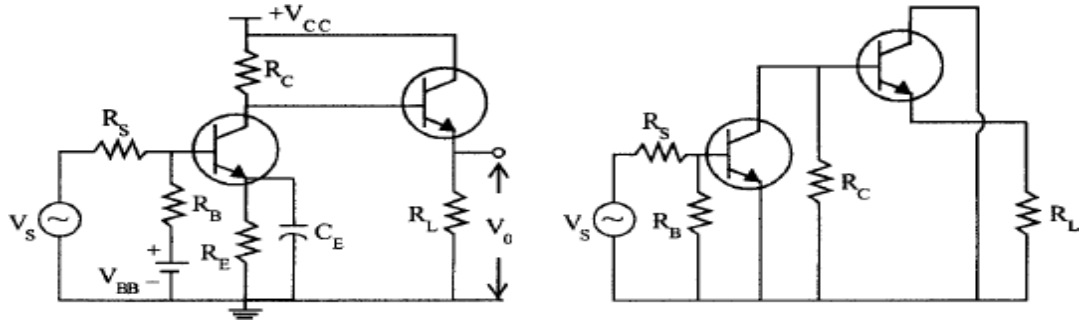
1. The various stages are DC isolated. This feature facilitates the biasing of individual stages.
2. The various stages can be similar. Hence the design of the amplifier is simplified.
3. The coupling capacitors influence the responses of the amplifier.
4. A great number of biasing resistors is necessary.



The most commonly used coupling in amplifiers is RC coupling. An RC-coupling network is shown in the illustration above. The network of R1, R2, and C1 enclosed in the dashed lines of the figure is the coupling network. You may notice that the circuitry for Q1 and Q2 is incomplete. That is intentional so that you can concentrate on the coupling network. R1 acts as a load resistor for Q1 (the first stage) and develops the output signal of that stage. Do you remember how a capacitor reacts to ac and dc? The capacitor, C1, "blocks" the dc of Q1's collector, but "passes" the ac output signal. R2 develops this passed, or coupled, signal as the input signal to Q2 (the second stage). This arrangement allows the coupling of the signal while it isolates the biasing of each stage. This solves many of the problems associated with direct coupling.

CE - CC Amplifiers

This is another type of two-stage BJT amplifier. The first stage in Common Emitter (CE) configuration provides voltage and current gains. The second stage in Common-Collector (CC) configuration provides impedance matching. This circuit is used in audio frequency amplifiers. The circuit is shown in Fig.



$$R_{L_2} \simeq R_L$$

$$h_{oc}\ R_{L_1} \leq 0.1$$

$$A_{I2} = A_{I'2} = (1 + h_{fe})$$

$$R_{i_2} = (1 + h_{fe})\ R_{L_2}$$

$$A_{V2} = A_{V2'} = \frac{A_{I_2} . R_{L_2}}{R_{i_2}}$$

$$= \frac{\left(1 + h_{fe}\ R_{L_2}\right)}{h_{ie} + \left(1 + h_{fe}\right) R_{L_2}}$$

$$= 1 - \frac{h_{ie}}{R_{i_2}};$$

$$A_{V_2} < 1$$

$$A_{I_1} = A_{I_1}' = -h_{fe}$$

$$R_{i_1} = R_{i_1}' = h_{ie}$$

$$A_{V_1} = A_{V_1}' = (A_{I_1} . R_{L_1} / R_i)$$

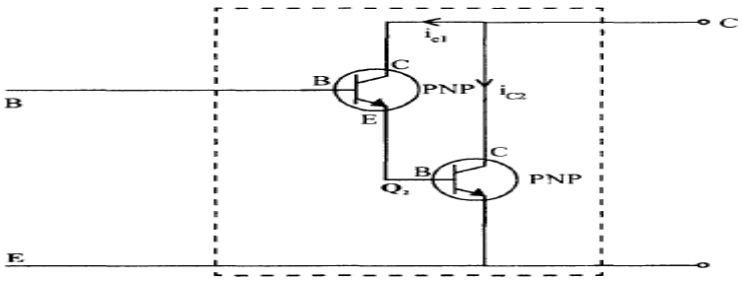
$$A_V = A_{V_1} \cdot A'_{V_2}$$
$$R_i = R_{i_1}$$
$$R_0 = R_{0_2}$$
$$A_I = \frac{A_V \cdot R_{i_1}}{R_{L_2}}$$

High Input Resistance Transistor Circuits

In some applications the amplifier circuit will have to have very high input impedance. Common Collector Amplifier circuit has high input impedance and low output impedance. But it's A_V<1.If the input impedance of the amplifier circuit is to be only 500 KO or less the Common Collector Configuration can be used. But if still higher input impedance is required a circuit. This circuit is known as the Darlington Connection (named after Darlington) or Darlington Pair Circuit.

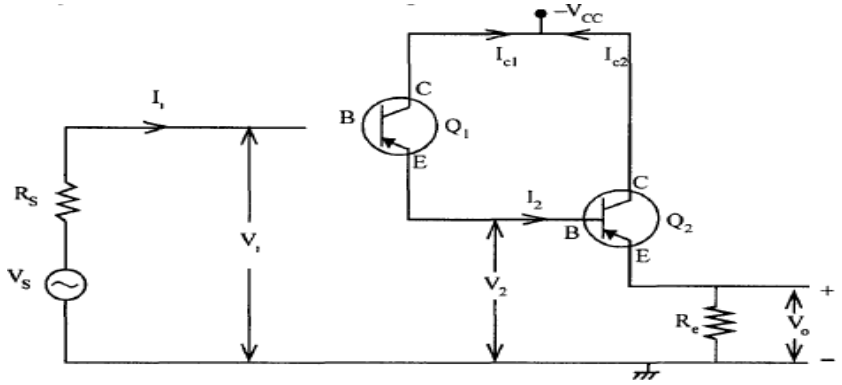
The Darlington Pair

This is two transistors connected together so that the amplified current from the first is amplified further by the second transistor. This gives the Darlington pair a very high current gain such as 10000. Darlington pairs are sold as complete packages containing the two transistors. They have three leads (B, C and E) which are equivalent to the leads of a standard individual transistor.

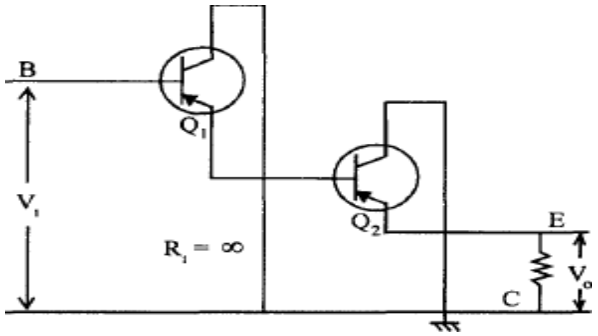


In this circuit, the two transistors are in Common Collector Configuration. The output of the first transistor Q1 (taken from the emitter of the Q1) is the input to the second transistor Q2 at

the base. The input resistance of the second transistor constitutes the emitter load of the first transistor. So, Darlington Circuit is nothing but two transistors in Common Collector Configuration connected in series. The same circuit can be redrawn as AC equivalent circuit. So, DC is taken as ground shown in below Fig. Hence 'C' at ground potential, Collectors of transistors Q1and Q2 is at ground potential.



There is no resistor connected between the emitter of Q1 and ground i.e., Collector Point.So, we can assume that infinite resistance is connected between emitter and collector.



The overall current gain is equal to the two individual gains multiplied together: Darlington

pair current gain, $h_{FE} = h_{FE1} \times h_{FE2}$

Here h_{FE1} and h_{FE2} are the gains of the individual transistors If

both the transistors are identical then

Current gain

$$A_I = \frac{I_c}{I_{b_1}} \cong (h_{fe})^2$$

Input resistance

$$R_i \cong \frac{(1+h_{fe})^2 R_e}{1+h_{oe}h_{fe}R_e}$$

Voltage gain

$$A_v \cong \left(1 - \frac{h_{ie}}{Ri_2}\right)$$

Output resistance

$$R_{o2} = \frac{R_s + h_{ie}}{(1+h_{fe})^2} + \frac{h_{ie}}{1+h_{fe}}$$

Therefore, the characteristic of Darlington Circuit are

1. Very High Input Resistance
2. Very Large Current Gain
3. Very Low Output Resistance
4. Voltage Gain, $A_V < 1$.

This gives the Darlington pair a very high current gain, such as 10000, so that only a tiny base current is required to make the pair switch on.

A Darlington pair behaves like a single transistor with a very high current gain. It has three leads (B, C and E) which are equivalent to the leads of a standard individual transistor. To turn on there must be 0.7V across both the base-emitter junctions which are connected in series inside the Darlington pair, therefore it requires 1.4V to turn on.

Darlington pairs are available as complete packages but you can make up your own from two transistors; TR1 can be a low power type, but normally TR2 will need to be high power. The maximum collector current Ic(max) for the pair is the same as Ic(max) for TR2.

A Darlington pair is sufficiently sensitive to respond to the small current passed by your skin and it can be used to make a touch-switch as shown in the diagram. For this circuit which just lights an LED the two transistors can be any general purpose low power transistors. The 100k resistor protects the transistors if the contacts are linked with a piece of wire. Two transistors may be combined to form a configuration known as the Darlington pair which behaves like a single transistor with a current gain equivalent to the product of the current gain of the two transistors. This is especially useful where very high currents need to be controlled as in a power amplifier or power-regulator circuit. Darlington transistors are available whereby two transistors are combined in one single package. The base-emitter volt-drop is twice that of a small transistor.

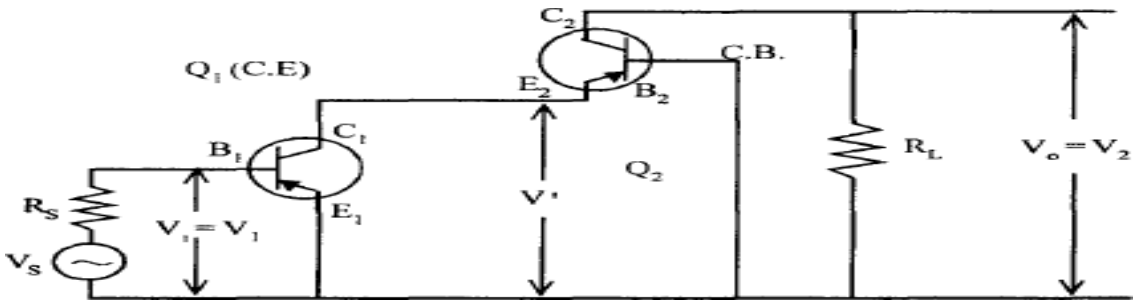
Disadvantages

1. The h-parameters for both the transistors will not be the same.
2. Leakage Current is more

The CASCODE Transistor Configuration

The circuit is shown in Figure. This transistor configuration consists of a Common Emitter Stage in cascade with a Common Base Stage. The collector current of transistor Q) equals the emitter current of Q_2.

The transistor Q_1 is in Common Emitter Configuration and transistor Q_2 is in Common Base Configuration. Let us consider the input impedance (h_{11}) etc., output admittance (h_{22}) i.e. the h - parameters of the entire circuit in terms of the h- parameters of the two transistors



Input impedance

$$h_{11} = \text{Input } Z = \left.\frac{V_1}{I_1}\right|_{V_2 = 0}$$

$$h_{11} \cong h_{ie}$$

Short circuit current gain

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0}$$

$$h_{21} = \frac{I_2}{I_1} = \frac{I}{I_1} \times \left.\frac{I_2}{I_0}\right|_{V_2 = 0}$$

$$\frac{I'}{I_1} = h_{fe} \qquad \text{since, } I = I_{C_1}.\ I_1 = I_{B_1}$$

$$\frac{I_2}{I'} = -\,h_{fb} \quad \text{since, } I = I_{E_2}.\ I_2 = I_{C_2}.$$

$$h_{21} = -\,h_{fe}.\ h_{fb}.$$

$$h_{fe} >> 1\ .\ -\,h_{fb} \simeq 1, \qquad \text{since } h_{fb} = \frac{I_C}{I_E}$$

$$\boxed{h_{21} \cong h_{fe}}$$

Output conductance

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0}$$

Reverse voltage gain

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0}$$

$$= \left.\frac{V_1}{V'} \times \frac{V^1}{V_2}\right|_{I_1 = 0}$$

$$\left.\frac{V_1}{V_0'}\right|_{I_i = 0} = h_{re} \cdot \left.\frac{V'}{V_2}\right| = h_{rb}$$

$h_{12} \cong h_{re}\, h_{rb}$.
$h_{re} \cong 10^{-4}$ $h_{rb} = 10^{-4}$. $\because$ h_{12} is very small
$h_i = h_{11} \cong h_{ie}$. Typical value = 1.1KΩ
$h_f = h_{21} \cong h_{fe}$. Typical value = 50
$h_o = h_{22} \cong h_{ob}$. Typical value = 0.49 μ A/V
$h_r = h_{12} \cong h_{re}\, h_{rb}$. Typical value = 7×10^{-8}.

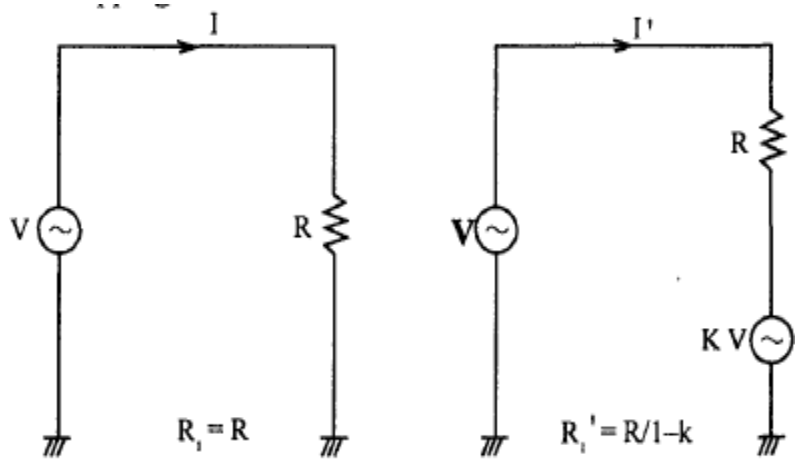
Therefore, for a CASCODE Transistor Configuration, its input Z is equal to that of a single Common Emitter Transistor (hie)' Its Current Gain is equal to that of a single Common Base Transistor (hfe). Its output resistance is equal to that of a single Common Base Transistor (hob)' the reverse voltage gain is very small, i.e., there is no link between V 1 (input voltage) and V 2 (output voltage). In other words, there is negligible internal feedback in the case of, a CASCODE Transistor Circuit, acts like a single stage C.E. Transistor (Since hie and hfe are same) with negligible internal feedback (:.hre is very small) and very small output conductance, (= hob) or large output resistance (=2MΩ equal to that of a Common Base Stage). The above values are correct, if we make the assumption that hob RL< 0.1 or RL is <200K.

CASCODE Amplifier will have

1. Very Large Voltage Gain.
2. Large Current Gain
3. Very High Output Resistance.

Boot-strap emitter follower

The maximum input resistance of a practical Darlington Circuit is only 2 MΩ. Higher input resistance cannot be achieved because of the biasing resistors R1, R2 etc. They come in parallel with Ri of the transistors and thus reduce the value of Ri. The maximum value of Ri is only 1/hob since, hob is resistance between base and collector. The input resistance can be increased greatly by boot strapping, the Darlington Circuit through the addition of Co between the first collector C1 and emitter B2.

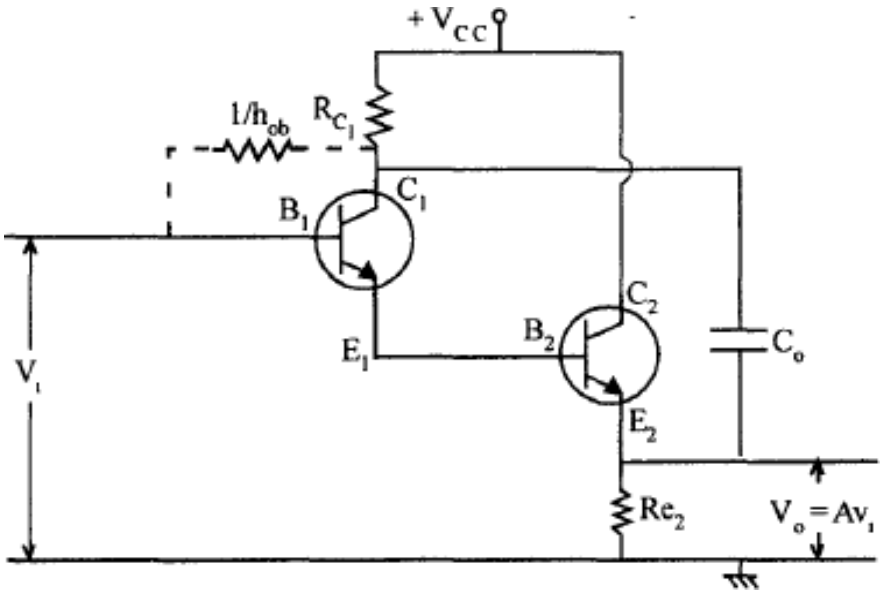


Boot strapping

In Fig, V is an AC signal generator, supplying current I to R. Therefore, the input resistance of V seen by the generator is R1 = V/I= R itself. Now suppose, the bottom end of R is not at ground potential but at higher potential i.e. another voltage source of KV (K < I) is connected between the bottom end of R and ground. Now the input resistance of the circuit is

$$R_i' = \frac{V}{I'} \qquad I' = \frac{(V - KV)}{R}$$

$$R_i' = \frac{VR}{V(1-K)} = \frac{R}{1-K}$$

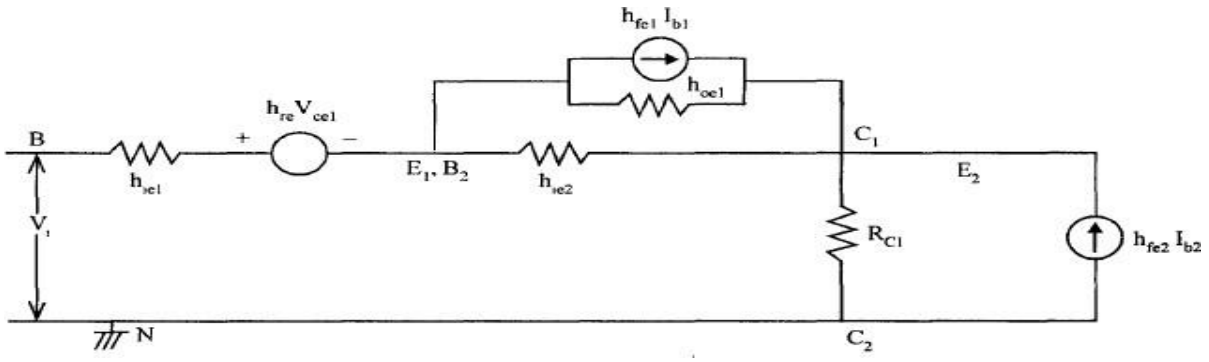


I' can be increased by increasing V. When V increases KV also increases. K is constant.Therefore the potential at the two ends of R will increase by the same amount, K is less than 1, therefore R_i> R. Now if K = 1, there is no current flowing through R (So V = KV there is nopotential difference). So the input resistance R\ = 00. Both the top and bottom of the resistorterminals are at the same potential. This is called as the Boots Strapping method which increases theinput resistance of a circuit. If the potential at one end of the resistance changes, the other end of Ralso moves through the same potential difference. It is as if R is pulling itself up by its boot straps.For CC amplifiers A_V< 1 = 0.095. So R_i can be made very large by this technique. K = Av = 1.Ifwe pull the boot with both the edges of the strap (wire) the boot lifts up. Here also, if the potentialat one end ofR is changed, the voltage at the other end also changes or the potential level ofR3 rises,as if it is being pulled up from both the ends.

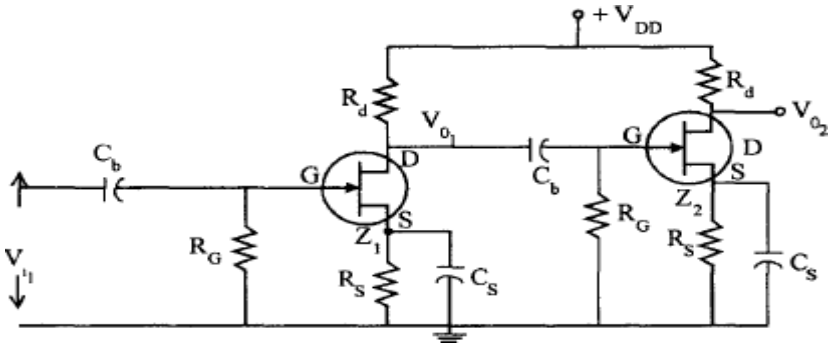
$$R_i = \frac{h_{ie}}{1 - A_V}; \quad A_V \cong 1.$$

$$R_i = \frac{R}{1 - K}$$

AC Equivalent circuit



Two Stage RC Coupled JFET amplifier (in Common Source (CS) configuration)
The circuit for two stages of RC coupled amplifier in CS configuration is as shown in fig.



The output Vo of I Stage is coupled to the input Vi of II Stage through a blocking capacitor Cb. It blocks the DC components present in the output or I Stage from reaching the input of the I stage which will alter the biasing already fixed for the active device. Resistor Rg is connected between gate and ground resistor Ro is connected between drain and V_{DD} supply. CS is the bypass capacitor used to prevent loss of gain due to negative feedback. The active device is assumed to operate in the linear region. So the small signal model of the device is valid. Frequency Roll-off is the term used for the decrease in gain with frequency in the uppercut-off region. It is expressed as db/octave on db/decade.

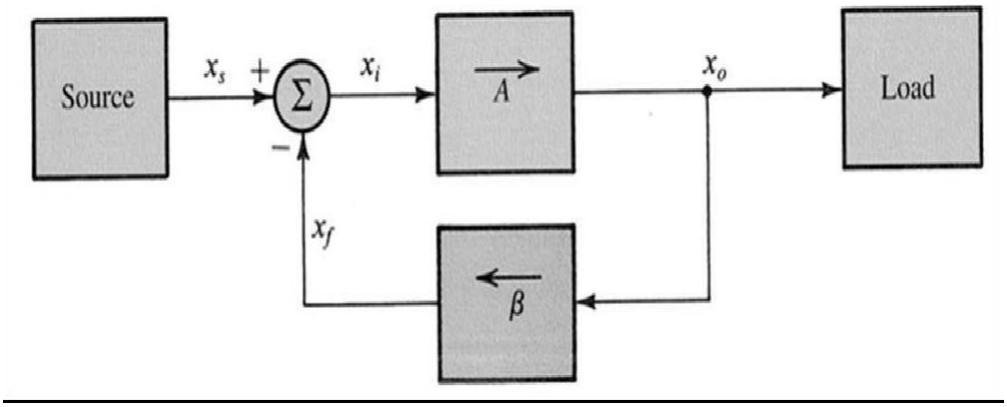
The purpose of multistage amplifiers is to get large .gain. So with BJTs, Common Emitter Configuration is used. If JFETs are employed, common source configuration is used.

MODULE II

FEEDBACK AMPLIFIERS

Feedback Amplifiers : Feedback principle and concept, types of feedback, classification of amplifiers, feedback topologies, Characteristics of negative feedback amplifiers, Generalized analysis of feedback amplifiers, Performance comparison of feedback amplifiers, Method of analysis of feedback amplifiers.

FEEDBACK AMPLIFIER:



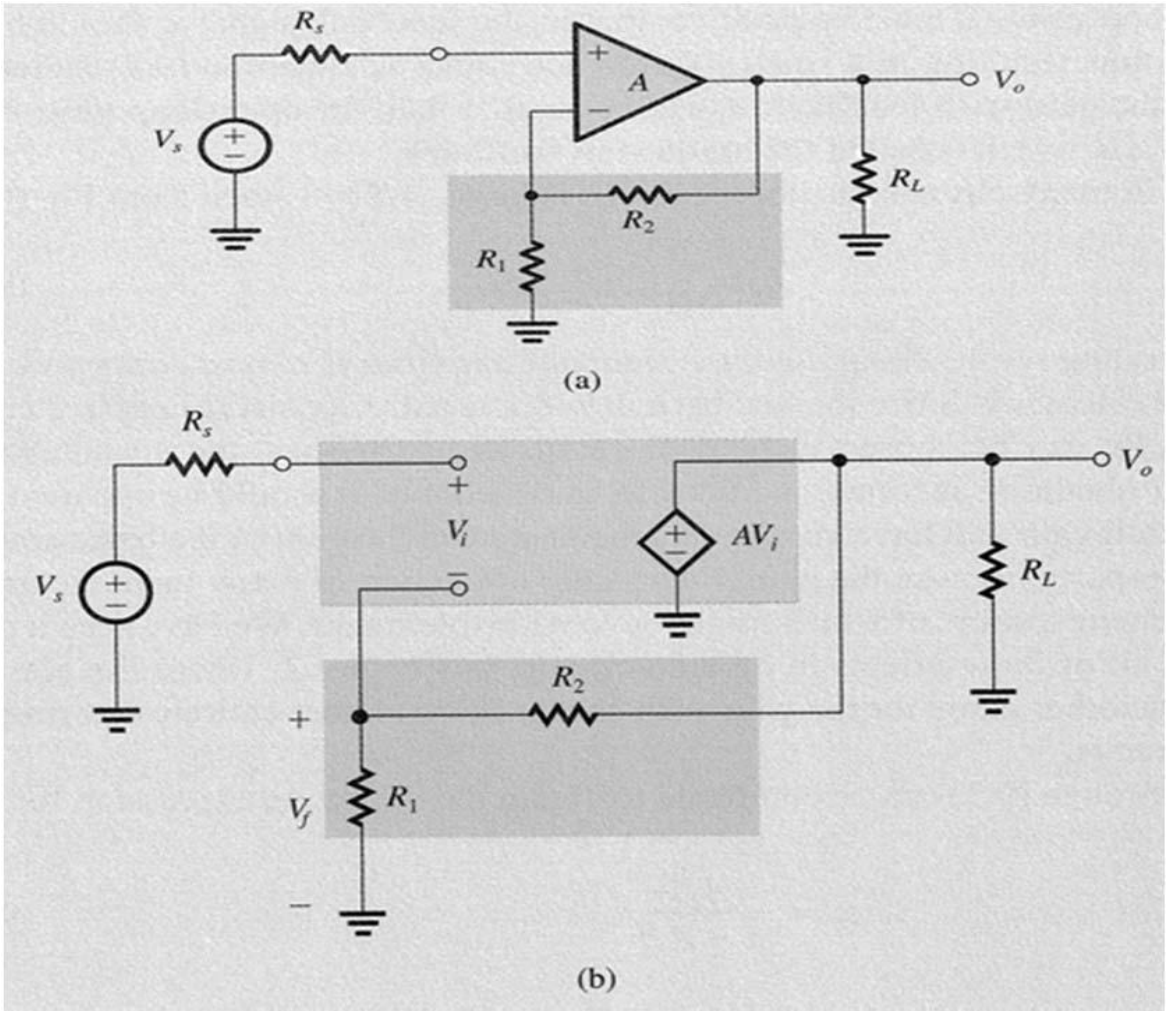
- Signal-flow diagram of a feedback amplifier
- Open-loop gain: A
- Feedback factor:
- Loop gain: A
- Amount of feedback: 1 + A
- Gain of the feedback amplifier (closed-loop gain):

Negative feedback:

- The feedback signal xf is subtracted from the source signal xs
- Negative feedback reduces the signal that appears at the input of the basic amplifier
- The gain of the feedback amplifier Af is smaller than open-loop gain A by a factor of (1+A)
- The loop gain A is typically large (A >>1):
- The gain of the feedback amplifier (closed-loop gain)
- The closed-loop gain is almost entirely determined by the feedback network better accuracy of Af.
- xf = xs(A)/(1+A) xs error signal xi = xs – xf

For Example, The feedback amplifier is based on an op amp with infinite input resistance and zero output resistance.

- Find an expression for the feedback factor.
- Find the condition under which the closed-loop gain Af is almost entirely determined by the feedback network.
- If the open-loop gain A = 10000 V/V, find R2/R1 to obtain a closed-loop gain Af of 10 V/V.
- What is the amount of feedback in decibel?
- If Vs = 1 V, find Vo, Vf and Vi.
- If A decreases by 20%, what is the corresponding decrease in Af ?



Some Properties of Negative Feedback

- The negative reduces the change in the closed-loop gain due to open-loop gain variation

Gain de sensitivity:

$$dA_f = \frac{dA}{(1+A\beta)^2} \rightarrow \frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}$$

1 □ *A*□

- Desensitivity factor:

Bandwidth extension

High-frequency response of a single-pole amplifier:

$$A(s)=\frac{A_M}{1+s/\omega_H}\rightarrow A_f(s)=\frac{A_M/(1+A_M\beta)}{1+s/\omega_H(1+A_M\beta)}$$

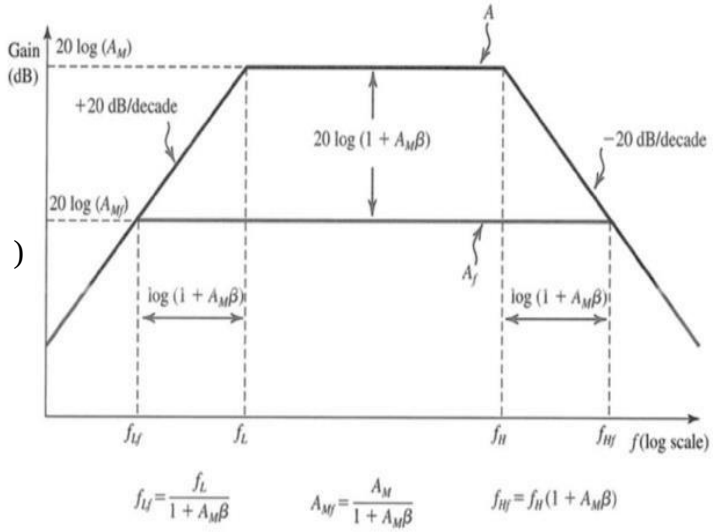
Low-frequency response of an amplifier with a dominant low-frequency pole:

$$A(s)=\frac{sA_M}{s+\omega_L}\rightarrow A_f(s)=\frac{sA_M/(1+A_M\beta)}{s+\omega_L/(1+A_M\beta)}$$

Negative feedback:

Reduces the gain by a factor of (1+AM)

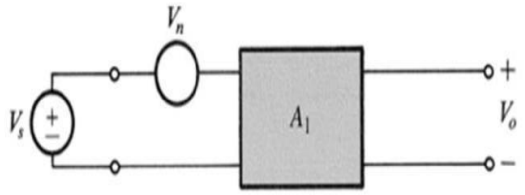
Extends the bandwidth by a factor of (1+AM)

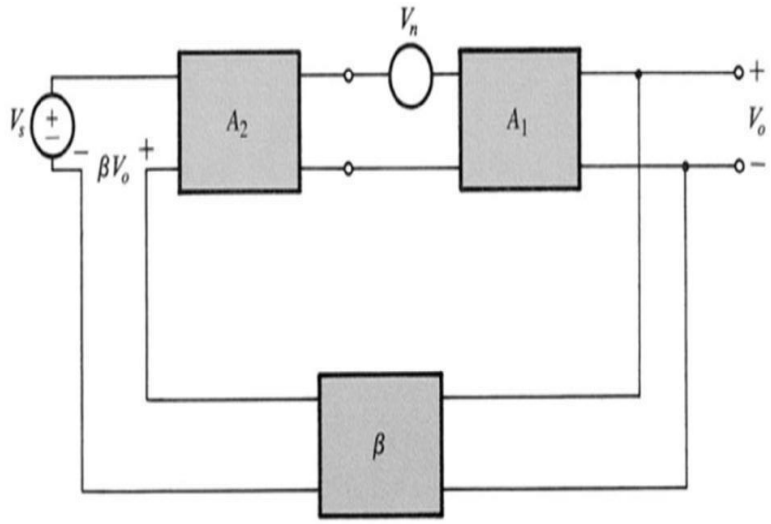


Interference reduction

- The signal-to-noise ratio:
  - The amplifier suffers from interference introduced at the input of the amplifier
  - Signal-to-noise ratio: S/I = Vs/Vn
- Enhancement of the signal-to-noise ratio:
  - Precede the original amplifier A1 by a clean amplifier A2
  - Use negative feedback to keep the overall gain constant.

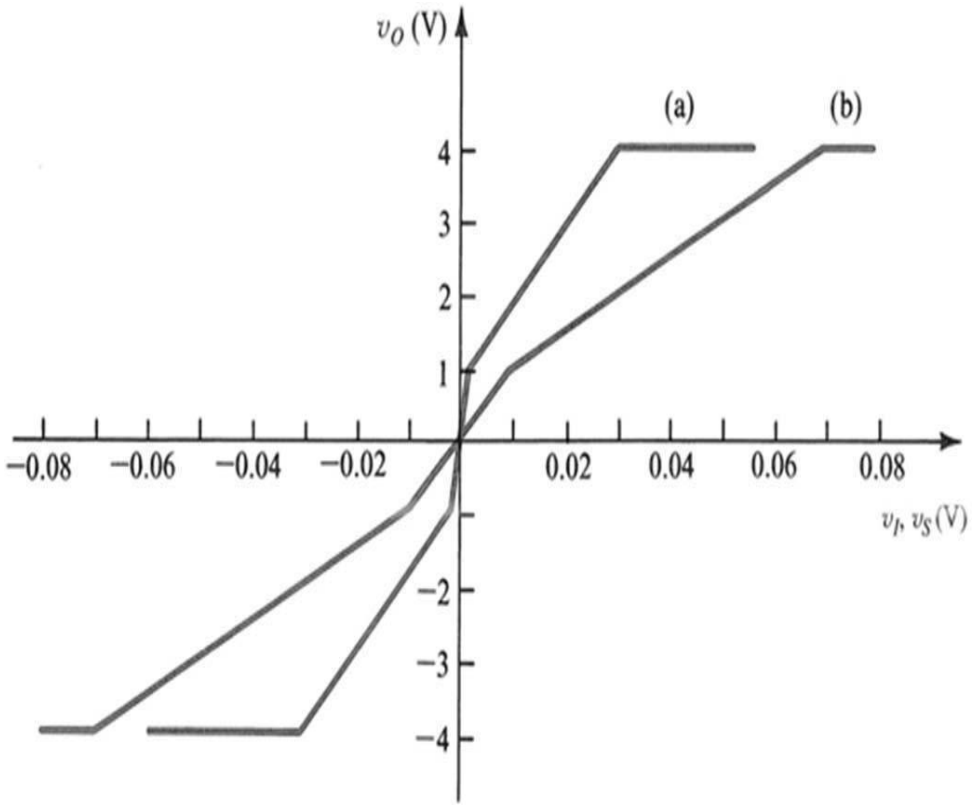
$$V_0 = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta} \rightarrow \frac{S}{I} = \frac{V_s}{V_n} A_2$$





Reduction in nonlinear distortion:

The amplifier transfer characteristic is linearised through the application of negative feedback.



□□ = 0.01

□ □ *A* changes from 1000 to 100

$$A_{f1} = \frac{1000}{1+1000\times 0.01} = 90.9$$

$$A_{f2} = \frac{100}{1+100\times 0.01} = 50$$

The Four Basic Feedback Topologies:

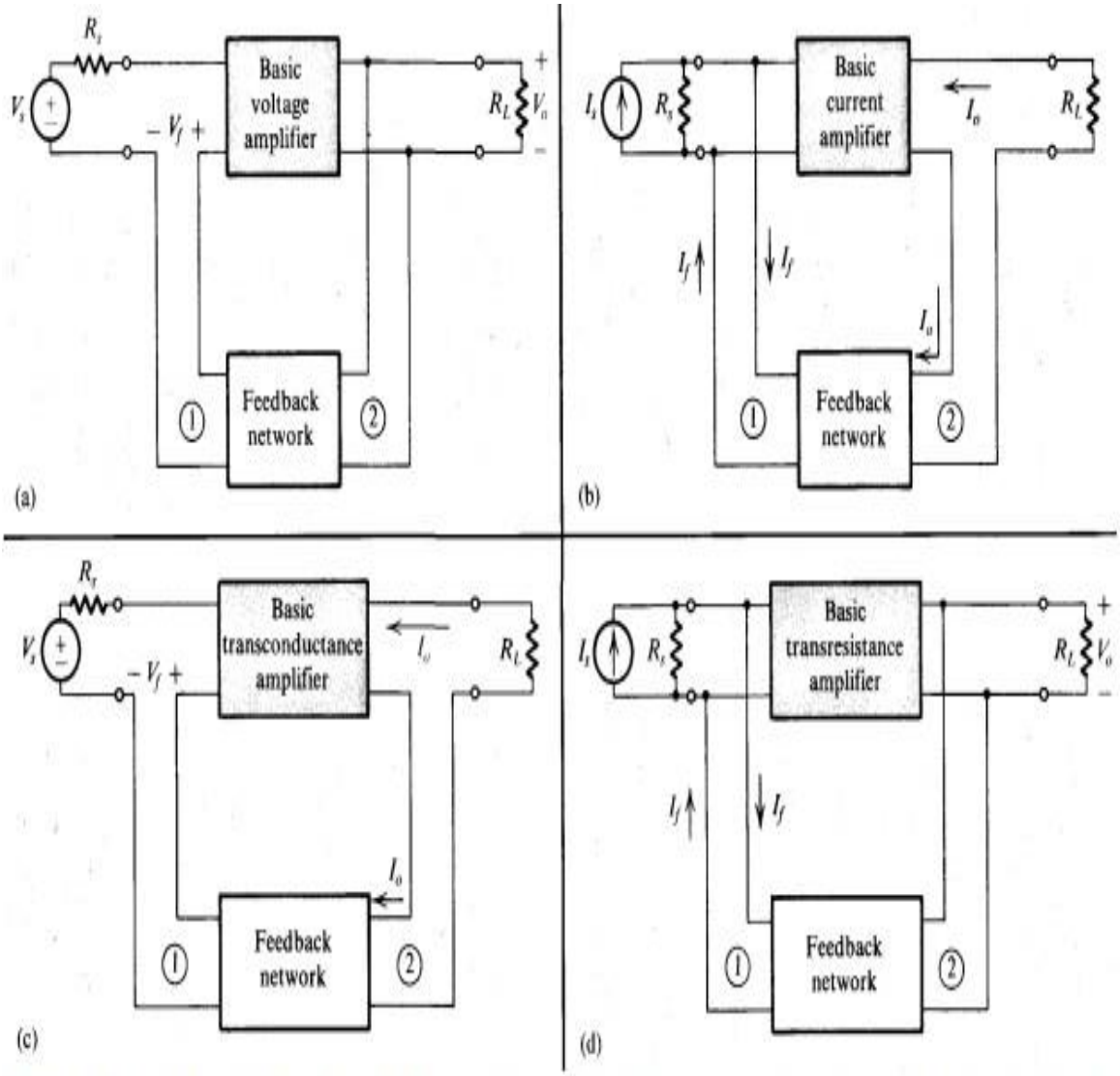
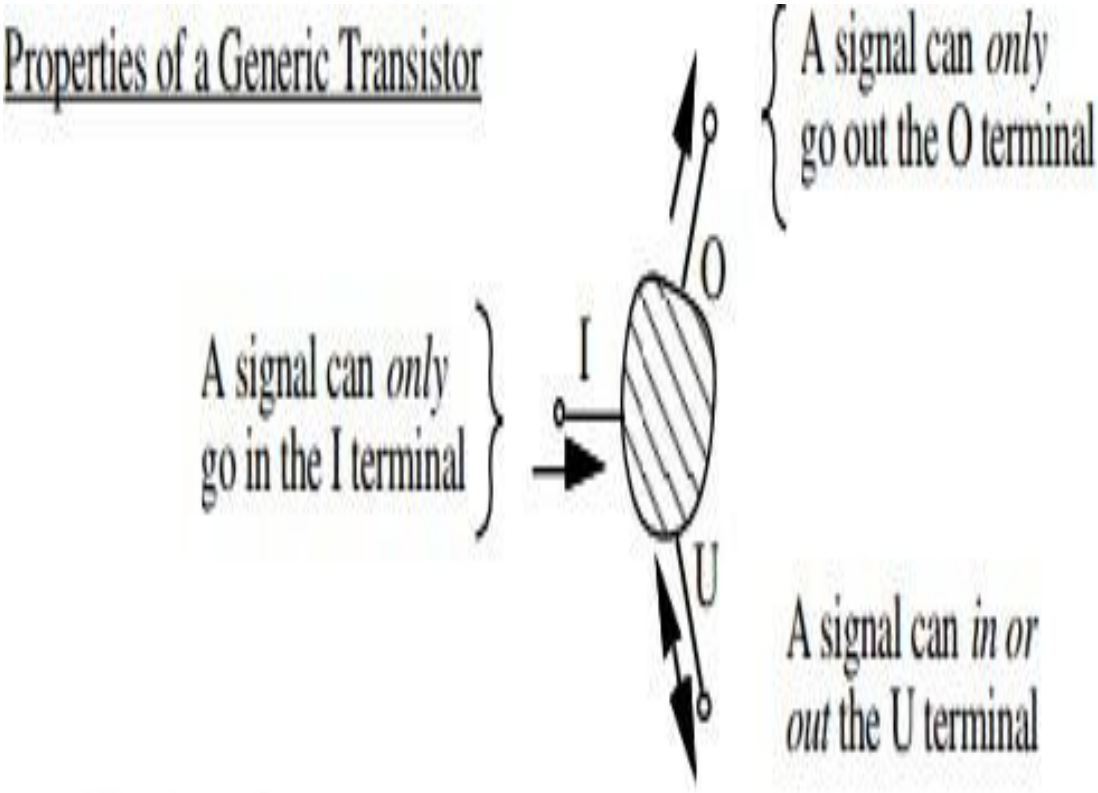


Fig. The four basic feedback topologies: (a) voltage-sampling series-mixing (series-shunt) topology; (b) current-sampling shunt-mixing (shunt-series) topology; (c) current-sampling series-mixing (series-series) topology; (d) voltage-sampling shunt-mixing (shunt-shunt) topology.

Method of analysis of Feedback Amplifiers:

1. Identify the topology.
2. Determine whether the feedback is positive or negative.
3. Open the loop and calculate A, ß, Ri, and Ro.
4. Use the Table to find Af, Rif and Rof or AF, RiF, and RoF.
5. Use the information in 4 to find whatever is required (v_{out}/v_{in}, R_{in}, R_{out}, etc.)

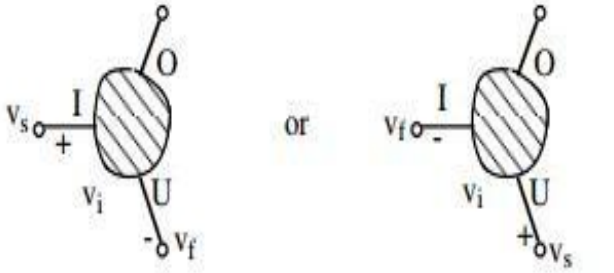


Identification of the Feedback Topology

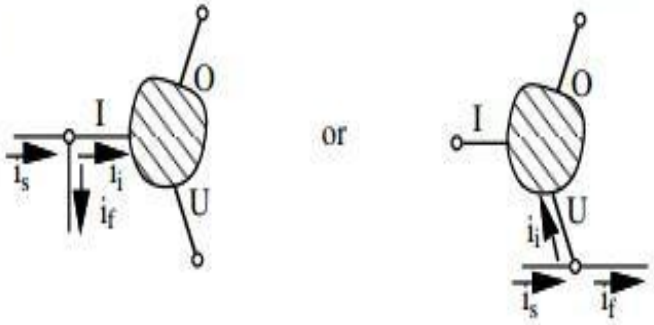
Isolate the input and output transistor(s) and apply the following identification.

Input

Series:

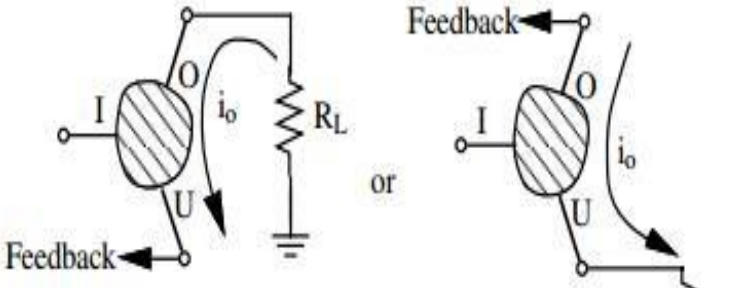


Shunt:

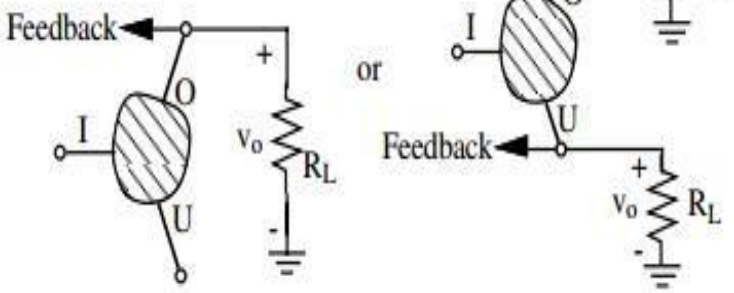


Output

Series:

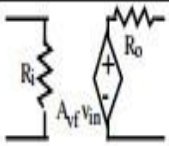
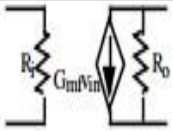
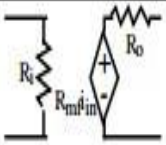
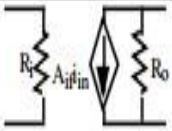
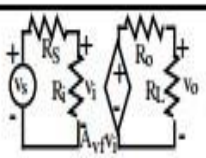
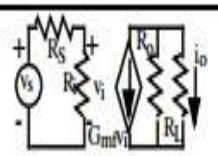
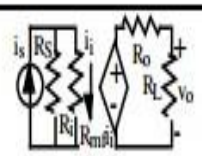
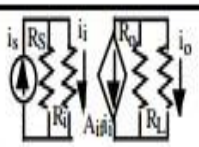
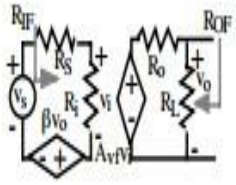
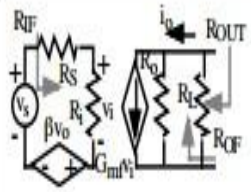
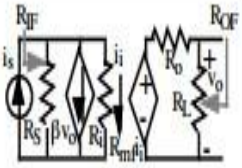
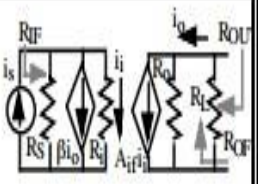


Shunt:



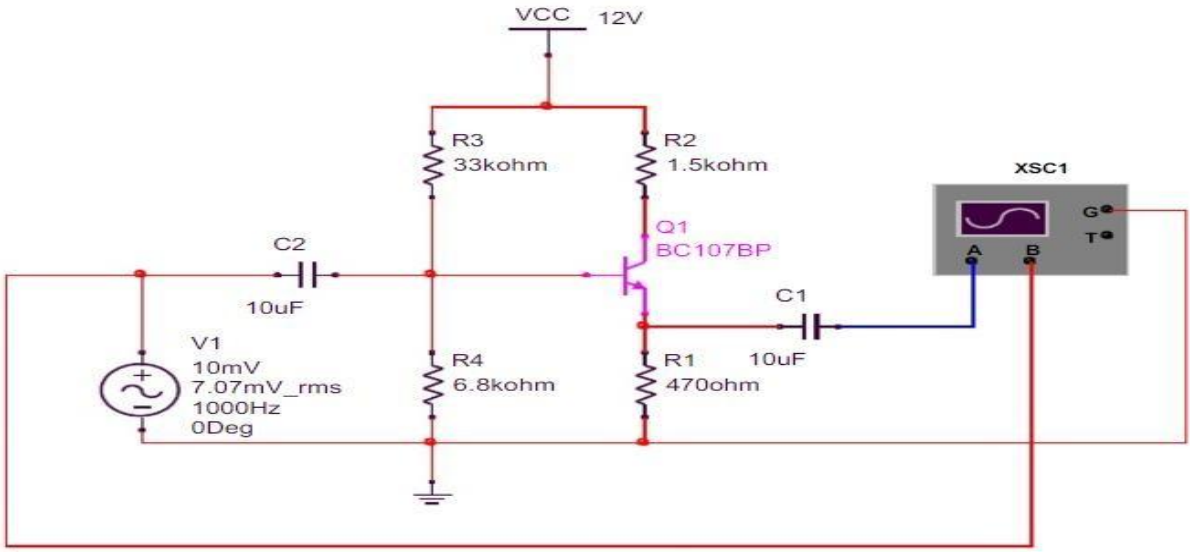
Performance comparison of feedback amplifiers:

Summary of the Important Relationships of Open-loop and Closed-loop Feedback Amplifiers.

Quantity	Voltage Amplifier	Transconductance Amplifier	Transresistance Amplifier	Current Amplifier
Input-output variable	Voltage-voltage	Voltage-current	Current-voltage	Current-current
Small Signal Model				
Small Signal Amplifier with Source & Load				
Ideal R_S	$R_S = 0$ or $R_S \ll R_i$	$R_S = 0$ or $R_S \ll R_i$	$R_S = \infty$ or $R_S \gg R_i$	$R_S = \infty$ or $R_S \gg R_i$
Ideal R_L	$R_L = \infty$ or $R_L \gg R_o$	$R_L = 0$ or $R_L \ll R_o$	$R_L = \infty$ or $R_L \gg R_o$	$R_L = 0$ or $R_L \ll R_o$
Overall Forward Gain	$A_V = \frac{R_i R_L A_{vf}}{(R_S+R_i)(R_L+R_o)}$	$G_M = \frac{R_i R_o G_{mf}}{(R_S+Ri)(R_L+R_o)}$	$R_M = \frac{R_S R_L R_{mf}}{(R_S+Ri)(R_L+R_o)}$	$A_I = \frac{R_S R_o A_{if}}{(R_S+Ri)(R_L+R_o)}$
Feedback Topology	Series-shunt	Series-series	Shunt-shunt	Shunt-series
Ideal ß, finite R_S and R_L Feedback Small Signal Models				
Closed-Loop Gain (Ideal R_S and R_L)	$A_{VF} = \frac{A_{Vf}}{(1+A_{vf}ß_v)}$	$G_{mF} = \frac{G_{mf}}{(1+G_{mf}ß_g)}$	$R_{mF} = \frac{R_{mf}}{(1+R_{mf}ß_r)}$	$A_{iF} = \frac{A_{if}}{(1+A_{if}ß_i)}$

Closed-Loop Input Resistance (Ideal R_S and R_L)	$R_{iF} = R_i(1 + A_{vf}\beta_v)$	$R_{iF} = R_i(1 + G_{mf}\beta_g)$	$R_{iF} = \frac{R_i}{1 + R_{mf}\beta_r}$	$R_{iF} = \frac{R_i}{1 + A_{if}\beta_i}$
Closed-Loop Output Resistance (Ideal R_S and R_L)	$R_{oF} = \frac{R_o}{1 + A_{vf}\beta_v}$	$R_{oF} = R_o(1 + R_{mf}\beta_g)$	$R_{oF} = \frac{R_o}{1 + R_{mf}\beta_r}$	$R_{oF} = R_o(1 + A_{if}\beta_i)$
Closed-Loop Gain	$A_{VF} = \frac{A_V}{(1+A_V\beta_v)}$	$G_{MF} = \frac{G_M}{(1+G_M\beta_g)}$	$R_{MF} = \frac{R_M}{(1+R_M\beta_r)}$	$A_{IF} = \frac{A_I}{(1+A_I\beta_i)}$
Closed-Loop Input Resistance	$R_{IF} = (R_i+R_S)(1+A_V\beta_v)$	$R_{IF} = (R_i+R_S)(1 + G_M\beta_g)$	$R_{IF} = \frac{\frac{R_iR_S}{R_i+R_S}}{1 + R_M\beta_r}$	$R_{IF} = \frac{\frac{R_iR_S}{R_i+R_S}}{1 + A_I\beta_i}$
Closed-Loop Output Resistance	$R_{OF} = \frac{\frac{R_oR_L}{R_o+R_L}}{1 + A_V\beta_v}$	$R_{OF} = (R_o+R_L)(1+G_M\beta_g)$	$R_{OF} = \frac{\frac{R_oR_L}{R_o+R_L}}{1 + R_M\beta_r}$	$R_{OF} = (R_o+R_L)(1+A_I\beta_i)$
Output Resistance of Series Output Fb. Ckt	$R_{OUT} = R_{OF}$	$R_{OUT} = \frac{R_L}{R_{OF}}(R_{OF}-R_L)$	$R_{OUT} = R_{OF}$	$R_{OUT} = \frac{R_L}{R_{OF}}(R_{OF}-R_L)$

In voltage series feedback amplifier, sampling is voltage and series mixing indicates voltage mixing. As both input and output are voltage signals and is said to be voltage amplifier with gain A_{vf}.



Band width is defined as the range frequencies over which gain is greater than or equal to 0.707 times the maximum gain or up to 3 dB down from the maximum gain

Bandwidth (BW) = f_h- f_l Where

f_h= Upper cutoff frequency And f_l=

Lower cutoff frequency.

Cutoff frequency is the frequency at which the gain is 0.707 times the maximum gain or 3dB down from the maximum gain. In all feedback amplifiers we use negative feedback, so gain is reduced and bandwidth is increased

$$A_{vf} = Av/[1+A_v\beta] \; And$$

$$BW_f = BW\,[1+ A_v\beta]$$

Where A_{vf} = Gain with feedback Av=

Gain without feedback β=feedback

gain

BW_f = Bandwidth with feedback and

BW = Bandwidth without feedback Output resistance will decrease due to shunt connection at output and input resistance will increase due to series connection at input.

So $R_{0f} = R_0/[1+A\nu\beta]$ and

$R_{if} = R_i[1+A\nu\beta]$.

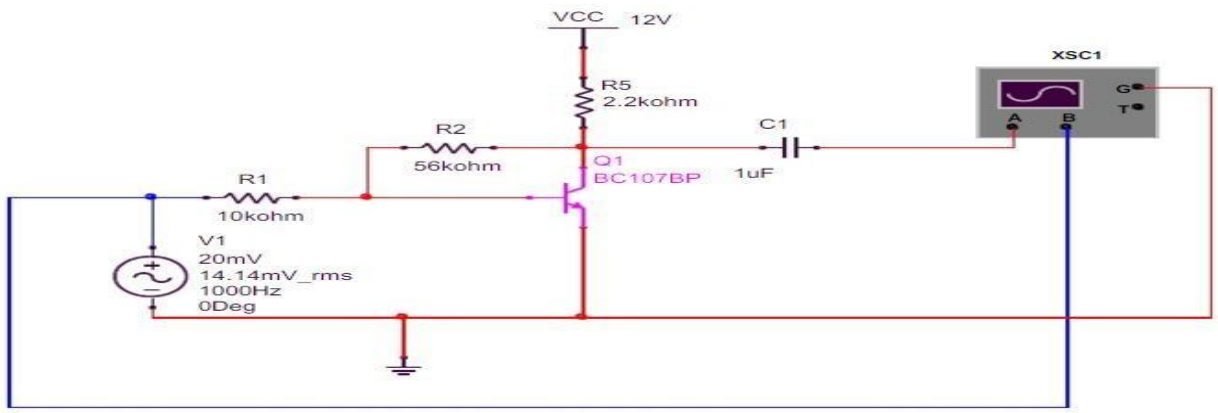
Where R 0f = Output resistance with feedback R_0= Output

resistance without feedback.

R_{if}= Input resistance with feedback R_i= Input

resistance without feedback

In voltage shunt feedback amplifier, sampling is voltage and shunt mixing indicates current mixing. As input is current signal and output is voltage signal, so it is said to be trans- resistance amplifier with gain R_{mf}.



Band width is defined as the range frequencies over which gain is greater than or equal to 0.707 times the maximum gain or up to 3 dB down from the maximum gain.

Bandwidth (BW) = f_h- f_l Where

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Lower cutoff frequency.

Cutoff frequency is the frequency at which the gain is 0.707 times the maximum gain or 3dB down from the maximum gain. In all feedback amplifiers we use negative feedback, so gain is reduced and bandwidth is increased.

$$R_{mf} = Rm/[1+R_m\beta]$$

$$And\ BW_f = BW\ [1+ R_m\beta]$$

Where

R_{mf} = Gain with feedback **R_m**=

Gain without feedback

β=feedback gain

BW = Bandwidth without feedback

Output resistance and input resistance both will decrease due to shunt connections at input and output. So

$$\mathbf{R_{0f} = R_0/[1+ R_m \beta]\ and}$$

$$\mathbf{R_{if} = R_i/[1+ R_m \beta].}$$

Where R 0f = Output resistance with feedback R_0= Output

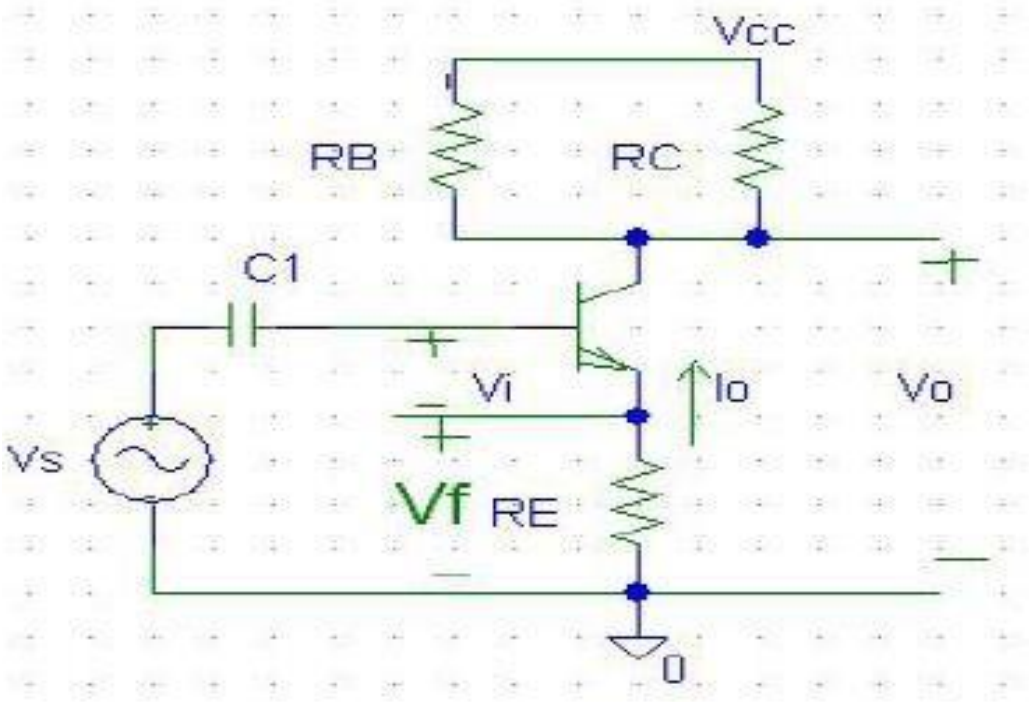
resistance without feedback.

R_{if}= Input resistance with feedback R_i= Input

resistance without feedback

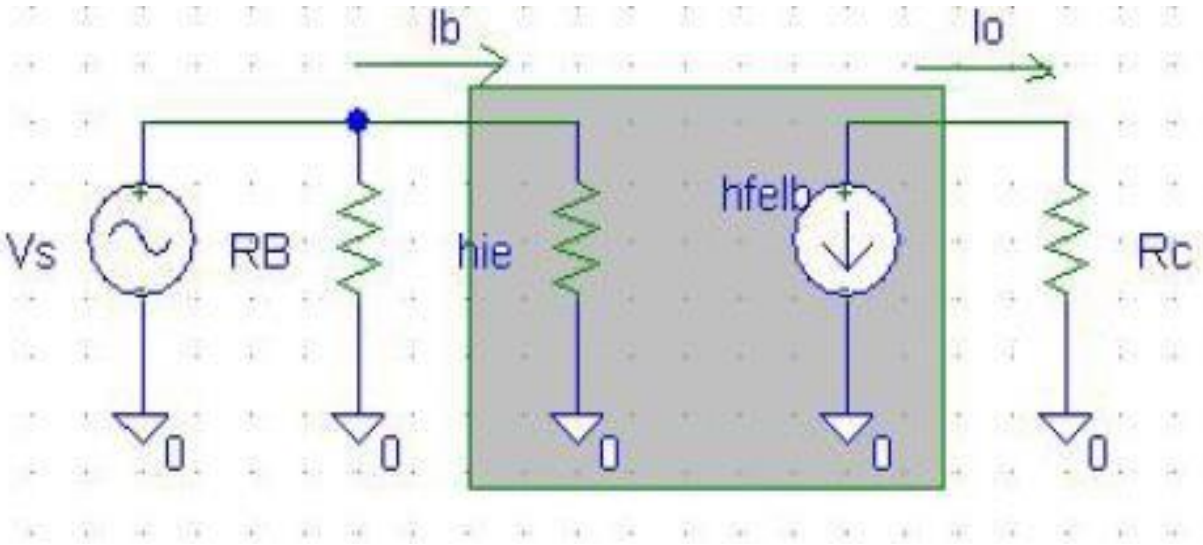
Current series feedback

- Feedback technique is to sample the output current (Io) and return a proportional voltage in series.
- It stabilizes the amplifier gain, the current series feedback connection increases the input resistance.
- In this circuit, emitter of this stage has an un bypassed emitter, it effectively has current-series feedback.
- The current through RE results in feedback voltage that opposes the source signal applied so that the output voltage Vo is reduced.



• To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is done in most of the amplifiers)

The fig below shows the equivalent circuit for current series feedback



Gain, input and output impedance for this condition is,

$$A_f = \frac{I_o}{V_s} = \frac{A}{1+A\beta} = \frac{-h_{fe}/h_{ie}}{1+(-R_E)\left(\frac{-h_{fe}}{h_{ie}+R_E}\right)}$$

$$Z_{if} = Z_i(1+A\beta) \cong h_{ie}\left(1+\frac{h_{fe}R_E}{h_{ie}}\right)$$

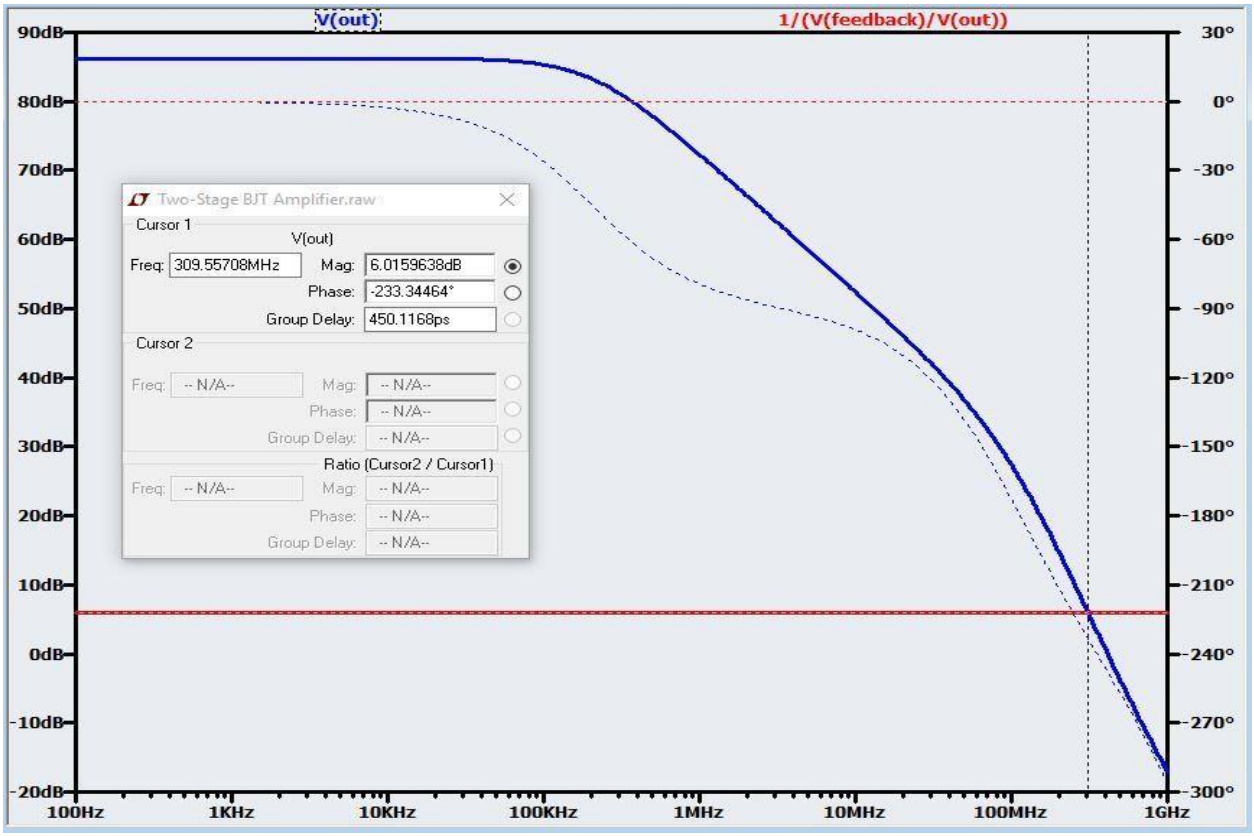
$$Z_{of} = Z_o(1+A\beta) \cong R_c\left(1+\frac{h_{fe}R_E}{h_{ie}}\right)$$

$$with-feedback..A;$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_c}{V_s} = \left(\frac{I_o}{V_s}\right)R_c = A_f R_C \cong \frac{-h_{fe}R_C}{h_{ie}+h_{fe}R_E}$$

We now know that by plotting the gain and phase shift of a negative feedback amplifier's loop gain—denoted by $A\beta$, where A is always a function of frequency and β can be considered a function of frequency if necessary—we can determine two things: 1) whether the amplifier is stable, and 2) whether the amplifier is *sufficiently* stable (rather than *marginally* stable). The first determination is based on the stability criterion, which states that the magnitude of the loop gain must be less than MODULEy at the frequency where the phase shift of the loop gain is 180°. The second is based on the amount of gain margin or phase margin; a rule of thumb is that the phase margin should be at least 45°.

It turns out that we can effectively analyze stability using an alternative and somewhat simplified approach in which open-loop gain A and feedback factor β are depicted as separate curves on the same axes. Consider the following plot for the discrete BJT amplifier with a frequency-independent (i.e., resistor-only) feedback network configured for $\beta = 0.5$:



Here you see V(out), which corresponds to the open-loop gain, and 1/(V(feedback)/V(out)). If you recall that β is the percentage (expressed as a decimal) of the output fed back and subtracted from the input, you will surely recognize that this second trace is simply $1/\beta$. So why did we plot $1/\beta$? Well, we know that loop gain is A multiplied by β, but in this plot the y- axis is in decibels and is thus logarithmic. Our high school math teachers taught us that multiplication of ordinary numbers corresponds to addition with logarithmic values, and likewise numerical division corresponds to logarithmic subtraction. Thus, a logarithmic plot of A multiplied by β can be represented as the logarithmic plot of A **plus** the logarithmic plot of β. Remember, though, that the above plot includes not β but rather $1/\beta$, which is the equivalent of **negative** β on a logarithmic scale. Let's use some numbers to clarify this:

$$\beta=0.5 \Rightarrow 20\log(\beta)\approx -6 \text{ dB}\beta=0.5 \Rightarrow 20\log f(\beta)\approx -6 \text{ dB } 1\beta=2 \Rightarrow$$

$$20\log(1\beta)\approx 6 \text{ dB}1\beta=2 \Rightarrow 20\log f(1\beta)\approx 6 \text{ dB}$$

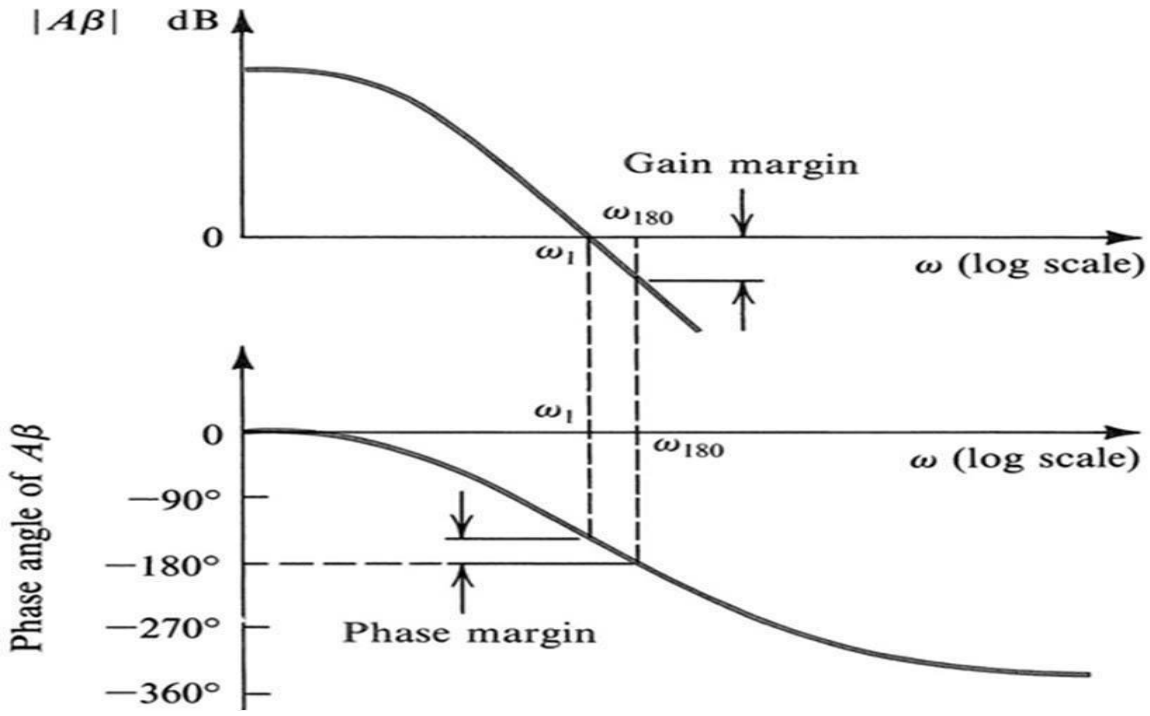
Thus, in this logarithmic plot, we have 20log(A) and -20log(β), which means that to reconstruct 20log($A\beta$) we need to **subtract the 1/β curve from the A curve**:

$20\log(A\beta)=20\log(A)+20\log(\beta) \Rightarrow 20\log(A\beta)=20\log(A)-(-20\log(\beta))$ $20\log(A\beta)=20\log(A)+20\log(\beta) \Rightarrow 20\log(A\beta)=20\log(A)-(-20\log(\beta))$

$$\Rightarrow 20\log(A\beta)=20\log(A)-20\log(1\beta).$$

Gain and phase margin

- The stability of a feedback amplifier is determined by examining its loop gain as a function of frequency.
- One of the simplest means is through the use of Bode plot for A .
- Stability is ensured if the magnitude of the loop gain is less than MODULEy at a frequency shift of 180 .
- Gain margin:
  - The difference between the value | | of at $_{180}$ and MODULEy. A
  - Gain margin represents the amount by which the loop gain can be increased while maintaining stability.
- Phase margin:
  - A feedback amplifier is stable if the phase is less than 180 at a frequency for which $|A\beta|=1$.
  - A feedback amplifier is unstable if the phase is in excess of 180 at a frequency for which | A | =1.
  - The difference between the a frequency for which | | =1 and 180 . A



Effect of phase margin on closed-loop response:

- Consider a feedback amplifier with a large low-frequency loop gain ($A_0 >> 1$).
- The closed-loop gain at low frequencies is approximately 1/ □ .
- Denoting the frequency at which | | =1 by □1: *A*□

$$A(j\omega_1)\beta = 1 \times e^{-j\theta} \text{ and } \theta = 180^\circ - \text{phase margin}$$

- The closed-loop gain at 1 peaks by a factor of 1.3 above the low-frequency gain for a phase margin of 45 .

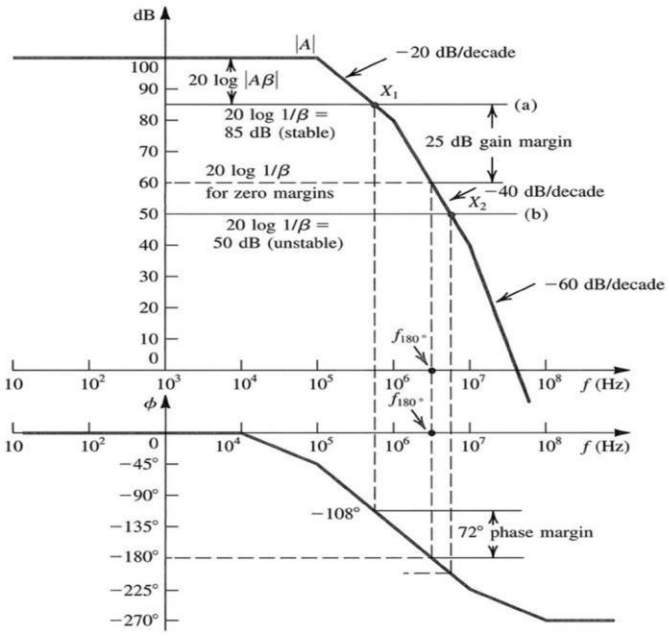
$$A_f(j\omega_1) = \frac{A(j\omega_1)}{1 + A(j\omega_1)\beta} = \frac{1}{\beta}\frac{e^{-j\theta}}{1 + e^{-j\theta}}$$

$$|A_f(j\omega_1)| = \frac{1/\beta}{|1 + e^{-j\theta}|}$$

- This peaking increase as the phase margin is reduced, eventually reaching infinite when the phase margin is zero (sustained oscillations).

An alternative approach for investigating stability

- In a Bode plot, the difference between 20 log|*A*(j □)| and 20 log(1/ □) is 20 log| *A*□ |.



$$A = \frac{10^5}{(1+jf/10^5)(1+jf/10^6)(1+jf/10^7)}$$

$$\phi = -\left[\tan^{-1}(f/10^5) + \tan^{-1}(f/10^6) + \tan^{-1}(f/10^7)\right]$$

MODULE III

OSCILLATORS AND LARGE SIGNAL AMPLIFIERS

Classification of Amplifiers

There are many forms of electronic circuits classed as amplifiers, from Operational Amplifiers and Small Signal Amplifiers up to Large Signal and Power Amplifiers. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal that is the relationship between input signal and current flowing in the load.

The type or classification of an amplifier is given in the following table.

Type of Signal	Type of Configuration	Classification	Frequency of Operation	Type of coupling	Based on the output	Number of stages
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)	a. RC coupled amplifiers	a. Voltage amplifiers	a. Single stage amplifiers
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)	b. Inductive coupled amplifiers	b. Power amplifiers	b. Two stage amplifiers
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)	c. Transformer coupled amplifiers and		c. Multistage amplifiers.
		Class C Amplifier	VHF, UHF and SHF Frequencies	d. Direct coupled amplifiers.		the number of stages,

Characteristics of amplifiers:

Amplifiers can be thought of as a simple box or block containing the amplifying device, such as a **Transistor**, **Field Effect Transistor** or **Op-amp**, which has two input terminals and two output terminals (ground being common) with the output signal being much greater than that of the input signal as it has been -Amplified.

Generally, an ideal signal amplifier has three main properties, Input Resistance or (Rin), Output Resistance or (Rout

) and of course amplification known commonly as Gain or (A). No matter how complicated an amplifier circuit is, a general amplifier model can still be used to show the relationship of these three properties.

To choose a right kind of amplifier for a purpose it is necessary to know the general characteristics of amplifiers. They are: Current gain, Voltage gain, Power gain, Input impedance, Output impedance, Bandwidth.

1. **Voltage gain:**

Voltage gain of an amplifier is the ratio of the change in output voltage to the corresponding change in the input voltage.

$A_V = \Delta V_0 / \Delta V_I$

2. **Current gain:** Current gain of an amplifier is the ratio of the change in output current to thecorresponding change in the input current

$A_I = \Delta I_0 / \Delta I_I$

3. **Power gain:** Power gain of an amplifier is the ratio of the change in output power to the corresponding change in the input power. where po and pi are the output power and input power respectively. Since power p = v × i, The power gain

$$A_P = P_O / P_I$$

$$A_P = A_V \times A_I$$

(Power amplification of the input signal takes place at the expense of the d.c. energy.)

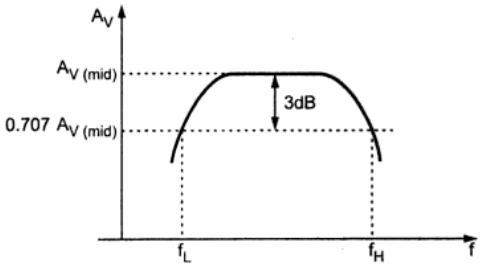
4. **Input impedance (Zi):** Input impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the input terminals and is given by the ratio of the input voltage to the input current

$$Z_I = \Delta V_I / \Delta I_I$$

5. **Output impedance (Z0):** Output impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the output terminals and is given by the ratio of the output

$$Z_O = \Delta V_O / \Delta I_O \text{ (At } V_s=0)$$

6. **Band width (BW):**The range of frequencies over which the gain (voltage gain or current gain) of an



amplifier is equal to and greater than 0.707 times the maximum gain is called the bandwidth.

In figure shown, f_L and f_H are the lower and upper cutoff frequencies where the voltage or the current gain falls to 70.7% of the maximum gain.

Bandwidth BW=(f_H- f_L).

Bandwidth is also defined as the range of frequencies over which the power gain of amplifier is equal to and greater than 50% of the maximum power gain.

The cutoff frequencies are also defined as the frequencies where the power gain falls to 50% of the maximum gain. Therefore, the cutoff frequencies are also called as Half power frequencies.

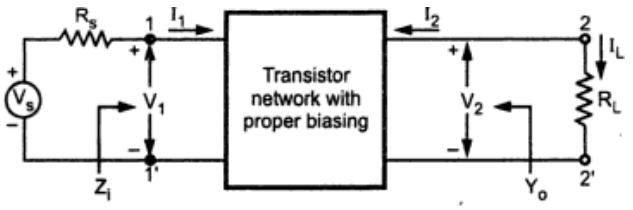
Comparison of CB, CE and CC amplifiers:

Parameters	CB	CE	CC
1. Current gain	Less than 1($\alpha \approx 1$)	High ($\beta > 1$)	Highest ($\gamma > 1$) ($\gamma = \beta + 1$)
2. Voltage gain	High	Very high	Less than 1
3. Power gain	High	Highest	>1 (low when compared to CB & CE amplifiers)
4.Input impedance	Lowest	Moderate	Highest
5.Output impedance	Highest	Moderate	Lowest
6.Phase difference	0^0 or 2π	180^0or $(2n+1)\pi$	0^0 or 2π
7. Applica-tions	Used mainly as HF amplifier	Used as a (voltage amplifier)	Used as a Buffer amplifier, impedance matching unit

HIGH FREQUENCY RESPONSE OF AMPLIFIER

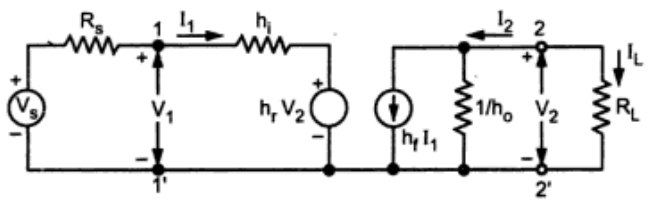
Small signal analysis of transistor amplifier

Fig shows a basic amplifier circuit. It can be noticed that to form a transistor amplifier it is necessary to connect an external load and signal source, along with proper biasing. Fig represents a transistor in any one of the three possible configurations



Basic transistor amplifier

Replacing transistor circuit with its small signal model as shown then analyzing hybrid model to find the current gain, i/p resistance, the voltage gain and the o/p resistance.



Transistor amplifier in its h-parameter model

The tabular column for parameters shown in the tabular column:

$A_i = -\frac{h_f}{1+h_o R_L}$
$A_{is} = \frac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$
$A_v = \frac{A_i R_L}{Z_i}$
$A_{vs} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$
$A_P = A_V A_i = A_i^2 \frac{R_L}{Z_i}$

The above formulae is applicable to all the configurations. An appropriate subscript to h-parameters corresponding to configuration must be added for the expressions.

Table below shows the typical values of h-parameters for 3 configurations at room temperature

Parameter	CE	CC	CB
$h_{11} = h_i$	1100 Ω	1100 Ω	21.6 Ω
$h_{12} = h_r$	2.5×10^{-4}	~ 1	2.9×10^{-4}
$h_{21} = h_f$	50	– 51	– 0.98
$h_{22} = h_o$	25 μA/V	25 μA/V	0.49 μA/V

Procedure for the analysis of transistor amplifier circuit

1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace dc source by a short circuit. In other words, short V_{CC} and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

Converting from one configuration to another configuration

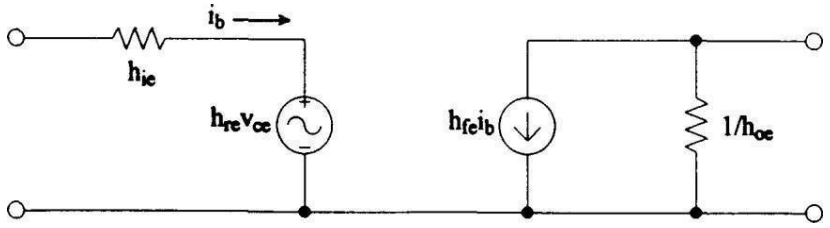
Most of the times h-parameters are specified in CE configuration, therefore for analyzing of CC & CB configurations it is require to first convert the given h-parameters for CE configuration into the required configuration by using conversion formulae as given the table below.

Symbol	Common emitter	Common collector	Common base	T equivalent circuit
h_{ie}	1,100 Ω	h_{ic} *	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{re}	25×10^{-4}	$1 - h_{rc}$ *	$\frac{h_{ib}\,h_{ob}}{1+h_{fb}} - h_{rb}$	$\frac{r_b}{(1-a)\,r_c}$
h_{fe}	50	$-(1+h_{fc})$ *	$-\frac{h_{fb}}{1+h_{fb}}$	$\frac{a}{1-a}$
h_{oe}	25 μA/V	h_{oc} *	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a)\,r_c}$
h_{ib}	$\frac{h_{ie}}{1+h_{fe}}$	$-\frac{h_{ic}}{h_{fe}}$	21.6 Ω	$r_e + (1-a)\,r_b$
h_{rb}	$\frac{h_{ie}\,h_{oe}}{1+h_{fe}} - h_{re}$	$h_{fc} - \frac{h_{ic}\,h_{oc}}{h_{fc}} - 1$	29×10^{-4}	$\frac{r_b}{r_c}$
h_{fb}	$-\frac{h_{fe}}{1+h_{fe}}$	$-\frac{1+h_{fc}}{h_{fc}}$	− 0.98	− a
h_{ob}	$\frac{h_{oe}}{1+h_{fe}}$	$-\frac{h_{oc}}{h_{fc}}$	0.49 μA/V	$\frac{1}{r_c}$
h_{ic}	h_{ie} *	1,100 Ω	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{rc}	$1 - h_{re} \approx 1$ *	1	1	$1 - \frac{r_e}{(1-a)\,r_c}$
h_{fc}	$-(1+h_{fe})$ *	− 51	$-\frac{1}{1+h_{fb}}$	$-\frac{1}{1-a}$
h_{oc}	h_{oe} *	25 μA/V	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a)\,r_c}$
a	$\frac{h_{fe}}{1+h_{fe}}$	$\frac{1+h_{fc}}{h_{fc}}$	$-h_{fb}$	0.980
r_c	$\frac{1+h_{fe}}{h_{oe}}$ *	$-\frac{h_{fc}}{h_{oc}}$ *	$\frac{1}{h_{ob}}$	2.04 M
r_e	$\frac{h_{re}}{h_{oe}}$ *	$\frac{1-h_{rc}}{h_{oc}}$ *	$h_{ib} + \frac{h_{rb}}{h_{ob}}(1+h_{fb})$ *	10 Ω
r_b	$h_{ic} + \frac{h_{re}}{h_{oe}}(1+h_{fe})$ *	$h_{ic} + \frac{h_{fc}}{h_{oc}}(1+h_{rc})$ *	$\frac{h_{rb}}{h_{ob}}$ *	590 Ω

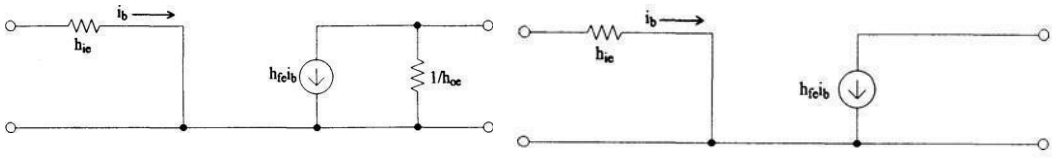
h-parameter conversion table

Simplified analysis of CE Configuration

The hybrid parameter equivalent circuit of a common-emitter transistor is shown in Fig.



The approximation $h_{re} \approx 0$ is sometimes utilized which yields a 3-parameter model shown in Figure The two approximations of $h_{re} \approx 0$ and $h_{oe} \approx 0$ are frequently utilized and result in the common 2-parameter model shown in Fig.

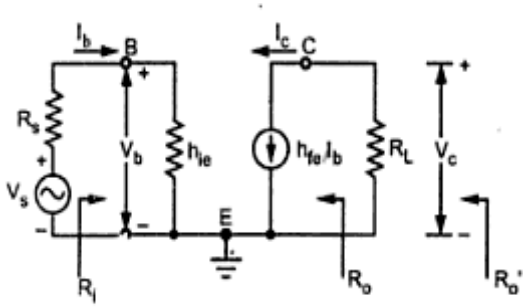


The values of h_{ie} , h_{fe}. h_{re} h_{oe} for a specifci bipolar junction transistor are typically found in the manufacturer‘s small- signal specifications. The values can also bedetermined fromthe **common-emitter** output characteristic curves.

Utilizing a single transistor model itis possible to analyze common-emitter, common-base, or common-collector amplifier circuits.

Approximate Hybrid Analysis for CE Transistor Amplifier

The *h*-parameter formulas (*CE* configuration) can be approximated to a form that is easier to handle. While these approximate formulas will not give results that are as accurate as the original formulas, they can be used for many applications. The CE approximate model is as shown in fig.



Approximate CE model

(i) Input impedance

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

In actual practice, the second termin this expression is very small as compared to the first term.

$$Z_{in} = h_{ie}$$

… approximate formula

(ii) Current gain:

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

In actual practice, $h_{oe}\, r_L$ is very small as compared to 1.

$$A_i = h_{fe}$$

… approximate formula

(iii) Voltage gain:

$$\text{Voltage gain, } A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

$$= \frac{-h_{fe}\, r_L}{Z_{in}\,(h_{oe}\, r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\, r_L$ is very small as compared to 1.

$$A_v = -\frac{h_{fe}\, r_L}{h_{ie}}$$

... approximate formula

(iv) Output impedance:

Output impedance of transistor

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie}}}$$

The second term in the denominator is very small as comparedto h_{oe}. $Z_{out} = \frac{1}{h_{oe}}$ ...approximate formula

The output impedance of transistor amplifier

$= Z_{out} \| r_L$ where $^* r_L = R_C \| R_L$

If the amplifier is unloaded (*i.e.* $RL = \infty$), $rL = RC$.

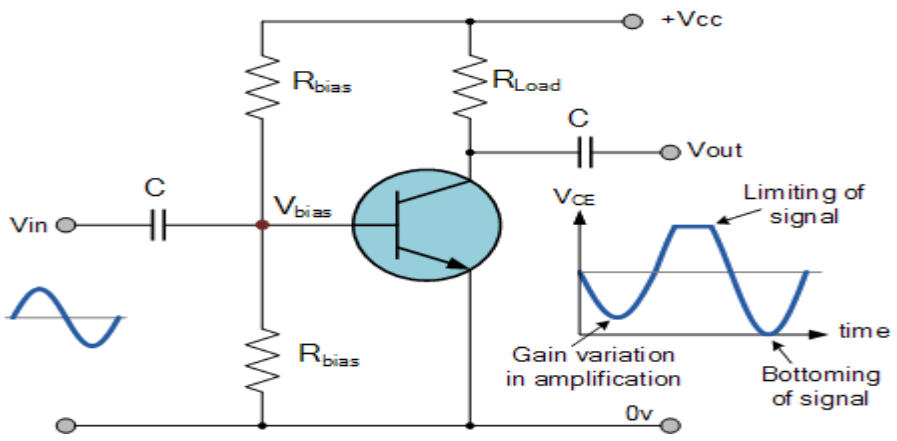
Approximate Hybrid Analysis for CC Transistor Amplifier

Amplifier Distortion

From the previous tutorials we that for a signal amplifier to operate correctly without any distortion to the output signal, it requires some form of DC Bias on its Base or Gate terminal so that it can amplify the input signal over its entire cycle with the bias ―Q-point‖ set as near to the middle of the load line as possible. This then gave us a ―Class- A‖ type amplification configuration with the most common arrangement being the ―Common Emitter‖ for Bipolar transistors and the ―Common Source‖ for unipolar FET transistors.

We also learnt that the Power, Voltage or Current Gain, (amplification) provided by the amplifier is the ratio of the peak output value to its peak input value (Output ÷ Input). However, if we incorrectly design our amplifier circuit and set the biasing Q-point at the wrong position on the load line or apply too large an input signal to the amplifier, the resultant output signal may not be an exact reproduction of the original input signal waveform. In other words the amplifier will suffer from what is commonly called **Amplifier Distortion**. Consider the Common Emitter Amplifiercircuit below.

Common Emitter Amplifier



Distortion of the output signal waveform may occur because:

- **1.** Amplification may not be taking place over the whole signal cycle due to incorrect biasing levels.

- **2.** The input signal may be too large, causing the amplifiers transistors to be limited by the supplyvoltage.
- **3.** The amplification may not be a linear signal over the entire frequency range of inputs.

This means then that during the amplification process of the signal waveform, some form of**Amplifier Distortion** has occurred.

Amplifiers are basically designed to amplify small voltage input signals into much larger output signals and this means that the output signal is constantly changing by some factor or value, called gain, multiplied

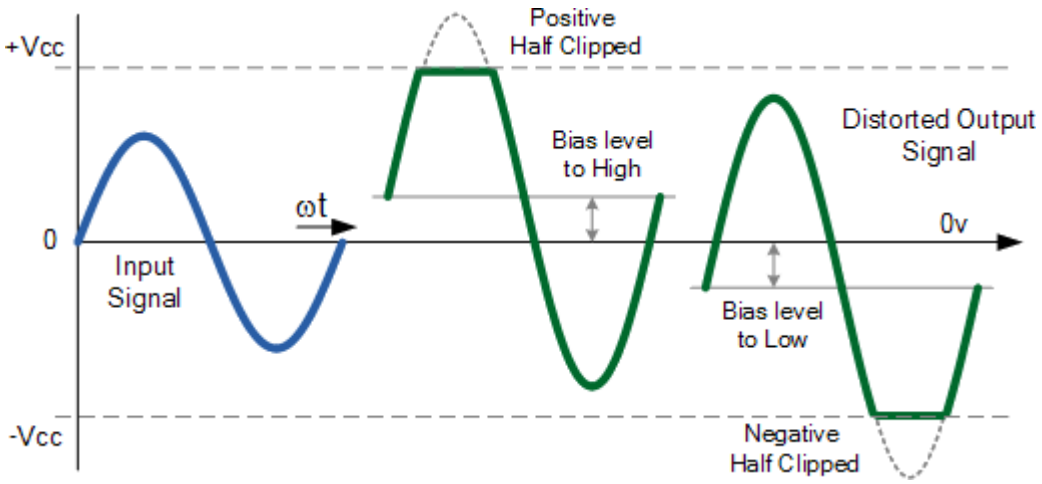
by the input signal for all input frequencies. We saw previously that this multiplication factor is called the Beta, β value of the transistor.

Common emitter or even common source type transistor circuits work fine for small AC input signals but suffer from one major disadvantage, the calculated position of the bias Q-point of a bipolar amplifier depends on the same Beta value for all transistors. However, this Beta value will vary from transistors of the same type, in other words, the Q-point for one transistor is not necessarily the same as the Q-point for another transistor of the same type due to the inherent manufacturing tolerances.

Then amplifier distortion occurs because the amplifier is not linear and a type of amplifier distortion called **Amplitude Distortion** will result. Careful choice of the transistor and biasing components can help minimise the effect of amplifier distortion.

Amplitude Distortion Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. This non-linearity of the output waveform is shown below.

Amplitude Distortion due to Incorrect Biasing

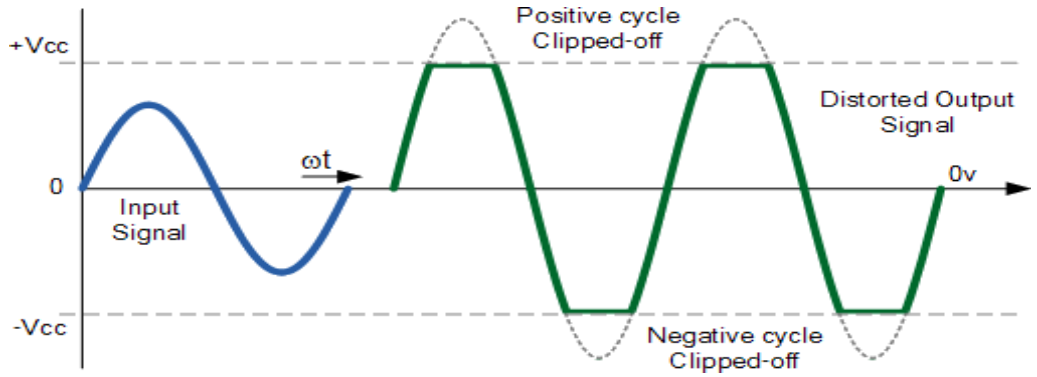


If the transistors biasing point is correct, the output waveform should have the same shape as that of the input waveform onl y bigger, (amplified). If there is insufficient bias and the Q-point lies in the lower half of the load line, then the output waveform will look like the one on the right with the negative half of the output waveform ‑cut-off‖ or clipped. Likewise, if there is too much bias and the Q-point lies in the upper half of the load line, then the output waveform will look like the one on the left with the positive half ‑cut-off‖ or clipped.

Also, when the bias voltage is set too small, during the negative half of the cycle the transistor does not fully conduct so the output is set by the supply voltage. When the bias is too great the positive half of the cycle saturates the transistor and the output drops almost to zero.

Even with the correct biasing voltage level set, it is still possible for the output waveform to become distorted due to a la rge input signal being amplified by the circuits gain. The output voltage signal becomes clipped in both the positive and negative parts of the waveform an no longer resembles a sine wave, even when the bias is correct. This type of amplitude distortion is called **Clipping** and is the result of ‑over-driving‖ the input of the amplifier.

When the input amplitude becomes too large, the clipping becomes substantial and forces the output waveform signal to exceed the power supply voltage rails with the peak (+ve half) and the trough (-ve half) parts of the waveform signal becoming flattened or ‑Clipped-off‖. To avoid this the maximum value of the input signal must be limited to a level that will prevent this clipping effect as shown above.



Amplitude Distortion due to Clipping

Amplitude Distortion greatly reduces the efficiency of an amplifier circuit. These ‑flat tops‖ of the distorted output waveform either due to incorrect biasing or over driving the input do not contribute anything to the strength of the output signal at the desired frequency.

Having said all that, some well known guitarist and rock bands actually prefer that their distinctive sound is highly distorted or

‑overdriven‖ by heavily clipping the output waveform to both the +ve and -ve power supply rails. Also, increasing the amounts of clipping on a sinusoid will produce so much amplifier distortion that it will eventually produce an output waveform which resembles that of a ‑square wave‖ shape which can then be used in electronic or digital synthesizer circuits.

We have seen that with a DC signal the level of gain of the amplifier can vary with signal amplitude, but as well as Amplitude

Distortion, other types of amplifier distortion can occur with AC signals in amplifier circuits, such as **Frequency Distortion** and **Phase Distortion**.

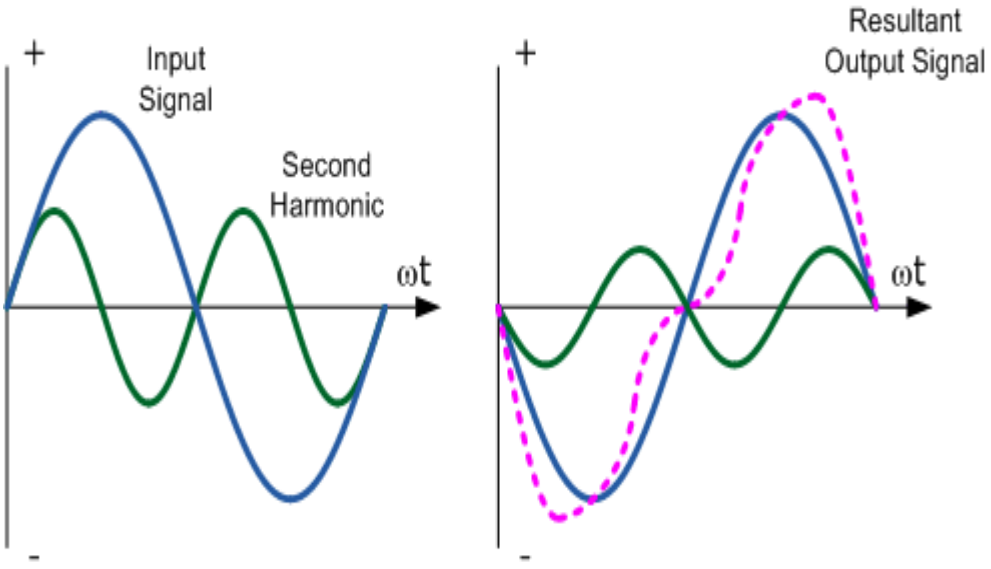
Frequency Distortion

Frequency Distortion is another type of amplifier distortion which occurs in a transistor amplifier when the level of amplification varies with frequency. Many of the input signals that a practical amplifier will amplify consist of the required signal waveform called the -Fundamental Frequency plus a number of different frequencies called

-Harmonics superimposed onto it.

Normally, the amplitude of these harmonics are a fraction of the fundamental amplitude and therefore have very little or no effect on the output waveform. However, the output waveform can become distorted if these harmonic frequencies increase in amplitude with regards to the fundamental frequency. For example, consider the waveform below:

Frequency Distortiondueto Harmonics



In the example above, the input waveform consists a the fundamental frequency plus a second harmonic signal. The resultant output waveform is shown on the right hand side. The frequency distortion occurs when the fundamental frequency combines with the second harmonic to distort the output signal. Harmonics are therefore multiples of the fundamental frequency and in our simple example a second harmonic was used.

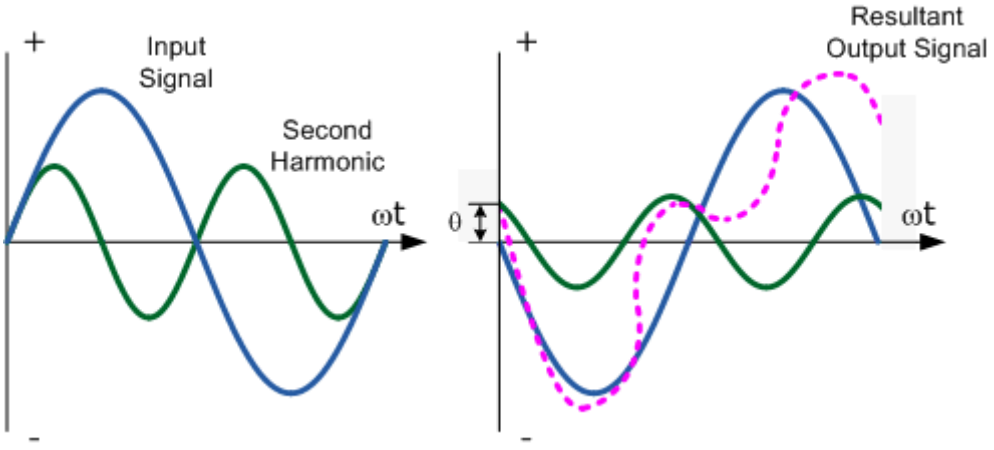
Therefore, the frequency of the harmonic is twice the fundamental, 2 x f or $2f$. Then a third harmonic would be $3f$, a fourth, $4f$, and so on. Frequency distortion due to harmonics is always a possibility in amplifier circuits containing reactive elements such as capacitance or inductance.

Phase Distortion

Phase Distortion or **Delay Distortion** is a type of amplifier distortion which occurs in a non-linear transistor amplifier when there is a time delay between the input signal and its appearance at the output.

If we say that the phase change between the input and the output is zero at the fundamental frequency, the resultant phase angle delay will be the difference between the harmonic and the fundamental. This time delay will depend on the construction of the amplifier and will increase progressively with frequency within the bandwidth of the amplifier. For example, consider the waveform below:

Phase Distortion due to Delay



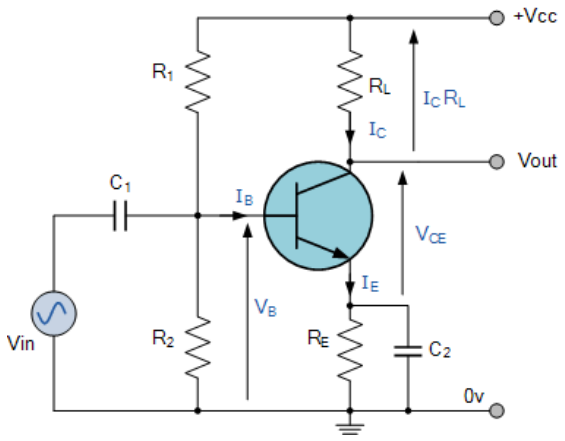
Other than high end audio amplifiers, most Practical Amplifiers will have some form of **Amplifier Distortion** being a combination of both -Frequency Distortion- and -Phase Distortion-, together with amplitude distortion. In most applications such as in audio amplifiers or power amplifiers, unless the amplifiers distortion is excessive or severe it will not generall y affect the operation or output sound of the amplifier.

In the next tutorial about Amplifiers we will look at the **Class A Amplifier**. Class A amplifiers are the most common type of amplifier output stage making them ideal for use in audio power amplifiers.

Amplifiers Tutorial Summary

Amplifiers are used extensively in electronic circuits to make an electronic signal bigger without affecting it in any other way. Generally we think of *Amplifiers* as audio amplifiers in the radios, CD players and stereo's we use around the home. In this amplifier tutorial section we looked at the amplifier which is based on a single bipolar transistor as shown below, but there are several different kinds of transistor amplifier circuits that we could use.

Typical Single Stage Amplifier Circuit



Small Signal Amplifiers

- Small Signal Amplifiers are also known as **Voltage Amplifiers**.

- Voltage Amplifiers have 3 main properties, **Input Resistance**, **Output Resistance** and **Gain**.

- The Gain of a small signal amplifier is the amount by which the amplifier -Amplifies| the input signal.
- Gain is a ratio of input divided by output, therefore it has no MODULEs but is given the symbol (A) with the most common types of transistor gain being, **Voltage Gain (Av), Current Gain (Ai)**and **Power Gain(Ap)**

The power Gain of the amplifier can also be expressed in Decibels or simply dB.

In order to amplify all of the input signal distortion free in a Class A type amplifier, DC Base Biasing is required.

DC Bias sets the Q-point of the amplifier half way along the loadline.

This DC Base biasing means that the amplifier consumes power even if there is no input signalpresent.

The transistor amplifier is non-linear and an incorrect bias setting will produce large amounts of distortion to the output waveform.

Too large an input signal will produce large amounts of distortion due to clipping, which is also a form of amplitude distortion.

Incorrect positioning of the Q-point on the load line will produce either Saturation **Clippingor Cut-off Clipping.**

The Common Emitter Amplifier configuration is the most common form of all the general purpose voltage

amplifier circuit using a Bipolar Junction Transistor.

The Common Source Amplifier configuration is the most common form of all the general purpose voltage amplifier circuit using a Junction Field Effect Transistor.

Simplified common emitter hybrid model:

1.3 Common Emitter Amplifier

Common Emitter Circuit is as shown in the Fig. 1.2. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an AC analysis.

$$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0} \qquad h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0}$$

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \qquad h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0}$$

The typical values of the *h-parameter* for a transistor in Common Emitter Configuration are,

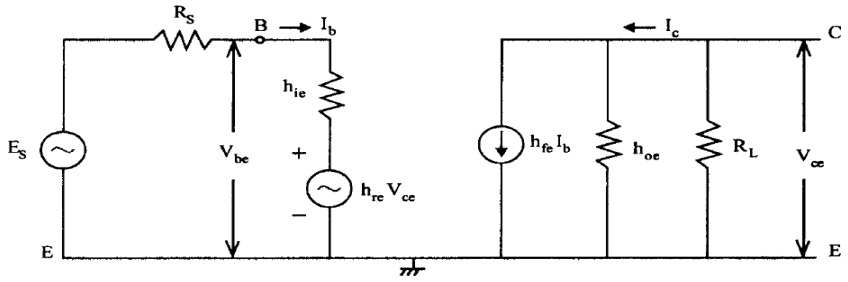


Fig. 1.3 h-parameter Equivalent Circuit Since,

V be is a fraction of volt O.2V, Ib in ~A, 1 00 ~A and so on. 0.2V h· = =4KO

Ie 50xlO-6

Single Stage Amplifiers

hfe == Ic/Ib :: 100.

Ie is in rnA and Is in 1lA. hfe » 1:: P

hre == 0.2 x 10-3. Because, it is the *Reverse* Voltage Gain. and Vbe

hre = Vee Vee> Vbe;

Input

h = -'"---

re Output

Output is » input, because amplification takes place. Therefore hre « 1. ho e= 8 Il 7v0;: and ho e == ~ . Vee

1.3.1 Input Resistance of the Amplifier Circuit (Ri)

In most practical cases it is appropriate to obtain approximate values of A_V , A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 4** shows the CE amplifier equivalent circuit in terms of h-parameters Since $1 / h_{oe}$ in parallel with R_L is approximately equal to R_L if $1 / h_{oe} >> R_L$ then h_{oe} may be neglected. Under these conditions.

$I_c = h_{fe} I_B$.

$h_{re} v_C = h_{re} I_C R_L = h_{re} h_{fe} I_b R_L$.

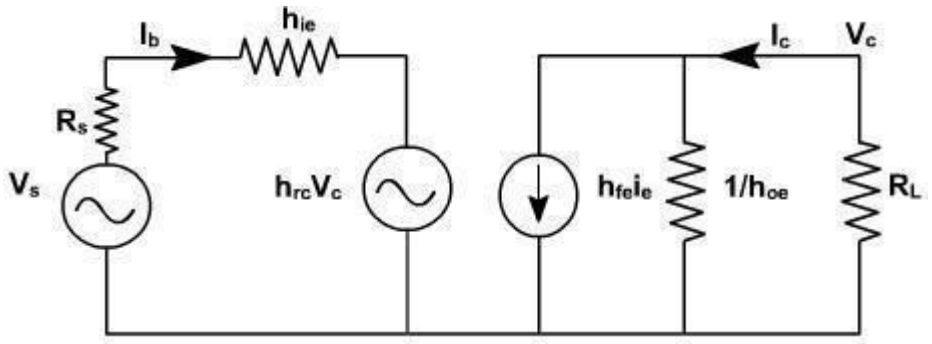


Fig. 4

Since $h_{fe}.h_{re}0.01$, this voltage may be neglected in comparison with $h_{ic} I_b$ drop across h_{ie} provided R_L is not very large. If load resistance R_L is small than hoe and h_{re} can beneglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedence seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon R_S and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe}. This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_V of each stage, it should be independent of h_{fe}. A simple and effective way is to connect an emitter resistor R_e as shown in **fig. 5**. The resistor provides negative feedback and provide stabilization.

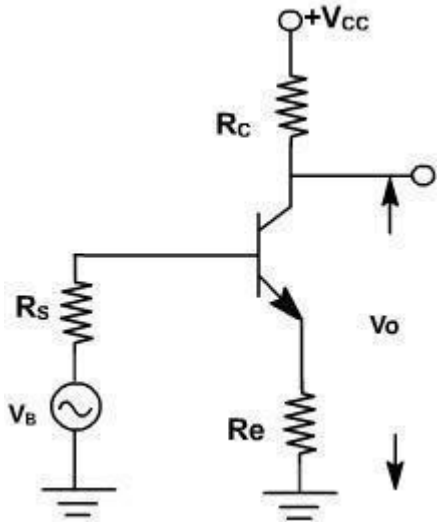


Fig. 5

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$$
$$= -h_{fe}$$

It is unaffected by the addition of R_C.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$
$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$
$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe})R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

An approximate analysis of the circuit can be made using the simplified model.

Subject to above approximation A_V is completely stable. The output resistance is infinite for the approximate model.

Common Emitter Amplifier Example No1

A common emitter amplifier circuit has a load resistance, R_L of 1.2kΩs and a supply voltage of 12v. Calculate the maximum Collector current (Ic) flowing through the load resistor when the transistor is switched fully -ON| (saturation), assume Vce = 0. Also find the value of the Emitter resistor, $R_E$with a voltage drop of 1v across it. Calculate the values of all the other circuit resistors assuming an NPN silicon transistor.

This then establishes point -A| on the Collector current vertical axis of the characteristics curves and occurs when Vce =

0. When the transistor is switched fully -OFF|, their is no voltage drop across either resistor R_E or R_L as no current is flowing through them. Then the voltage drop across the transistor, Vce is equal to the supply voltage, Vcc. This establishes point -B| on the horizontal axis of the characteristics curves.

Generally, the quiescent Q-point of the amplifier is with zero input signal applied to the Base, so the Collector sits half-way along the load line between zero volts and the supply voltage, (Vcc/2). Therefore, the Collector current at the Q-point of the amplifier will be given as:

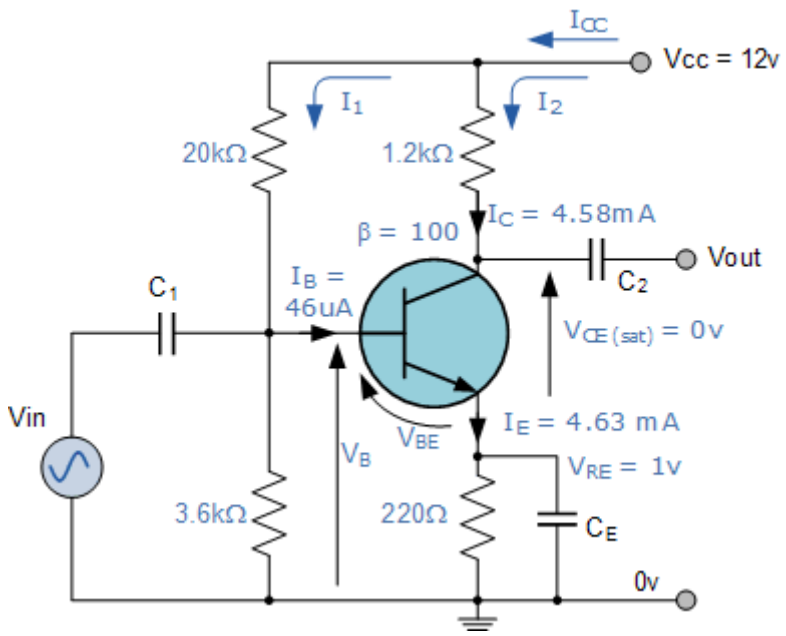
This static DC load line produces a straight line equation whose slope is given as: $-1/(R_L + R_E)$ and that it crosses the vertical Ic axis at a point equal to $Vcc/(R_L + R_E)$. The actual position of the Q-point on the DC load line is determined by the mean value of Ib.

As the Collector current, Ic of the transistor is also equal to the DC gain of the transistor (Beta), times the Base current (β x Ib), if we assume a Beta (β) value for the transistor of say 100, (one hundred is a reasonable average value for low power signal transistors) the Base current Ib flowing into the transistor will be given as:

Instead of using a separate Base bias supply, it is usual to provide the Base Bias Voltage from the main supply rail (Vcc) through a dropping resistor, R1. Resistors, R1 and R2 can now be chosen to give a suitable quiescent Base current of 45.8μA or 46μA rounded off. The current flowing through the potential divider circuit has to be large compared to the actual Base current, Ib, so that the voltage divider network is not loaded by the Base current flow.

A general rule of thumb is a value of at least 10 times Ib flowing through the resistor R2. Transistor Base/Emitter voltage, Vbe is fixed at 0.7V (silicon transistor) then this gives the value of R2 as:

If the current flowing through resistor R2 is 10 times the value of the Base current, then the current flowing through resistor R1 in the divider network must be 11 times the value of the Base current. The



Coupling Capacitors

In **Common Emitter Amplifier** circuits, capacitors C1 and C2 are used as **Coupling Capacitors** to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not effected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit.

This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only R_L plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

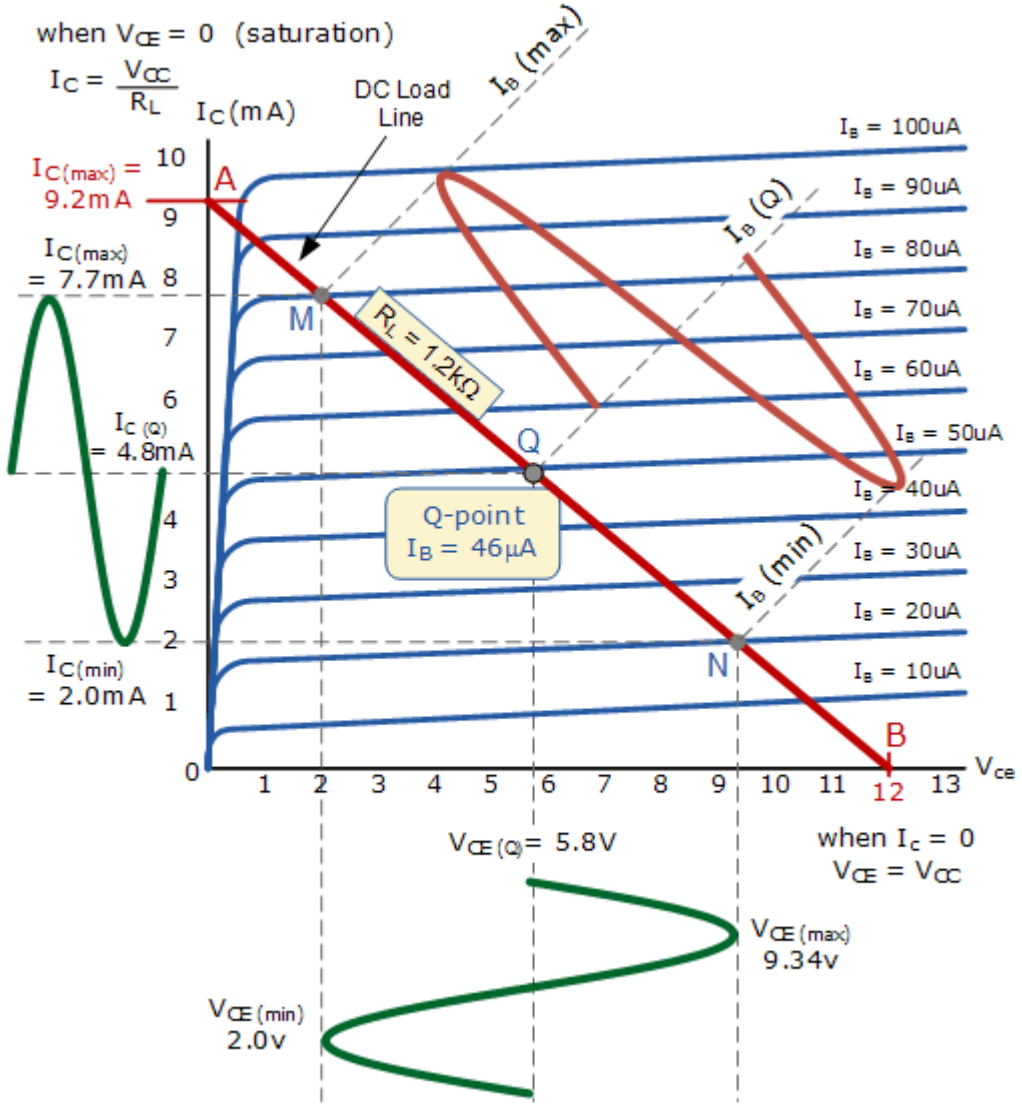
Output Characteristics Curves

Ok, so far so good. We can now construct a series of curves that show the Collector current, Icagainst the Collector/Emitter voltage, Vce with different values of Base current, Ib for our simple common emitter amplifier circuit. These curves are known as the -Output Characteristic Curves| and are used to show how the transistor will operate over its dynamic range. A static or DC load line is drawn onto the curves for the load resistor RL of 1.2kΩ to show all the transistors possible operating points.

When the transistor is switched -OFF|, Vce equals the supply voltage Vcc and this is point B on the line. Likewise when the transistor is fully -ON| and saturated the Collector current is determined by the load resistor, RL and this is point A on the line.

We calculated before from the DC gain of the transistor that the Base current required for the mean position of the transistor was 45.8µA and this is marked as point Q on the load line which represents the **Quiescent point** or **Q- point** of the amplifier. We could quite easily make life easy for ourselves and round off this value to 50µA exactly, without any effect to the operating point.

Output Characteristics Curves



Point Q on the load line gives us the Base current Q-point of Ib = 45.8µA or 46µA. We need to find the maximum and minimum peak swings of Base current that will result in a proportional change to the Collector current, Ic without any distortion to the output signal.

As the load line cuts through the different Base current values on the DC characteristics curves we can find the peak swings of Base current that are equally spaced along the load line. These values are marked as

points N and M on the line, giving a minimum and a maximum Base current of 20μAand 80μA respectively.

These points, N and M can be anywhere along the load line that we choose as long as they are equally spaced from Q. This then gives us a theoretical maximum input signal to the Base terminal of 60μA peak-to-peak, (30μA peak) without producing any distortion to the output signal.

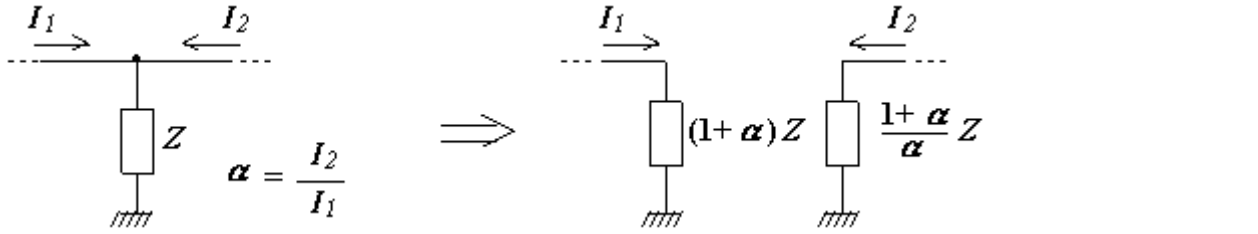
Any input signal giving a Base current greater than this value will drive the transistor to go beyond point N and into its ‑cut-off| region or beyond point M and into its Saturation region thereby resulting in distortion to the output signal in the form of

‑clipping|.

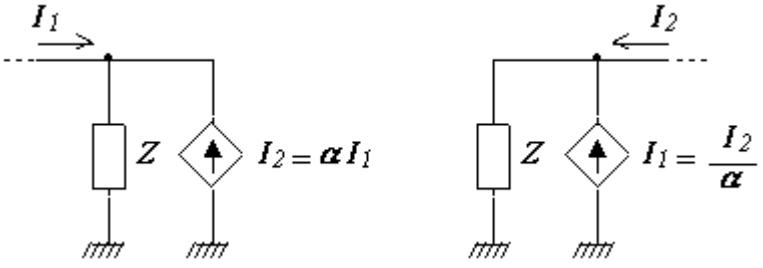
Using points N and M as an example, the instantaneous values of Collector current and corresponding values of Collector- emitter voltage can be projected from the load line. It can be seen that the Collector-emitter voltage is in anti-phase (-180^{o}) with the collector current.

As the Base current Ib changes in a positive direction from 50μA to80μA, the Collector-emitter voltage, which is also the output voltage decreases from its steady state value of 5.8v to 2.0v.

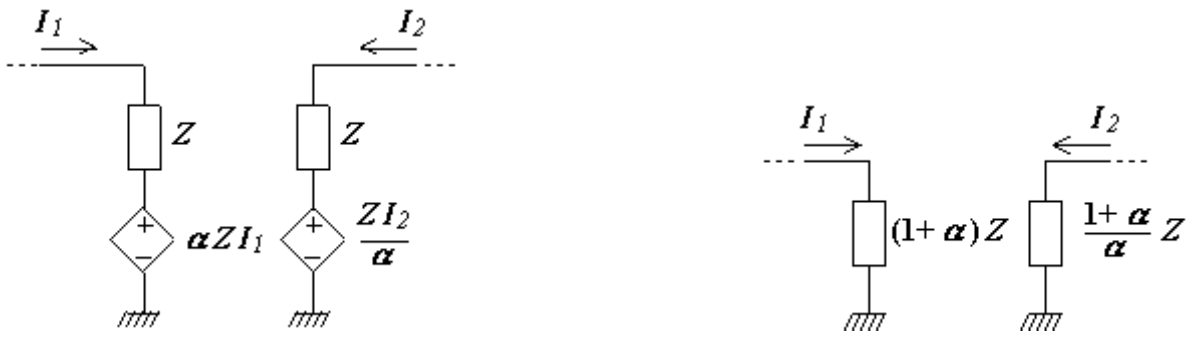
Then a single stage **Common Emitter Amplifier** is also an ‑Inverting Amplifier| as an increase in Base voltage causes a decrease in Vout and a decrease in Base voltage produces an increase in Vout. In other words the output signal is 180^{o} out-of- phase with the input signal.



In fact, replacing the two-port network by its equivalent, as in the figure,



it results the circuit on the left in the next figure and then, applying the source absorption theorem, the circuit on the right.



Multistage Transistor Amplifiers

T he output from a single stage amplifier is usually insufficient to drive an output device.

Inther words, the gain of a single amplifier is inadequate for practical purposes. Consequently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is *coupled* in some way to the input of the next stage. The resulting

system is referred to as multistage amplifier. It may be emphasised here that a practical amplifier is always a multistage amplifier. For example, in a transistor radio receiver, the number of amplification stages may be six or more. In this chapter, we shall focus our attention on the various multistage transistor amplifiers and their practical applications.

11.1 Multistage Transistor Amplifier

A transistor circuit containing more than one stage of amplification is known as **multistage transistor amplifier.**

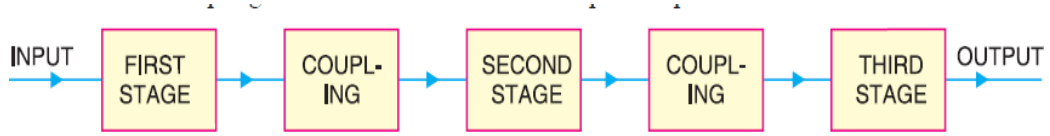
In a multistage amplifier, a number of single amplifiers are connected in **cascade arrangement*

i.e. output of first stage is connected to the input of the second stage through a suitable *coupling device* and so on. The purpose of coupling device (*e.g.* a capacitor, transformer etc.) is (*i*) to transfer

a.c. output of one stage to the input of the next stage and (*ii*) to isolate the d.c. conditions of one stage from the next stage.

Fig. 11.1 shows the block diagram of a 3-stage amplifier. Each stage consists of

one transistor and associated circuitry and is coupled to the next stage through a coupling device. The name of the amplifier is usually given after the type of coupling used. *e.g.*



Hence, it almost remains constant.

The cascode amplifier is combined common-emitter and common-base. This is an AC circuit equivalent with batteries and capacitors replaced by short circuits.

The key to understanding the wide bandwidth of the cascode configuration is the *Miller effect*. The Miller effect is the multiplication of the bandwidth robbing collector-base capacitance by voltage gain A_v. This C-B capacitance is

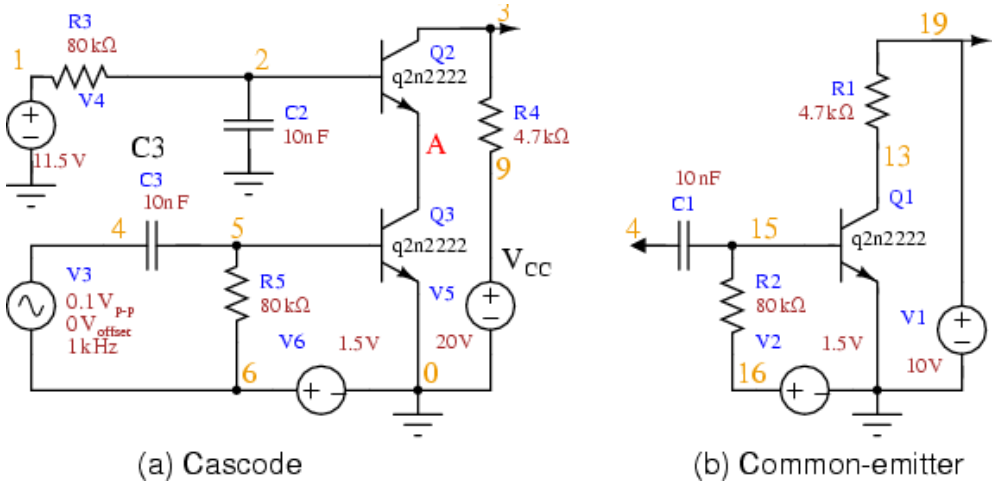
smaller than the E-B capacitance. Thus, one would think that the C-B capacitance would have little effect. However, in the C-E configuration, the collector output signal is out of phase with the input at the base. The collector signal capacitively coupled back opposes the base signal. Moreover, the collector feedback is $(1-A_v)$ times larger than the base signal. Keep in mind that A_v is a negative number for the inverting C-E amplifier. Thus, the small C-B capacitance appears $(1+A|_v|)$ times larger than its actual value. This capacitive gain reducing feedback increases with frequency, reducing the high frequency response of a C-E amplifier.

The approximate voltage gain of the C-E amplifier in Figure below is $-R_L/r_{EE}$. The emitter current is set to 1.0 mA by biasing. R_{EE}= 26mV/I_E = 26mV/1.0ma = 26 Ω. Thus, $A_v = -R_L/R_{EE}$ = -4700/26 = -181. The pn2222 datasheet list C_{cbo} = 8 pF.[FAR] The miller capacitance is $C_{cbo}(1-A_v)$. Gain A_v = -181, negative since it is inverting gain. $C_{miller} = C_{cbo}(1-A_v)$ = 8pF(1-(-181)=1456pF

A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. To have a moderately high input impedance, the C-E stage is still desirable. The key is to reduce the gain (to about 1) of the C- E stage which reduces the Miller effect C-B feedback to $1 \cdot C_{CBO}$. The total C-B feedback is the feedback capacitance $1 \cdot C_{CB}$ plus the actual capacitance C_{CB} for a total of $2 \cdot C_{CBO}$. This is a considerable reduction from $181 \cdot C_{CBO}$. The miller capacitance for a gain of -2 C-E stage is $C_{miller} = C_{cbo}(1-A_v) = C_{miller} = C_{cbo}(1-(-1)) = C_{cbo} \cdot 2$.

The way to reduce the common-emitter gain is to reduce the load resistance. The gain of a C-E amplifier is approximately R_C/R_E. The internal emitter resistance r_{EE} at 1mA emitter current is 26Ω. For details on the 26Ω, see

-Derivation of R_{EE}|, see REE. The collector load R_C is the resistance of the emitter of the C-B stage loading the C-E stage, 26Ω again. CE gain amplifier gain is approximately $A_v = R_C/R_E$=26/26=1. This Miller capacitance is $C_{miller} = C_{cbo}(1-A_v)$ = 8pF(1-(- 1)=16pF. We now have a moderately high input impedance C-E stage without suffering the Miller effect, but no C-E dB voltage gain. The C-B stage provides a high voltage gain, A_V = -181. Current gain of cascode is β of the C-E stage, 1 for the C- B, β overall. Thus, the cascode has moderately high input impedance of the C-E, good gain, and good bandwidth of the C-B.



SPICE: Cascode and common-emitter for comparison.

The SPICE version of both a cascode amplifier, and for comparison, a common-emitter amplifier is shown in Figure above. The netlist is in Table below. The AC source V3 drives both amplifiers via node 4. The bias resistors for this circuit are calculated in an example problem cascode.

Frequency response of RC coupled amplifier: The frequency response of a typical RC coupled amplifiers is shown in the fig. It is clear from the graph that the voltage gain drops off at low frequencies and high frequencies.

While it remains constant in the mid frequency range. This behavior of the amplifier is explained as follows;

At low frequencies: The coupling capacitors CC offer a high reactance. Hence it will allow only a part of the signal to pass from one stage to the next stage. In addition to this, the emitter bypass capacitor CE cannot shunt the emitter resistor RE effectively, because of its large reactance at low frequencies. Due to these reasons, the gain of the amplifier drops at low frequencies.

At high frequencies: The coupling capacitor CC offers a low reactance and it acts as a short circuit. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Moreover, at high frequencies, capacitive reactance of base emitter junction is low which increases the base current. This in turn reduces the current amplification factor β. As a result of these two factors, gain drops at high frequencies.

At mid frequency: In the mid frequency range, the effect of coupling capacitor is such that it maintains a constant gain. Thus, as the frequency increases, the reactance of capacitor CC decreases, which tends to increase the gain. However, at the same time, lower capacitive reactance increases the loading effect of first stage to which the gain reduces. These two factors cancel each other. Thus the constant gain is maintained.

Advantages of RC coupled amplifiers:

it requires components like resistors and capacitors. Hence, it is small, light and inexpensive. **Amax** 2max*A* **f1 f2 f (Hz) Band Width Gain 3dB LF HFMF** Transistor Amplifiers Page 19 of 23

It has a wide frequency response. The gain is constant over audio frequency range which is the region of most importance for

speech and music.

It provides less frequency distortion.

Its overall amplification is higher than that of other coupling combinations.

Disadvantages of RC coupled amplifiers:

The overall gain of the amplifier is comparatively small because of the loading effect.

RC coupled amplifiers have tendency to become noisy with age, especially in moist climate.

The impedance matching is poor as the output impedance is several hundred ohms, where as that of a speaker is only few ohms. Hence, small amount of power will be transferred to the speaker.

Applications:

RC coupled amplifiers have excellent audio frequency fidelity over a wide range of frequency i.e, they are widely used as voltage amplifiers. This property makes it very useful in the initial stages of public address system. However, it may be noted that a coupled amplifier cannot be used as a final stage of the amplifier because of its poor impedance matching.

Direct coupled amplifier :

The circuit diagram of direct coupling using two identical transistors is shown in the fig. In this method, the ac output signal is fed directly to the next stage. This type of coupling is used where low frequency signals are to be amplified. The coupling devices such as capacitors, inductors and transformers cannot be used at

low frequencies because there size becomes very large. The amplifiers using this coupling are called direct coupled amplifiers or dc amplifiers.

Advantages Fig . Two stage Direct coupled amplifier R1 RC *v*s is iB ic +VCCR1RC*v*o2 ic *v*o1 Page 20 of 23 The circuit arrangement is simple because of minimum number of components.

The circuit can amplify even very low frequency signals as well as direct current signals. No bypass and coupling capacitors

are required.

Disadvantages

1. It cannot be used for amplifying high frequencies.
2. The operating point is shifted due to temperature variations.

Applications : Direct coupled amplifiers find applications in regulator circuits of electronic power supplies, differential amplifiers,pulseamplifiers,electronic instrument.

INTRODUCTION

Feedback Amplifiers

A practical amplifier has a gain of nearly one million *i.e.* its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce *hum* due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of *negative feedback i.e.* by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Ideally an amplifier should reproduce the input signal, with change in magnitude and with or without change in phase. But some of the short comings of the amplifier circuit are

Change in the value of the gain due to variation in supplying voltage, temperature or due to components.

Distortion in wave-form due to non linearities in the operating characters of the Amplifying device.

The amplifier may introduce noise (undesired signals)

The above drawbacks can be minimizing if we introduce feedback CLASSIFICATION OF AMPLIFIERS

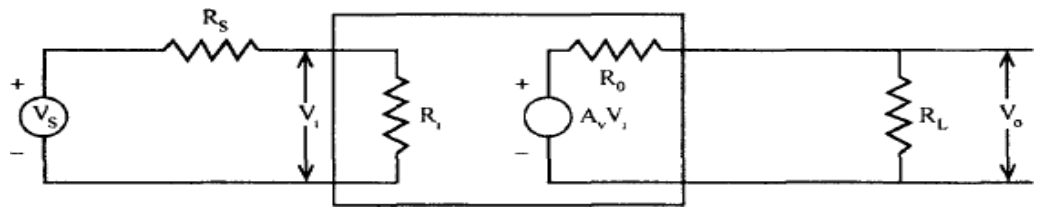
Amplifiers can be classified broadly as,

I. Voltage amplifiers.
2. Current amplifiers.
3. Transconductance amplifiers.
4. Transresistance amplifiers.

This classification is with respect to the input and output impedances relative to the load and source impedances.

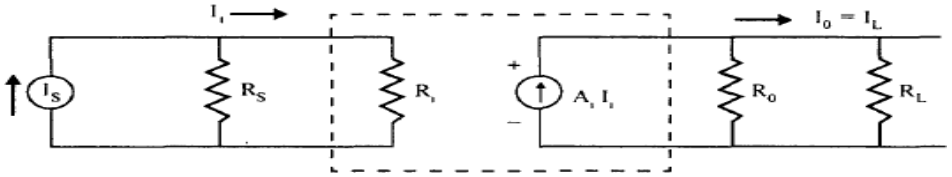
VOLTAGE AMPLIFIER

This circuit is a 2-port network and it represents an amplifier (see in Fig 7.1). Suppose R,» Rs, drop across Rs is very small.



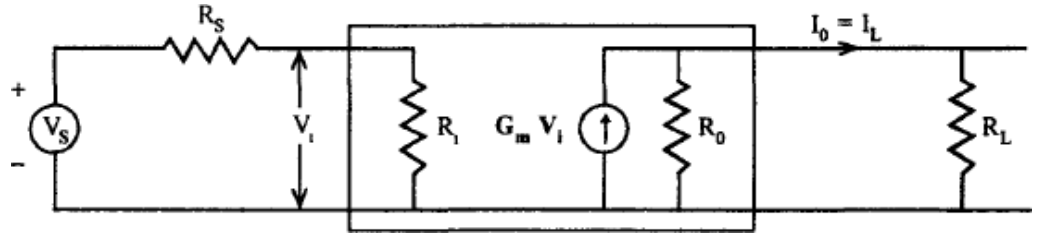
CURRENT AMPLIFIER

An ideal current amplifier is one which gives output current proportional to input current and the proportionality factor is independent ofRs and RL.



TRANSCONDUCTANCE AMPLIFIER

Ideal Transconductance amplifier supplies output current which is proportional to input voitage independently ofthe magnitude ofRs and RL.

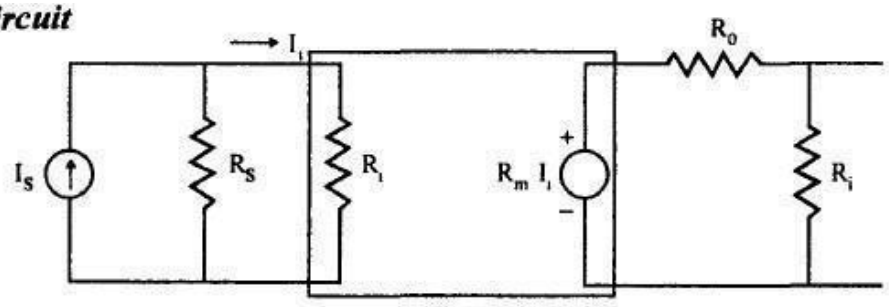


TRANS RESISTANCE AMPLIFIER

It gives output voltage Vo proportional to Is, independent of Rs a. RL. For *ideal amplifiers*

Rj =0, Ro=O

Equivalent circuit

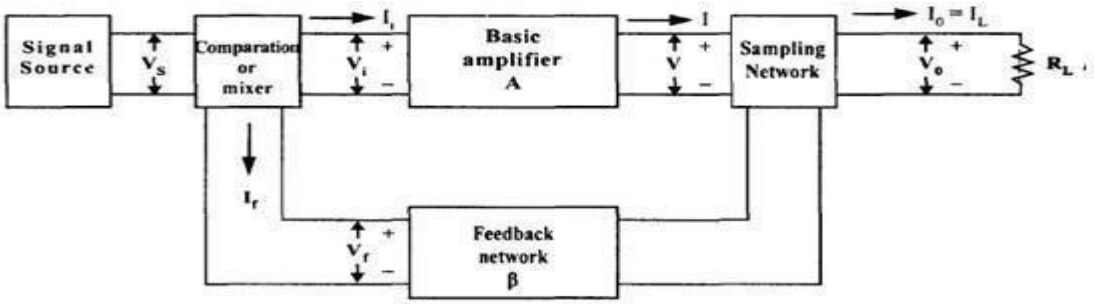


Concepts of feedback

The process of injecting a fraction of output energy of some device back to the input is known as **feedback**.

The principle of feedback is probably as old as the invention of first machine but it is only some 50 years ago that feedback has come into use in connection with electronic circuits. It has been found very useful in reducing noise in amplifiers and making amplifier operation stable. Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers *viz positive feedback* and *negative feedback*.

GENERALIZED BLOCK SCHEMATIC



Signal Source

It can be a voltage source V s or a current source Is FEEDBACK NETWORK

It is a passive two port network. It may contain resistors, capacitors or inductors. But usually a resistance is used as the feedback element. Here the output current is sampled and feedback. The feedback network is connected in series with te output. This is called as *Current Sampling or* Loop Sampling.

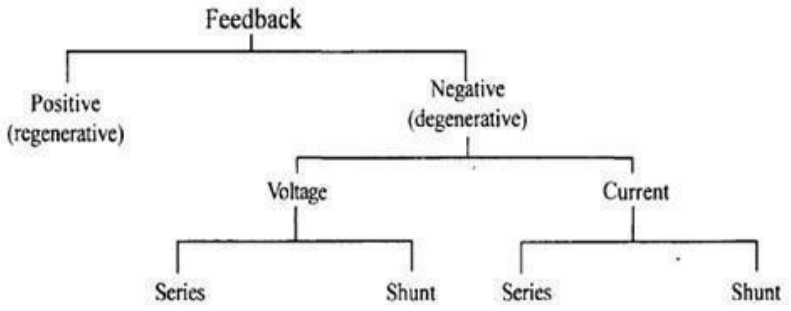
A voltage feedback is distinguished in this way from current feedback. For voltage feedback,

the feedback element (resistor) will be in parallel with the output. For current feedback the element will be in series.

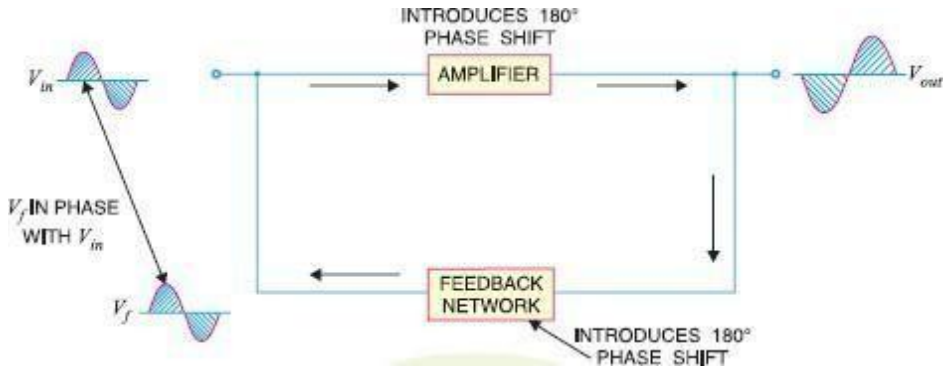
COMPARATOR OR MIXER NETWORK

This is usually a differential amplifier. It has two inputs and gives a single output which is the difference of the two inputs.

basic types of feedback in amplifiers

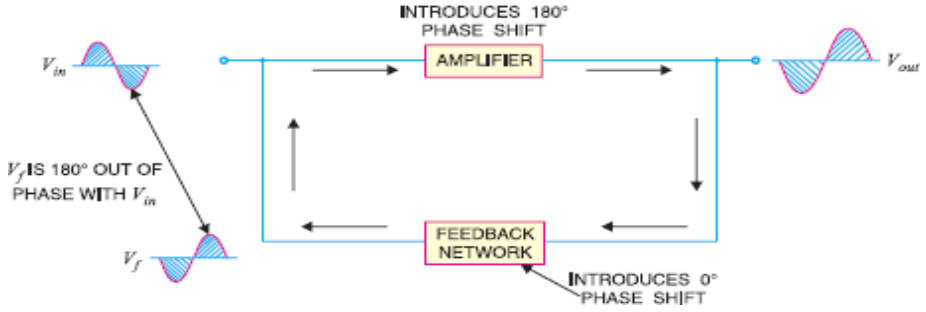


(i) Positive feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback*. This is illustrated in Fig.. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the *feedback voltage Vf* to be in phase with the input signal *Vin*.



The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative feedback. When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback*. This is illustrated in Fig.. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (*i.e.*, 0° phase shift). The result is that the *feedback voltage Vf* is 180° out of phase with the input signal *Vin*.



General characteristics of negative feedback amplifiers

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers :

(i) Gain stability. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product *Av mv* much greater than MODULEy. Therefore, in the above relation, 1 can be neglected as compared to

$$A_{vf} = \frac{A_v}{A_v\, m_v} = \frac{1}{m_v}$$

Av mv and the expression becomes : It may be seen that the gain now depends only upon feedback fraction *mv i.e.*, on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(ii) Reduces non-linear distortion. A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear

$$D_{vf} = \frac{D}{1 + A_v\, m_v}$$

distortion in large signal amplifiers. It can be proved mathematically that :

where *D* = distortion in amplifier without feedback

Dvf = distortion in amplifier with negative feedback

It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor 1 + *Av mv*.

(iii) Improves frequency response. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

(iv) Increases circuit stability. The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilized or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(v) Increases input impedance and decreases output impedance. The negative voltage

feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

(a) Input impedance. The increase in input impedance with negative voltage feedback can be explained by referring to Fig.. Suppose the input impedance of the amplifier is *Zin* without feedback and *Z 'in* with negative feedback. Let us further assume that input current is *i*1.

$$Z'_{in} = Z_{in}(1 + A_v m_v)$$

(b) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is given by :

$$Z'_{out} = \frac{Z_{out}}{1 + A_v m_v}$$

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor 1 + *Av mv*. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

Effect of feedback on amplifier characteristics

CLASSIFACTION OF FEEDBACK AMPLIFIERS

There are four types of feedback,

1. Voltage series feedback.
2. Voltage shunt feedback.
3. Current shunt feedback.
4. Current series feedback.

If the feedback signal is taken across RL, it is a Vo or so it is *Voltage feedback.*

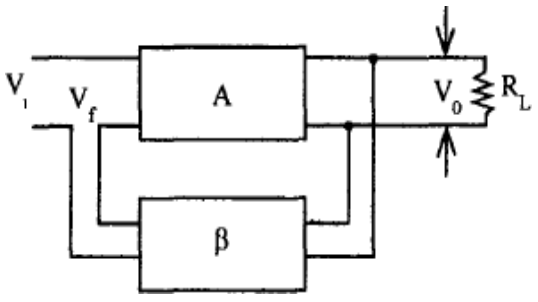
If the feedback signal is taken in series with the output terminals, feedback signal is proportional to I0 , So it is *current feedback.*

If the feedback signal is in series with the input, it is *seriesfeedback.*

If the feedback signal is in shunt with the input, it is *shuntfeedback.*

Voltage Series Configuration

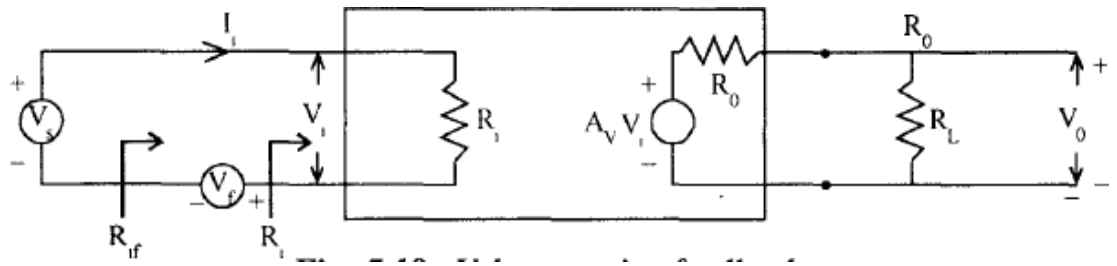
Feedback signal is taken across RL.proportional to Vo. So it is voltage feedback. Vf is coming in series with VI So it is Voltage series feedback.



Voltage series feedback.

EXPRESSION FOR INPUT RESISTANCE RI WITH VOLTAGE SERIES FEEDBACK

In this circuit Av represents the open circuit voltage gain taking Rs into account



Voltage series feedback

$$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$$

$$V_S = I_i R_i + \beta \cdot V_0$$

$$\boxed{\frac{V_s}{I_i} = R_i + \frac{\beta . V_o}{I_i} = R_i\left(1 + \frac{\beta . V_o}{I_i \times R_i}\right)}$$

$$R_{if} = R_i\left(1 + \beta . \frac{V_o}{V_i}\right) = R_i(1 + \beta . A_V)$$

A_V = voltage gain, without feedback.

EXPRESSION FOR OUTPUT RESISTANCE Ro WITH VOLTAGE SERIES FEEDBACK

$$V_i = V_S - V_f$$

$$V_s = V_i + V_f$$

$$R_0' = R_{if} = V_S / I_i .$$

$$V_f = I_i R_i + V_f = I_i R_i + \beta V_0$$

$$V_0 = \frac{A_v V_i R_L}{R_o + R_L} = (A_V I_i R_i)$$

$$\frac{A_v . R_L}{R_o + R_L} = A_V, \; V_i = I_i . R_i .$$

R_O is determined by impressing voltage 'V' at the output terminals or messing 'I', with input R_{of}

$$I = \frac{V_0 - A_V V_1}{R_0} = \frac{V_0 + \beta A_v V}{R_o}$$

$\because$ V_0 = output voltage.

$V_1 = -\beta_V$

Because with $V_S = 0.\ V_1 = -V_f = -\beta_V$

Hence, $R_{of} = \frac{V_0}{I} = \frac{R_o}{1 + \beta A_v}$

This expression is excluding R_L. If we consider R_L also R_{of} is in parallel with R_L.

$$R_{of}' = \frac{R_{of} . R_L}{R_{of} + R_L}$$ Substitute the1 value of R_{of}

$$R_{of}' = \frac{\frac{R_o}{1 + \beta A_V} \times R_L}{\frac{R_0}{1 + \beta A_V} + R_L} = \frac{R_o R_L}{R_o + R_L + \beta . A_v R_L}$$

terminals.-shorted.

Disconnect R_{oL} To find R_{of}' remove external signal (set Vs = 0, or Is = 0) Let $R_L = \infty$ Impress a voltage V across the output terminals and calculate the current I delivered by V.

Then, R_{Of} = V/I.

OSCILLATORS

Condition Classification of oscillators for oscillations

RC Phase shift Oscillators

Generalized analysis of LC Oscillators- Hartley Oscillators Colpitts Oscillators,

Wien Bridge Oscillators Crystal Oscillators, Stability of Oscillators

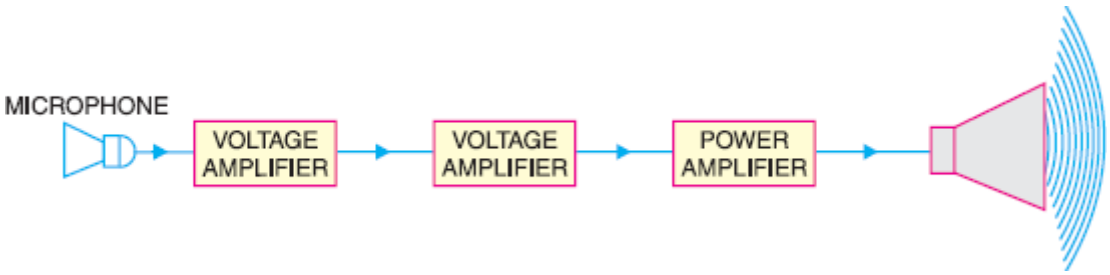
LARGE SIGNAL AMPLIFIERS

INTRODUCTION

A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. The first few stages in this multistage amplifier have the function of only voltage amplification. However, the last stage is designed to provide maximum power. This final stage is known as *power stage*.

The term audio means the range of frequencies which our ears can hear. The range of human hearing extends from 20 Hz to 20 kHz. Therefore, audio amplifiers amplify electrical signals that have a frequency range corresponding to the range of human hearing *i.e.* 20 Hz to 20 kHz. Fig.

12.1 shows the block diagram of an audio amplifier. The early stages build up the voltage level of the signal while the last stage builds up power to a level sufficient to operate the loudspeaker. In this chapter,



we shall talk about the final stage in a multistage amplifier—the power amplifier.

Transistor Audio Power Amplifier

A transistor amplifier which raises the power level of the signals that have audio frequency range is known as **transistor audio power amplifier.** In general, the last stage of a multistage amplifier is the *power stage*. The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power. A transistor that is suitable

for power amplification is generally called a *power transistor*. It differs from other transistors mostly in size ; it is considerably larger to provide for handling the great amount of power.

Audio power amplifiers are used to deliver a large amount of power to a low resistance load. Typical load values range from 300Ω (for transmission antennas) to 8Ω (for loudspeakers). Although these load values do not cover every possibility, they do illustrate the fact that audio power amplifiers usually drive low-resistance loads. The typical power output rating of a power amplifier is 1W or more.

Small-Signal and Large-Signal Amplifiers:The input signal to a multistage amplifier is generally small (a few mV from a cassette or CD or a few μV from an antenna). Therefore, the first few stages of a multistage amplifier handle small signals and have the function of only voltage amplification. However,

the last stage handles a large signal and its job is to produce a large amount of power in order to operate the output device (*e.g.* speaker).

(i) Small-signal amplifiers. Those amplifiers which handle small input a.c. signals (a few μV or a few mV) are called *small-signal amplifiers.* Voltage amplifiers generally fall in this class.

The small-signal amplifiers are designed to operate over the linear portion of the output characteristics. Therefore, the transistor parameters such as current gain, input impedance, output impedance etc. do not change as the amplitude of the signal changes. Such amplifiers amplify the signal with little or no distortion.

(ii) Large-signal amplifiers. Those amplifiers which handle large input a.c. signals (a few volts) are called *large-signal amplifiers.* Power amplifiers fall in this class. The large-signal amplifiers are designed to provide a large amount of a.c. power output so that they can operate the output device *e.g.* a speaker. The main features of a large-signal amplifier or power amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device. It may be noted that all large-signal amplifiers are not necessarily power amplifiers but it is safe to say that most are. In general, where amount of power involved is 1W or more, the amplifier is termed as *power amplifier.*

Output Power of Amplifier

An amplifier converts d.c. power drawn from d.c. supply *VCC* into a.c. output power. The output power is always less than the input power because losses occur in the various resistors present in the circuit. For example, consider the R-C coupled amplifier circuit shown in Fig. 12.2. The currents are flowing through various resistors causing I^2R loss. Thus power loss in $R1$ is $I1^2 R1$, power loss in RC is $IC^2 RC$, power loss in RE is $IE^2 RE$ and so on. All these losses appear as heat. Therefore, losses occurring in an amplifier not only decrease the efficiency but they also increase the temperature of the circuit.

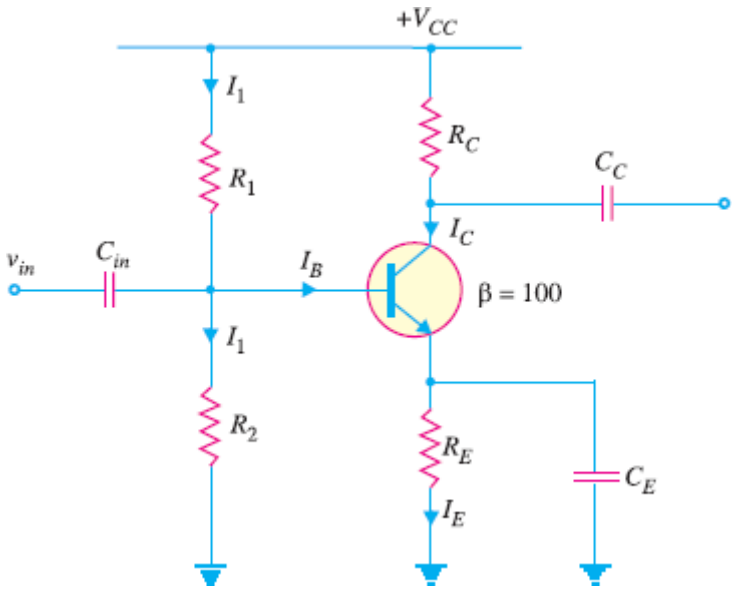


Fig. 4.2

When load *RL* is connected to the amplifier, A.C. output power,

$$P_O = \frac{V_L^2}{R_L}$$

Example 4.1. If in Fig. 4.2; R1 = 10 k ; R2 = 2.2 k ; RC = 3.6 k ; RE = 1.1. k and VCC = + 10 V, find the d.c. power drawn from the supply by the amplifier.

Solution. The current *I*1 flowing through *R*1 also flows through *R*2 (a reasonable assumption because *IB* is small).

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{10\text{V}}{10\ \text{k}\Omega + 2.2\ \text{k}\Omega} = \frac{10\text{V}}{12.2\ \text{k}\Omega} = 0.82\ \text{mA}$$

D.C. voltage across R_2, $V_2 = I_1 R_2 = 0.82\ \text{mA} \times 2.2\ \text{k}\Omega = 1.8\text{V}$

D.C. voltage across R_E, $V_E = V_2 - V_{BE} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V}$

D.C. emitter current, $I_E = V_E/R_E = 1.1\text{V}/1.1\ \text{k}\Omega = 1\ \text{mA}$

$\therefore \quad I_C \simeq I_E = 1\ \text{mA}$

Total d.c current I_T drawn from the supply is

$$I_T = I_C + I_1 = 1\ \text{mA} + 0.82\ \text{mA} = 1.82\ \text{mA}$$

$\therefore$ D.C. power drawn from the supply is

$$P_{dc} = V_{CC} I_T = 10\text{V} \times 1.82\ \text{mA} = \mathbf{18.2\ mW}$$

Example 4.2. Determine the a.c. load power for the circuit shown in Fig. 4.3.

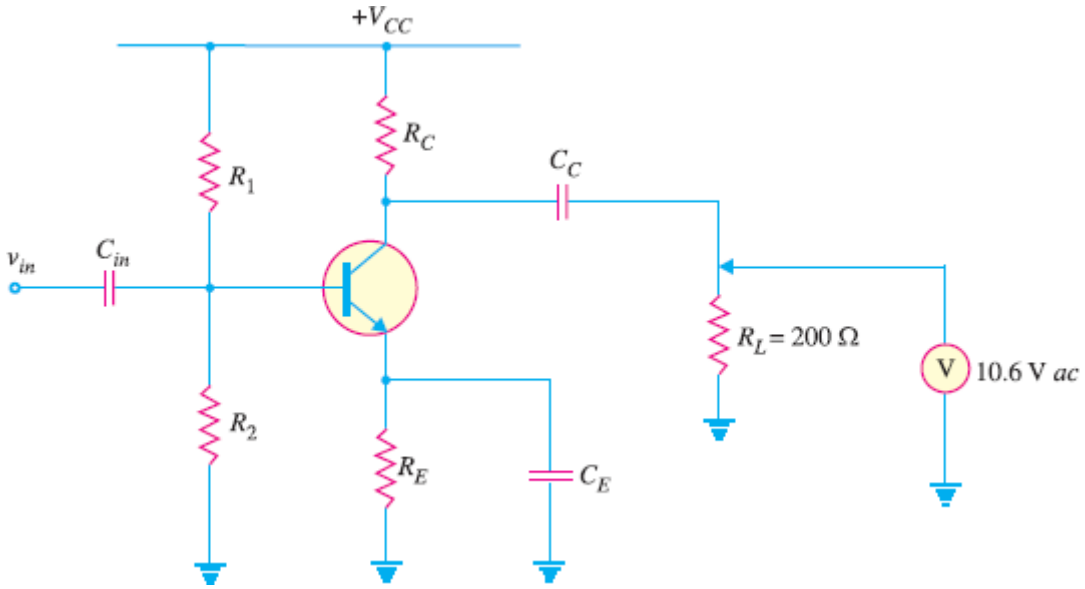


Fig. 4.3.

Solution. The reading of a.c. voltmeter is 10.6V. Since a.c. voltmeters read r.m.s. voltage, we have,

$$\text{A.C. output power, } P_o = \frac{V_L^2}{R_T} = \frac{(10.6)^2}{200\ \Omega} = \mathbf{561.8\ mW}$$

Example 4.3. In an RC coupled power amplifier, the a.c. voltage across load RL (= 100) has a peak- to-peak value of 18V. Find the maximum possible a.c. load power.

Solution. The peak-to-peak voltage, VPP = 18V. Therefore, peak voltage (or maximum voltage)

=

The distinction between voltage and power amplifiers is somewhat artificial since useful power (*i.e.* product of voltage and current) is always developed in the load resistance through which current flows. The difference between the two types is really one of degree; it is a question of how much voltage and how much power. A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level. On the other hand, a power amplifier is designed to obtain maximum output power.

$$A_v = \beta \times \frac{R_C}{R_{in}}$$

1. Voltage amplifier. The voltage gain of an amplifier is given by :

In order to achieve high voltage amplification, the following features are incorporated in such amplifiers :

(i) The transistor with high β□ (>100) is used in the circuit. In other words, those transistors are employed which have thin base.

□

(ii) The input resistance *Rin* of the transistor is sought to be quite low as compared to the collector load *RC*.

(iii) A relatively high load *RC* is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (j 1 mA). If the collector current is small, we can use large *RC* in the collector circuit.

2. Power amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current. In order to achieve high power amplification, the following features are incorporated in such amplifiers :

(i) The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

(ii) The base is made thicker to handle large currents. In other words, transistors with comparatively smaller are used.

(iii) Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form :

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually *R – C* coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

Example 4.4. A power amplifier operated from 12V battery gives an output of 2W. Find the maximum collector current in the circuit.

Solution.

Let IC be the maximum collector current.

Power = battery voltage □□ collector current

$$2 = 12 \times I_C$$

$$I_C = \frac{2}{12} = \frac{1}{6}\text{A} = \mathbf{166.7\ mA}$$

This example shows that a power amplifier handles large power as well as large current. **Example**

4.5. A voltage amplifier operated from a 12 V battery has a collector load of 4 k . Find the maximum collector current in the circuit.

$$\text{Max. collector current} = \frac{\text{battery voltage}}{\text{collector load}} = \frac{12\text{ V}}{4\text{ k}\Omega} = 3\text{ mA}$$

Solution. **The maximum collector current will flow when the whole battery voltage is dropped across RC.**

This example shows that a voltage amplifier handles small current.

Example 4.6. A power amplifier supplies 50 W to an 8-ohm speaker. Find (i) a.c. output voltage (ii) a.c. output current.

Solution.

(*i*) $P = V^2/R$

$\therefore$ a.c. output voltage, $V = \sqrt{PR} = \sqrt{50 \times 8} = 20\text{ V}$

(*ii*) a.c. output current, $I = V/R = 20/8 = 2.5\text{ A}$

Performance Quantities of Power Amplifiers

As mentioned previously, the prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are : ***collector efficiency, distortion*** and ***power dissipation capability.***

(i) Collector efficiency. The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output. Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as collector efficiency and may be defined as under :

The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as **collector efficiency.**

Collector efficiency means as to how well an amplifier converts d.c. power from the battery into a.c. output power. For instance, if the d.c. power supplied by the battery is 10W and a.c. output power is 2W, then collector efficiency is 20%. The greater the collector efficiency, the larger is the a.c. power output. It is obvious that for power amplifiers, maximum collector efficiency is the desired goal.

(ii) Distortion. *The change of output wave shape from the input wave shape of an amplifier is known as* **distortion.** A transistor like other electronic devices, is essentially a non-linear device. Therefore, whenever a signal is applied to the input of the transistor, the output signal is not exactly like the input signal *i.e.* distortion occurs. Distortion is not a problem for small signals (*i.e.* voltage amplifiers) since transistor is a linear device for small variations about the operating

point. However, a power amplifier handles large signals and, therefore, the problem of distortion immediately arises. For the comparison of two power amplifiers, the one which has the less distortion is the better. We shall discuss the method of reducing distortion in amplifiers in the chapter of negative feedback in amplifiers.

(iii) Power dissipation capability. *The ability of a power transistor to dissipate heat is known as* **power dissipation capability.** As stated before, a power transistor handles large currents and heats up during operation. As any temperature change influences the operation of transistor, therefore, the transistor must dissipate this heat to its surroundings. To achieve this, generally a *heat sink* (a metal case) is attached to a power transistor case. The increased surface area allows heat to escape easily and keeps the case temperature of the transistor within permissible limits. Classification of Power Amplifiers

Transistor power amplifiers handle large signals. Many of them are driven so hard by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle. Therefore, such amplifiers are generally classified according to their mode of operation

i.e. the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as :

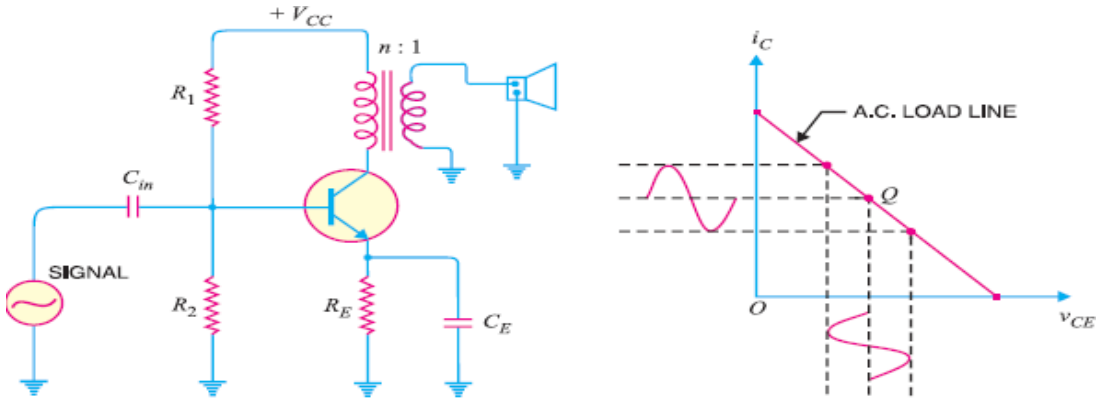
Amplifier circuits may be classified in terms of the portion of the cycle for which the active device conducts.

Class A: It is one, in which the active device conducts for the full 360°. Class B: Conduction for 1800

Class C: Conduction for < 1800

Class AB :Conduction angle is between 1800 and 3600

(*i*) class *A* power amplifier **(*ii*)** class *B* power amplifier **(*iii*)** class *C* power amplifier



(*i*) (*ii*)

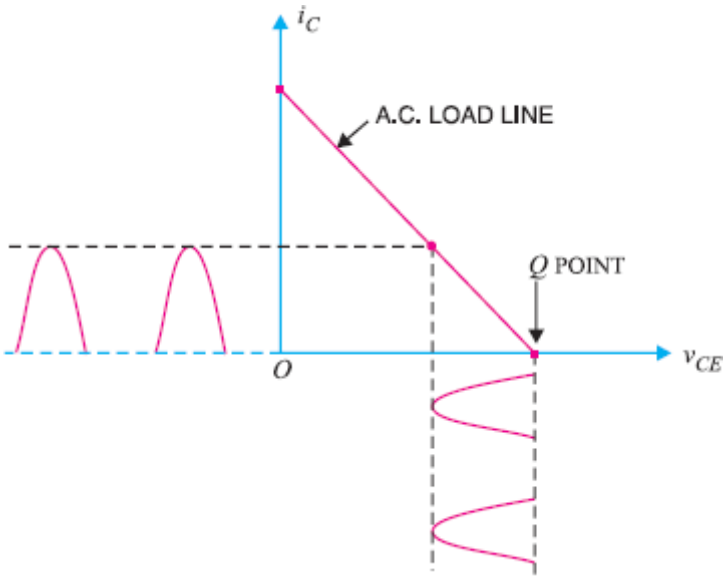
(i) **Class A power amplifier.** *If the collector current flows at all times during the full cycle of the*

(ii) *signal, the power amplifier is known as* **class A power amplifier.**

Fig. 4.4

Obviously, for this to happen, the power amplifier must be biased in such a way that no part of the signal is cut off. Fig. 4.4 (*i*) shows circuit of class *A* power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers. The use of transformer permits impedance matching, resulting in the transference of maximum power to the load *e.g.* loudspeaker. Fig. 4.4 (*ii*) shows the class *A* operation in terms of *a.c.* load line. The operating point *Q* is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion. However, they have the disadvantage of low power output and low collector efficiency (about 35%).

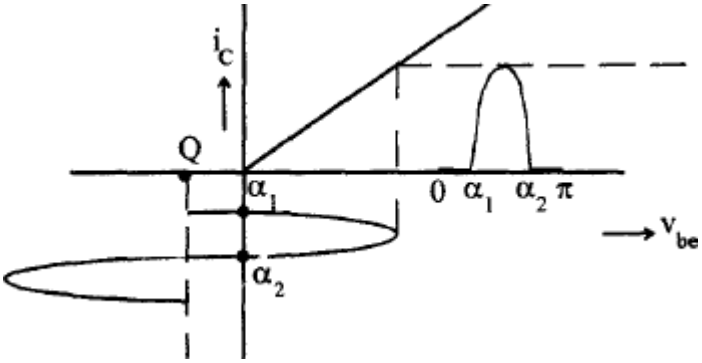
(iii) **Class B power amplifier.** *If the collector current flows only during the positive half-cycle of the input signal, it is called a* **class B power amplifier.** In class *B* operation, the transistor bias is so adjusted that zero signal collector current is zero *i.e.* no biasing circuit is needed at all. During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows. Fig. 12.5 shows the class *B* operation in terms of a.c. load line. Obviously, the operating point *Q*



shall be located at collector cut off voltage. It is easy to see that output from a class *B* amplifier is amplified half-wave rectification. In a class *B* amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs. However, class *B* amplifiers provide higher power output and collector efficiency (50 −60%). Such amplifiers are mostly used for power amplification in push-pull arrangement. In such an Arrangement, 2 transistors are used in class *B* operation. One transistor amplifies the positive half cycle of the signal while the other amplifies the negative half-cycle.

(iv) **Class C power amplifier.** *If the collector current flows for less than half-cycle of the input*

signal, it is called **class C power amplifier.** In class *C* amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts. Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers *i.e.* to amplify a narrow band of frequencies near the resonant frequency.



Expression for Collector Efficiency

For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.

Now, Collector efficiency

$$* P_o = [(0.5 \times 0.707) v_{ce\,(p-p)}]\,[(0.5 \times 0.707) i_{c\,(p-p)}]$$

$$= \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$$

$$\text{Collector } \eta = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8\, V_{CC}\, I_C}$$

where *Vce* is the *r.m.s.* value of signal output voltage and *Ic* is the *r.m.s.* value of output signal current. In terms of peak-to-peak values (which are often convenient values in load-line work), the

$$\text{Collector efficiency, } \eta = \frac{\text{a.c. power output}}{\text{d.c. power input}}$$

$$= \frac{P_o}{P_{dc}}$$

$$* P_{dc} = V_{CC} I_C$$

$$P_o = V_{ce} I_c$$

a.c. power output can be expressed as :

Series-Fed Class A Amplifier

Fig. 4.6 (*i*) shows a series – fed class *A* amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency. Nevertheless, it will help the reader to understand the class *A* operation. The d.c. load line of the circuit is shown in Fig. 12.6 (*ii*). When an *ac* signal is applied to the amplifier, the output current and voltage will vary about the operating point *Q*. In order to achieve the maximum

symmetrical swing of current and voltage (to achieve maximum output power), the *Q* point should be located at the centre of the *dc* load line. In that case, operating point is *IC* =*VCC*/2*RC* and *VCE* = *VCC*/2 .

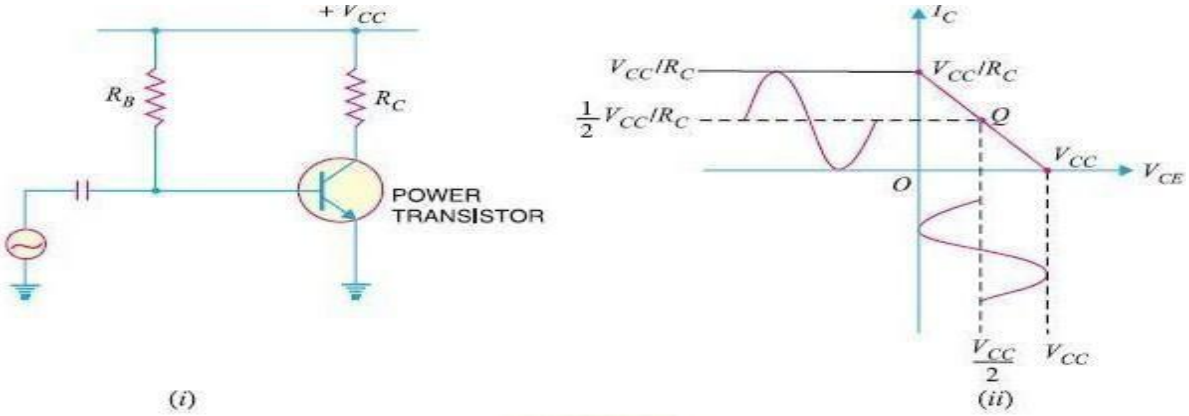


Fig. 4.6

$$\text{Maximum } v_{ce\,(p-p)} = V_{CC}$$

$$\text{Maximum } i_{c\,(p-p)} = V_{CC}/R_C$$

$$\text{Max. } ac \text{ output power, } P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8R_C}$$

$$\text{D.C. power supplied, } P_{dc} = V_{CC}\, I_C = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C}$$

$$\therefore \quad \text{Maximum collector } \eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = 25\%$$

Thus the maximum collector efficiency of a class *A* series-fed amplifier is 25%. In actual practice, the collector efficiency is far less than this value.

Example 4.7. *Calculate the* (*i*) *output power* (*ii*) *input power and* (*iii*) *collector efficiency of the amplifier circuit shown in Fig. 12.7* (*i*). *It is given that input voltage results in a base current of 10 mA peak.*

Maximum Collector Efficiency of Transformer Coupled Class A Power Amplifier

In class *A* power amplifier, the load can be either connected directly in the collector or it can be

Solution. First draw the *d.c.* load line by locating the two end points *viz.*, $I_{C\,(sat)} = V_{CC}/R_C = 20\text{ V}/20\,\Omega = 1\text{ A} = 1000\text{ mA}$ and $V_{CE} = V_{CC} = 20\text{ V}$ as shown in Fig. 12.7 (*ii*). The operating point *Q* of the circuit can be located as under :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1\,\text{k}\Omega} = 19.3\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 25\,(19.3\text{ mA}) = 482\text{ mA}$$

$$\text{Also} \quad V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - (482\text{ mA})\,(20\,\Omega) = 10.4\text{ V}$$

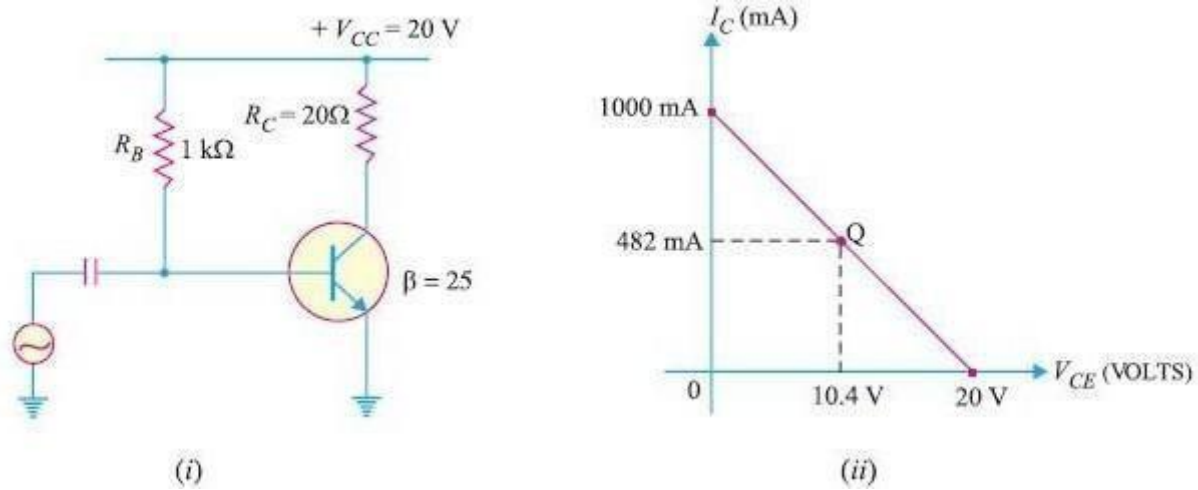
The operating point *Q* (10.4 V, 482 mA) is shown on the d.c. load line.

(*i*) $i_c\text{-}(peak) = \beta\, i_b\,(peak) = 25 \times (10\text{ mA}) = 250\text{ mA}$

$$\therefore \quad P_{o\,(ac)} = \frac{i_c^2(peak)}{2} R_C = \frac{(250 \times 10^{-3})^2}{2} \times 20 = \mathbf{0.625\text{ W}}$$

(*ii*) $P_{dc} = V_{CC}\, I_C = (20\text{ V})\,(482 \times 10^{-3}) = \mathbf{9.6\text{ W}}$

(*iii*) $\text{Collector } \eta = \frac{P_o(ac)}{P_{dc}} \times 100 = \frac{0.625}{9.6} \times 100 = \mathbf{6.5\ \%}$



(*i*) (*ii*)

transformer coupled. The latter method is often preferred for two main reasons. First, transformer coupling permits impedance matching and secondly it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.

Fig. 12.8 (*i*) shows the transformer coupled class *A* power amplifier. In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig. 4.8 (*ii*). Under zero signal conditions, the effective resistance in the collector circuit is that of the primary winding of the transformer. The primary resistance has a v line is a vertical line rising from *VCC* as shown in Fig. 12.8 (*ii*).

When signal is applied, the collector current will vary about the operating point *Q*.

In order to get maximum a.c. power output (and hence maximum collector □), the peak value ofcollector current due to signal alone should be equal to the zero signal collector current *IC*. In terms of a.c. load line, the operating point *Q* should be located at the centre of a.c. load line.ery small value and is assumed zero. Therefore, d.c. load

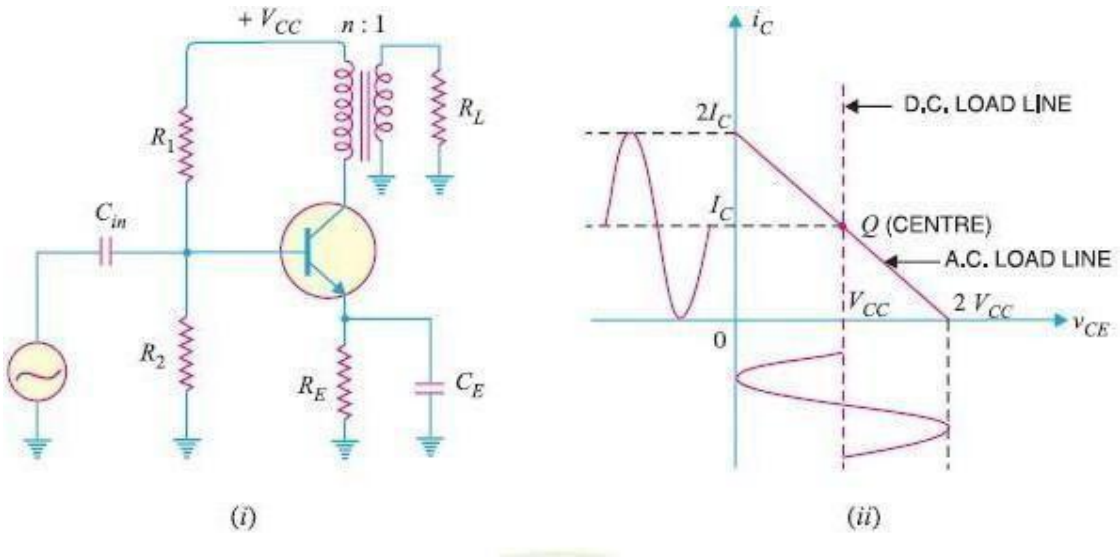


Fig. 4.8

During the peak of the positive half-cycle of the signal, the total collector current is 2 *IC* and *vce* = 0. During the negative peak of the signal, the collector current is zero and *vce* = 2*VCC*.

 Peak-to-peak collector-emitter voltage is

vce (*p* - *p*) = 2*VCC* Peak-to-peak collector current, *ic* (*p* - *p*) = 2 *IC*

$$= \frac{v_{ce(p-p)}}{R_L'} = \frac{2V_{CC}}{R_L'}$$

where *RL'* is the reflected value of load *RL* and appears in the primary of the transformer. If *n* (= *Np*/*Ns*) is the turn ratio of the transformer, then, *RL'* = n^2 *RL*.

$$= I_C^2 R_L'$$

d.c. power input, *Pdc* = *VCC IC*

Max.a.c. output power, *Po* (*max*)=

$$P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8}$$

$$= \frac{2V_{CC} \times 2I_C}{8}$$

$$= \frac{1}{2} V_{CC} I_C$$

$$= \frac{1}{2} I_C^2 R_L'$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\,(max)}}{P_{dc}} \times 100$$

$$= \frac{(1/2)\, I_C^2\, R_L'}{I_C^2\, R_L'} \times 100 = 50\%$$

Important Points About Class A Power Amplifier

(i) A *transformer coupled class *A* power amplifier has a maximum collector efficiency of50% *i.e.*, maximum of 50% d.c. supply power is converted into a.c. power output. In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.

(ii) The power dissipated by a transistor is given by:

Pdis = *Pdc* - *Pac* where *Pdc* = available d.c. power *Pac* = available a.c. power

Clearly, in class *A* operation, the transistor must dissipate less heat when signal is applied and therefore runs cooler.

(iii) When no signal is applied to a class *A* power amplifier, *Pac* = 0.

Pdis = *Pdc*

Thus in class *A* operation, maximum power dissipation in the transistor occurs under zero signal conditions. Therefore, the power dissipation capability of a power transistor (for class *A* operation) must be atleast equal to the zero signal rating. For example, if the zero signal power dissipation of a transistor is 1 W, then transistor needs a rating of atleast 1W. If the power rating of the transistor is less than 1 W, it is likely to be damaged.

(iv) When a class *A* power amplifier is used in the final stage, it is called **single ended class A power amplifier.**

Example 4.8. *A power transistor working in class A operation has zero signal power dissipation of 10 watts. If the a.c. output power is 4 watts, find :*

(*i*) *collector efficiency* (*ii*) *power rating of transistor*

Solution.

Zero signal power dissipation, *Pdc* = 10 W

a.c. power output, *Po* = 4 W

(i) Collector efficiency = $\frac{P_o}{P_{dc}} \times 100 = \frac{4}{10} \times 100 = 40\%$

(ii) The zero signal power represents the worst case *i.e.* maximum power dissipation ina transistor occurs under zero signal conditions.

∴ Power rating of transistor = **10 W**

It means to avoid damage, the transistor must have a power rating of atleast 10 W.

Example 4.9. *A class A power amplifier has a transformer as the load. If the transformer has*

a turn ratio of 10 and the secondary load is 100 Ω, find the maximum a.c. power output. Given that zero signal collector current is 100 mA.

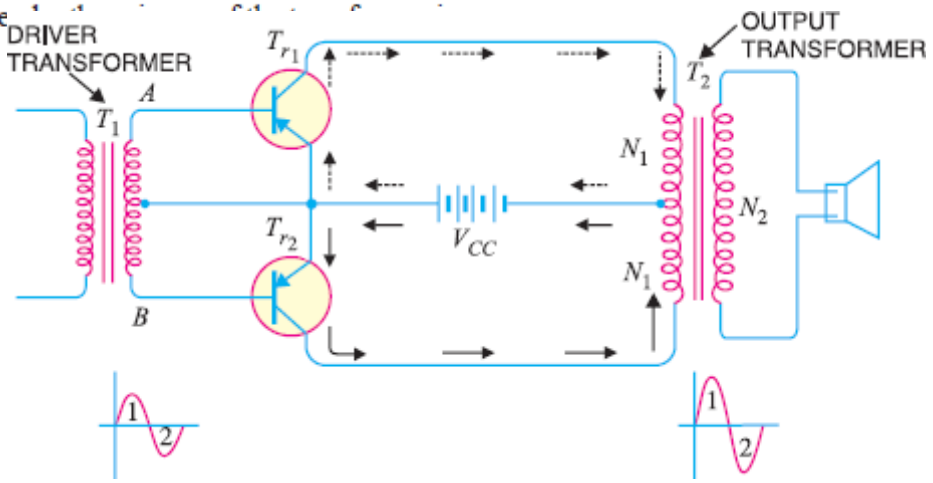
Solution.

Transformer turn ratio, $n = 10$

Zero signal collector current, $I_C = 100\,\text{mA}$

Load as see

$\therefore$



Secondary load, $RL = 100\ \Omega$

Class B Push-Pull Power Amplifier

The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. 4.14 shows the circuit of a push-pull amplifier. Two transistors *Tr*1 and *Tr*2 placed back to back are employed. Both transistors are operated in class *B* operation *i.e*. collector current is nearly zero in the absence of the signal. The centre-tapped secondary of driver transformer *T*1 supplies equal and opposite voltages to the base circuits of two transistors. The output transformer *T*2 has the centre-tapped primary winding. The supply voltage *VCC* is connected between the bases and this centre tap. The loudspeaker is connected across the secondary of this transformer.

Circuit operation. The input signal appears across the secondary *AB* of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end *A* becomes positive and end *B* negative. This will make the base-emitter junction of *Tr*1 reverse biased and that of *Tr*2 forward biased. The circuit will conduct current due to *Tr*2 only and is shown by solid arrows. Therefore, this half-cycle of the signal is amplified by *Tr*2 and appears in the lower half of the primary of output transformer. In the next halfcycle of the signal, *Tr*1 is forward biased whereas *Tr*2 is reverse biased. Therefore, *Tr*1 conducts and is shown by dotted arrows. Consequently, this half- cycle of the signal is amplified by *Tr*1 and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.

It may be noted here that push-pull arrangement also permits a maximum transfer of power to the load through impedance matching. If *RL* is the resistance appearing across secondary of output transformer, then resistance *R′L* of primary shall become :

$$R_L' = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

where N_1 = Number of turns between either end of primary winding and centre-tap

N_2 = Number of secondary turns

Advantages

(i) The efficiency of the circuit is quite high (i.e 75%) due to class *B* operation.

(ii) A high a.c. output power is obtained.

Disadvantages

(i) Two transistors have to be used.

(ii) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.

(iii) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.

(iv) The circuit gives more distortion.

(v) Transformers used are bulky and expensive.

Maximum Efficiency for Class B Power Amplifier

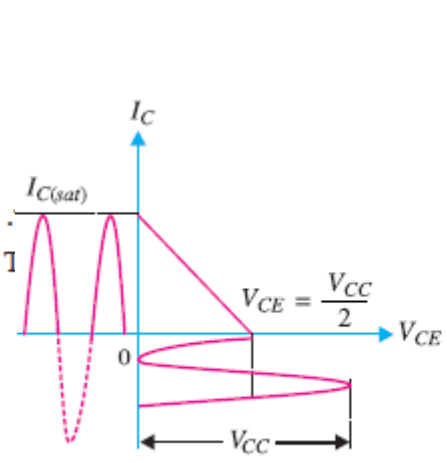
We have already seen that a push-pull circuit uses two transistors working in class *B* operation. For class *B* operation, the Q-point is located at cut-off on both d.c. and a.c. load lines. For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. 4.15 (*i*). It is clear that a.c. output voltage has a peak value of *VCE* and a.c. output current has a peak

$\therefore$ Peak a.c. output voltage $= V_{CE}$

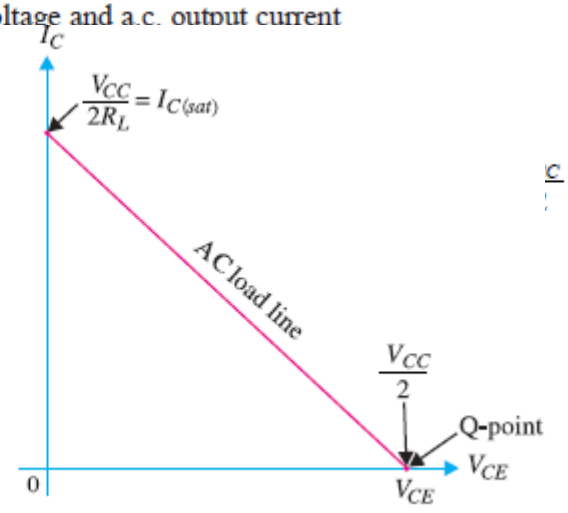
Peak a.c. output current $= I_{C(sat)} = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{2R_L}$ $\left(\because V_{CE} = \frac{V_{CC}}{2}\right)$

Maximum average a.c. output power $P_{o(max)}$ is

$P_{o(max)}$ = Product of r.m.s. values of a.c. output voltage and a.c. output current



(*i*)



(*ii*)

value of *IC* (*sat*). The same information is also conveyed through the a.c. load line for the circuit [See Fig. 4.15 (*ii*)].

Fig. 4.15

where *Idc* is the average current drawn from the supply *VCC*. Since the transistor is on for alternating half-cycles, it effectively acts as a half-wave rectifier.

$$\therefore \quad I_{dc} = \frac{I_{C\,(sat)}}{\pi}$$

$$\therefore \quad P_{dc} = \frac{V_{CC}\, I_{C\,(sat)}}{\pi}$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{0.25\, V_{CC}\ I_{C\,(sat)}}{\left(V_{CC}\, I_{C\,(sat)}\right)/\pi} \times 100 = 0.25\pi \times 100 = 78.5\%$$

Thus the maximum collector efficiency of class *B* power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

Power dissipated by transistors. The power dissipated (as heat) by the transistors in class *B* amplifier is the difference between the input power delivered by *VCC* and the output power delivered to the l

$$P_{2T} = P_{dc} - P_{ac}$$

where P_{2T} = power dissipated by the two transistors

∴ Power dissipated by each transistor is

$$P_T = \frac{P_{2T}}{2} = \frac{P_{dc} - P_{ac}}{2}$$

Example 4.18. *F* *determine (i) maximum load*

Solution. $V_{CC} = 12\ \text{V}\ ;\ R_L = 8\Omega$

(*i*) Maximum load power, $P_{o\,(max)} = 0.25\, V_{CC}\, I_{C\,(sat)}$

$$= 0.25\, V_{CC} \times \frac{V_{CC}}{2\, R_L} \qquad \left(\because I_{C\,(sat)} = \frac{V_{CC}}{2\, R_L}\right)$$

$$= 0.25 \times 12 \times \frac{12}{2 \times 8} = \mathbf{2.25\ W}$$

(*ii*) D.C. input power, $P_{dc} = \frac{V_{CC}\, I_{C\,(sat)}}{\pi} = \frac{V_{CC}}{\pi} \times \frac{V_{CC}}{2\, R_L}$

$$= \frac{12}{\pi} \times \frac{12}{2 \times 8} = \mathbf{2.87\ W}$$

(*iii*) Collector $\eta = \frac{P_{o\,(max)}}{P_{dc}} \times 100 = \frac{2.25}{2.87} \times 100 = \mathbf{78.4\%}$

Example 4.19. *A class B push-pull amplifier with transformer coupled load uses two transistors rated 10 W each. What is the maximum power output one can obtain at the load from thecircuit?*

Solution. The power dissipation by each transistor is $P_T = 10\text{W}$. Therefore, power dissipated by two transistors is $P_{2T} = 2 \times 10 = 20\text{W}$.

Now $$P_{dc} = P_{o\,(max)} + P_{2T} \; ; \; \text{Max. } \eta = 0.785$$

$$\therefore \quad \text{Max } \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + P_{2T}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$$

$$\text{or} \quad 0.785 = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$$

$$\text{or} \quad 0.785\, P_{o\,(max)} + 15.7 = P_{o\,(max)}$$

$$\text{or} \quad P_{o\,(max)}\,(1 - 0.785) = 15.7$$

$$\therefore \quad P_{o\,(max)} = \frac{15.7}{1 - 0.785} = \frac{15.7}{0.215} = \mathbf{73.02\ W}$$

Example 4.20. *A class B amplifier has an efficiency of 60% and each transistor has a rating of 2.5W. Find the a.c. output power and d.c. input power*

Solution. The power dissipated by each transistor is $P_T = 2.5\text{W}$.

Therefore, power dissipated by the two transistors is $P_{2T} = 2 \times 2.5 = 5\text{W}$.

Now $$P_{dc} = P_{ac} + P_{2T} \; ; \; \eta = 0.6$$

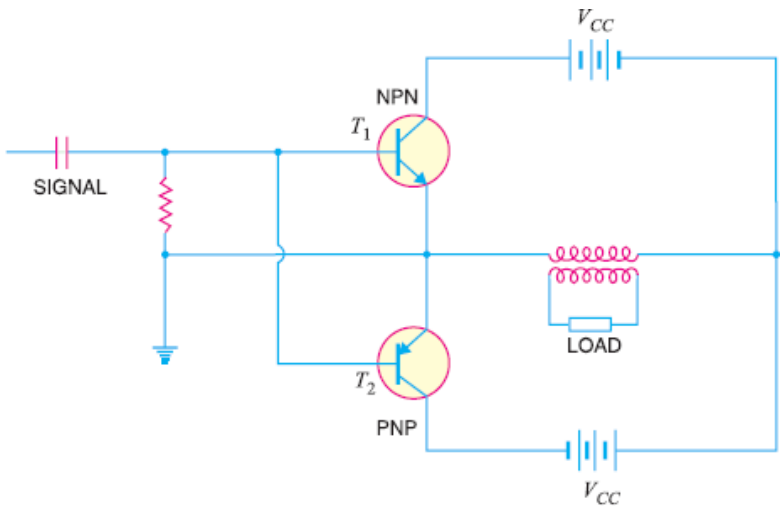
$$\therefore \quad \eta = \frac{P_{ac}}{P_{dc}} = \frac{P_{ac}}{P_{ac} + P_{2T}}$$

$$\text{or} \quad 0.6 = \frac{P_{ac}}{P_{ac} + 5} \qquad \text{or} \quad 0.6\, P_{ac} + 3 = P_{ac}$$

$$\therefore \quad P_{ac} = \frac{3}{1 - 0.6} = \frac{3}{0.4} = \mathbf{7.5\ W}$$

and $$P_{dc} = P_{ac} + P_{2T} = 7.5 + 5 = \mathbf{12.5\ W}$$

Example 4.21. *A class B amplifier uses VCC = 10V and drives a load of 10Ω. Determine the end point values of the a.c. load line.*



Solution.

$$I_{C\,(sat)} = \frac{V_{CC}}{2R_L} = \frac{10\text{V}}{2(10\,\Omega)} = 500\text{ mA}$$

This locates one end-point of the a.c. load line on the collector current axis.

$$V_{CE\,(off)} = \frac{V_{CC}}{2} = \frac{10\text{V}}{2} = 5\text{V}$$

Complementary-Symmetry Amplifier

By complementary symmetry is meant a principle of assembling push-pull class *B* amplifier without requiring centre-tapped transformers at the input and output stages. Fig. 4.16 shows the transistor push-pull amplifier using complementary symmetry. It employs one *npn* and one *pnp* transistor and requires no centre-tapped transformers. The circuit action is as follows. During the positive-half of the input signal, transistor *T*1 (the *npn* transistor) conducts current while *T*2 (the *pnp* transistor) is cut off. During the negative half-cycle of the signal, *T*2 conducts while *T*1 is cut off. In this way, *npn* transistor amplifies the positive half-cycles of the signal while the *pnp* transistor amplifies the negative half-cycles of the signal. Note that we generally use an output transformer (not centre- tapped) for impedance matching.

Fig. 4.16

Advantages

(i) This circuit does not require transformer. This saves on weight and cost.

(ii) Equal and opposite input signal voltages are not required.

Disadvantages

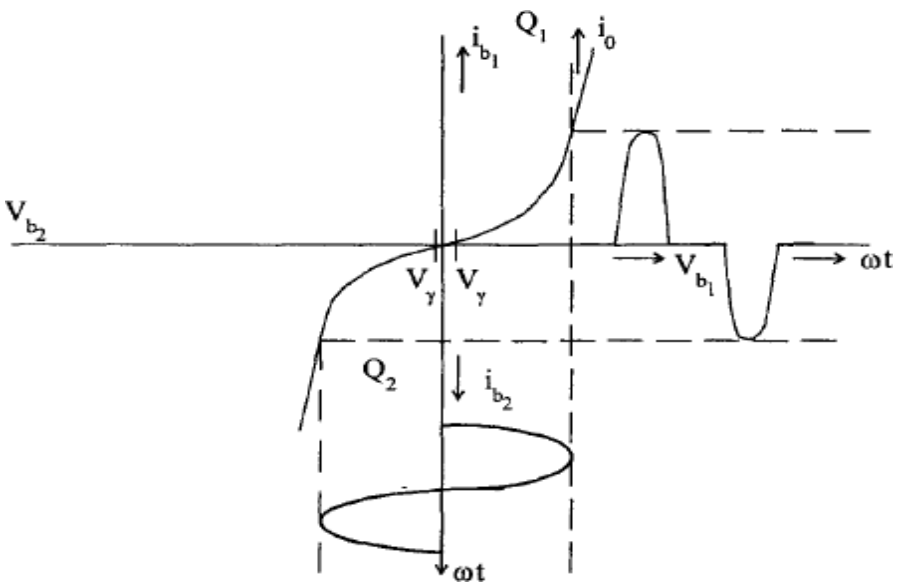
(i) It is difficult to get a pair of transistors (*npn* and *pnp*) that have similar characteristics.

(ii) We require both positive and negative supply voltages.

DISTORTION

Let ib1 V c, Vb1 be the input characteristic of the first transistor and ib2, V s, Vb2 is the input characteristic of th6 second transistor. V y is the cut)n voltage. These are t6e two tiansistors of the class B pushpull amplifier. Now the base input voltage being given to the transistor is sinusoidal, i.e., base drive is sinusoidal. So because of the *cut in voltage*, eventhough input voltage is present, output will not be transmitted or there is distortion in the output current of the transistor. This is known as *crossover distortion.* But this will not occur if the base current drive is sinusoidal. Since in the graphical analysis the input current is taken in the I quadrant. No distortion if the operating point is in the active region. Cross-over distortion can also be laminated in class AB operation. A small stand by current flows at zero excitation. The input signal is shifted by constant DC bias so that the input signal is shifted by an amount V

γ



Thermal Runaway

All semiconductor devices are very sensitive to temperature variations. If the temperature of a transistor exceeds the permissible limit, the transistor may be *permanently damaged. Silicon transistors can withstand temperatures upto 250ºC while the germanium transistors can withstand temperatures upto 100ºC.

There are two factors which determine the operating temperature of a transistor *viz*.

(i) surrounding temperature and

(ii) power dissipated by the transistor.

When the transistor is in operation, almost the entire heat is produced at the collector-base junction. This power dissipation causes the junction temperature to rise. This in turn increases the collector current since more electron-hole pairs are generated due to the rise in temperature. This produces an increased power dissipation in the transistor and consequently a further rise in temperature. Unless adequate cooling is provided or the transistor has built-in temperature compensation circuits to prevent excessive collector current rise, the junction temperature will continue to increase until the maximum permissible temperature is exceeded. If this situation occurs, the transistor will be permanently damaged.

The unstable condition where, owing to rise in temperature, the collector current rises and continues to increase is known as **thermal runaway.**

Thermal runaway must always be avoided. If it occurs, permanent damage is caused and the transistor must be replaced.

Heat Sink

As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat generated must be dissipated to the surroundings in order to keep the temperature within permissible limits. Generally, the transistor is fixed on a metal sheet (usually aluminium) so that additional heat is transferred to the *Al* sheet.

The metal sheet that serves to dissipate the additional heat from the power transistor is known as

heat sink.

Most of the heat within the transistor is produced at the collector junction. The heat sink increases the surface area and allows heat to escape from the collector junction easily. The result is that temperature of the transistor is sufficiently lowered. Thus heat sink is a direct practical means of combating the undesirable thermal effects *e.g.* thermal runaway. material, volume, area, shape, contact between case and sink and movement of air around the sink. Finned aluminium heat sinks yield the best heat transfer per MODULE cost. It should be realised that the use of heat sink alone may not be sufficient to prevent thermal runaway under all conditions. In designing a transistor circuit, consideration should also be given to the choice of

(i) operating point

(ii) ambient temperatures which are likely to be encountered and

(iii) the type of transistor *e.g.* metal case transistors are more readily cooled by conduction than plastic ones.

Circuits may also be designed to compensate automatically for temperature changes and thus stabilise the operation of the transistor components.

Classification of heat Sinks

Low Power Transistor Type.

High Power Transistor Type.

Low Power Transistor Type

- Low Power Transistors can be mounted directly on the metal chassis to increase the heat dissipation capability. The casing of the transistor must be insulated from the metal chassis to prevent shorting.
- Beryllium oxide insulating washers are used for insulating casing from the chassis. They have good thermal conductivity.
- Zinc oxide film silicon compound between washer and chassis, improves the heat transfer from the semiconductor device to case to the chassis.

High Power Transistor Type.

Mathematical Analysis

The permissible power dissipation of the transistor is very important item for power transistors. The permissible power rating of a transistor is calculated from the following relation :

$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

where
P_{total} = total power dissipated within the transistor
$T_{J\,max}$ = maximum junction temperature. It is 90°C for *germanium* transistors and 150°C for *silicon* transistors.
T_{amb} = ambient temperature *i.e.* temperature of surrounding air
θ = *thermal resistance *i.e.* resistance to heat flow from the junction to the surrounding air

The MODULE of Ə is °C/ watt and its value is always given in the transistor manual. A low thermal resistance means that it is easy for heat to flow from the junction to the surrounding air. The larger the transistor case, the lower is the thermal resistance and *vice-versa*. It is then clear that by using heat sink, the value of θ can be decreased considerably, resulting in increased power dissipation.

Example 4.15. *A power transistor dissipates 4 W. If TJmax = 90°C, find the maximum ambient temperature at which it can be operated. Given Ə = 10°C/W.*

Solution.

$P_{total} = 4$ W
$T_{J\,max} = 90°C$
$\theta = 10°C/W$

Now $P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$

or $4 = \frac{90 - T_{amb}}{10}$

∴ Ambient temperature, $T_{amb} = 90 - 40 = 50°C$

The above example shows the effect of ambient temperature on the permissible power dissipation in a transistor. The lower the ambient temperature, the greater is the permissible power dissipation. Thus, a transistor can pass a higher collector current in winter than insummer.

Example 4.16. (*i*) *A power transistor has thermal resistance θ = 300°C/W. If the maximum junction temperature is 90°C and the ambient temperature is 30°C, find the maximum permissible power dissipation.*

(*ii*) *If a heat sink is used with the above transistor, the value of θ is reduced to 60°C/W. Find the maximum permissible power dissipation.*

Solution.

(i) Without heat sink

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 300°C/W$$
$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{300} = 0.2\ W = 200\ mW$$

(ii) With heat sink

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 60°C/W$$
$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{60} = 1\ W = 1000\ mW$$

It is clear from the above example that permissible power dissipation with heat sink is 5 times as compared to the case when no heat sink is used.

Example 4.17. *The total thermal resistance of a power transistor and heat sink is 20°C/W. The ambient temperature is 25°C and TJ max = 200°C. If VCE = 4 V, find the maximum collector current that the transistor can carry without destruction. What will be the allowed value of collector current if ambient temperature rises to 75°C ?*

Solution.

$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{200-25}{20} = 8.75\ W$$

This means that maximum permissible power dissipation of the transistor at ambient temperature of 25°C is 8.75 W *i.e.*

$$V_{CE} I_C = 8.75$$
$$\therefore \quad I_C = 8.75/4 = 2.19\ A$$

Again
$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{200-75}{20} = 6.25\ W$$
$$\therefore \quad I_C = 6.25/4 = 1.56\ A$$

This example clearly shows the effect of ambient temperature.

MODULE IV

LINEAR WAVE SHAPING AND SAMPLING GATES

INTRODUCTION:

A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. The first few stages in this multistage amplifier have the function of only voltage amplification. However, the last stage is designed to provide maximum power. This final stage is known as *power stage*.

The term audio means the range of frequencies which our ears can hear. The range of human hearing extends from 20 Hz to 20 kHz. Therefore, audio amplifiers amplify electrical signals that have a frequency range corresponding to the range of human hearing *i.e*. 20 Hz to 20 kHz. Figure shows the block diagram of an audio amplifier. The early stages build up the voltage level of the signal while the last stage builds up power to a level sufficient to operate the loudspeaker. In this chapter, we shall talk about the final stage in a multistage amplifier—the power amplifier.

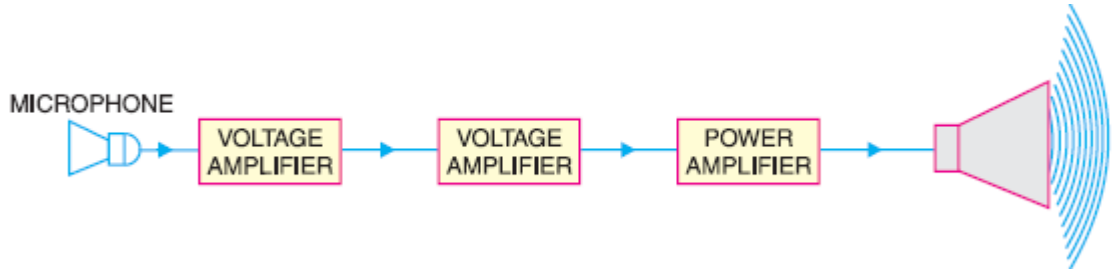


Fig. 4.1

Transistor Audio Power Amplifier

A transistor amplifier which raises the power level of the signals that have audio frequency range is known as **transistor audio power amplifier.** In general, the last stage of a multistage amplifier is the *power stage*. The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power. A transistor that is suitable for power amplification is generally called a *power transistor*. It differs from other transistors mostly in size; it is considerably larger to provide for handling the great amount of power.

Audio power amplifiers are used to deliver a large amount of power to a low resistance load. Typical load values range from 300Ω (for transmission antennas) to 8Ω (for loudspeakers). Although these load

values do not cover every possibility, they do illustrate the fact that audio power amplifiers usually drive low-resistance loads. The typical power output rating of a power amplifier is 1W or more.

Small-Signal and Large-Signal Amplifiers

The input signal to a multistage amplifier is generally small (a few mV from a cassette or CD or a few μV from an antenna). Therefore, the first few stages of a multistage amplifier handle small signals and have the function of only voltage amplification. However, the last stage handles a large signal and its job is to produce a large amount of power in order to operate the output device (*e.g.* speaker).

(i) Small-signal amplifiers. Those amplifiers which handle small input a.c. signals (a few μV or a few mV) are called *small-signal amplifiers.* Voltage amplifiers generally fall in this class. The small-signal amplifiers are designed to operate over the linear portion of the output characteristics. Therefore, the transistor parameters such as current gain, input impedance, output impedance etc. do not change as the amplitude of the signal changes. Such amplifiers amplify the signal with little or no distortion.

(ii) **Large-signal amplifiers.** Those amplifiers which handle large input a.c. signals (a few volts) are called *large-signal amplifiers.* Power amplifiers fall in this class. The large-signal amplifiers are designed to provide a large amount of a.c. power output so that they can operate the output device e.g. a speaker. The main features of a large-signal amplifier or power amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device. It may be noted that all large-signal amplifiers are not necessarily power amplifiers but it is safe to say that most are. In general, where amount of power involved is 1W or more, the amplifier is termed as *power amplifier*.

Output Power of Amplifier

An amplifier converts d.c. power drawn from d.c. supply V_{CC} into a.c. output power. The output power is always less than the input power because losses occur in the various resistors present in the circuit. For example, consider the R-C coupled amplifier circuit shown in Fig. 4.2. The currents are flowing through various resistors causing I^2R loss. Thus power loss in R_1 is I_1^2 $R1$, power loss in RC is I_C^2 R_C, power loss in R_E is I_E^2 R_E and so on. All these losses appear as heat. Therefore, losses occurring in an amplifier not only decrease the efficiency but they also increase the temperature of the circuit.

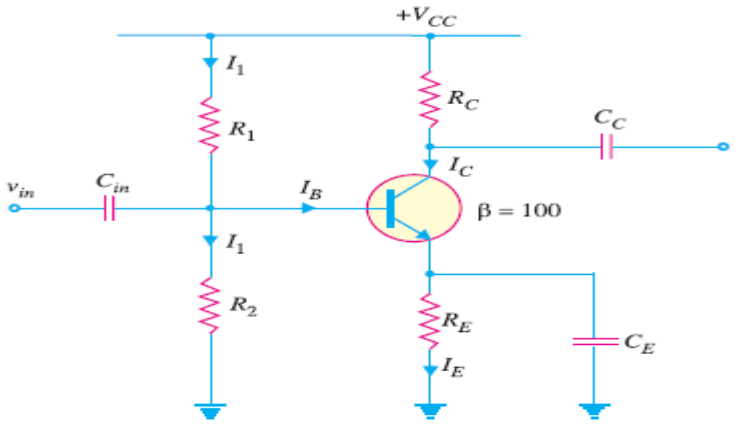


Fig. 4.2

When load R_L is connected to the amplifier, A.C. output power,

$$P_O = \frac{V_L^2}{R_L}$$

Example 4.1. If in Fig. 4.2; R1 = 10 kΩ; R2 = 2.2 kΩ; RC = 3.6 kΩ; RE = 1.1. kΩ and V_{CC}= + 10 V, find the d.c. power drawn from the supply by the amplifier.

Solution. The current I_1 flowing through R_1 also flows through R_2 (a reasonable assumption because I_B is small).

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{10\text{V}}{10\ \text{k}\Omega + 2.2\ \text{k}\Omega} = \frac{10\text{V}}{12.2\ \text{k}\Omega} = 0.82\ \text{mA}$$

D.C. voltage across R_2, $V_2 = I_1 R_2 = 0.82\ \text{mA} \times 2.2\ \text{k}\Omega = 1.8\text{V}$

D.C. voltage across R_E, $V_E = V_2 - V_{BE} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V}$

D.C. emitter current, $I_E = V_E/R_E = 1.1\text{V}/1.1\ \text{k}\Omega = 1\ \text{mA}$

$\therefore \quad I_C \simeq I_E = 1\ \text{mA}$

Total d.c current I_T drawn from the supply is

$$I_T = I_C + I_1 = 1\ \text{mA} + 0.82\ \text{mA} = 1.82\ \text{mA}$$

$\therefore$ D.C. power drawn from the supply is

$$P_{dc} = V_{CC} I_T = 10\text{V} \times 1.82\ \text{mA} = \mathbf{18.2\ mW}$$

Example 4.2. Determine the a.c. load power for the circuit shown in Fig. 4.3.

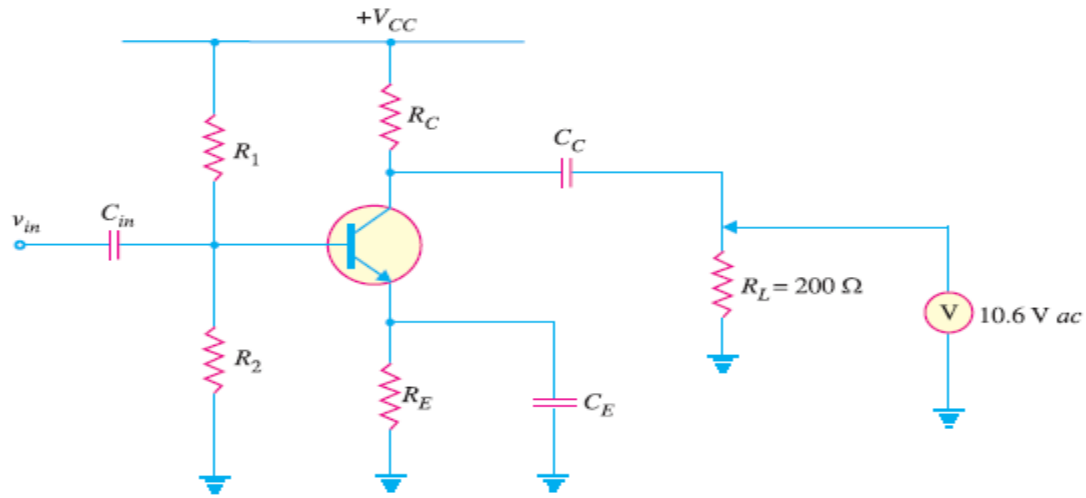


Fig. 4.3

Solution. The reading of a.c. voltmeter is 10.6V. Since a.c. voltmeters read r.m.s. voltage, we have,

$$\text{A.C. output power, } P_O = \frac{V_L^2}{R_L} = \frac{(10.6)^2}{200\ \Omega} = \mathbf{561.8\ mW}$$

Example 4.3. In an RC coupled power amplifier, the a.c. voltage across load RL (= 100 □ □) has a peak-to-peak value of 18V. Find the maximum possible a.c. load power.

Solution. The peak-to-peak voltage, VPP = 18V. Therefore, peak voltage (or maximum voltage) =

$V_{PP}/2$ and the r.m.s value, $V_L = V_{PP}/2\sqrt{2}$.

$$\therefore \quad P_{O\,(max)} = \frac{V_L^2}{R_L} = \frac{(V_{PP}/2\sqrt{2})^2}{R_L} = \frac{V_{PP}^2}{8\,R_L}$$

Here $V_{PP} = 18\text{V and } R_L = 100\Omega$

$$\therefore \quad P_{O\,(max)} = \frac{(18V)^2}{(8\times 100)\ \Omega} = 405\times 10^{-3}\ \text{W} = \mathbf{405\ mW}$$

Difference Between Voltage and Power Amplifiers:

The distinction between voltage and power amplifiers is somewhat artificial since useful power (*i.e.* product of voltage and current) is always developed in the load resistance through which current flows. The difference between the two types is really one of degree; it is a question of how much voltage and

how much power. A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level. On the other hand, a power amplifier is designed to obtain maximum output power.

1. Voltage amplifier. The voltage gain of an amplifier is given by :

$$A_v = \beta \times \frac{R_C}{R_{in}}$$

In order to achieve high voltage amplification, the following features are incorporated in such amplifiers:

(i) The transistor with high β□ (>100) is used in the circuit. In other words,those transistors are employed which have thin base.

(ii) The input resistance R_{in} of the transistor is sought to be quite low as compared to the collector load *RC*.

(iii) A relatively high load *RC* is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (j 1 mA). If the collector current is small, we can use large *RC* in the collector circuit.

2. Power amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current. In order to achieve high power amplification, the following features are incorporated in such amplifiers :

(i) The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

(ii) The base is made thicker to handle large currents. In other words, transistors with comparatively smaller are used.

(iii) Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form:

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually *R – C* coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

Example 4.4. A power amplifier operated from 12V battery gives an output of 2W. Find the maximum collector current in the circuit.

Solution.

Let I_C be the maximum collector current.

Power = battery voltage x collector current

$$2 = 12 \times I_C$$
$$I_C = \frac{2}{12} = \frac{1}{6}\text{A} = \textbf{166.7 mA}$$

This example shows that a power amplifier handles large power as well as large current.

Example 4.5. A voltage amplifier operated from a 12 V battery has a collector load of 4 kΩ.

Find the maximum collector current in the circuit.

Solution.

The maximum collector current will flow when the whole battery voltage is dropped across RC.

$$\text{Max. collector current} = \frac{\text{battery voltage}}{\text{collector load}} = \frac{12\text{ V}}{4\text{ k}\Omega} = \textbf{3 mA}$$

This example shows that a voltage amplifier handles small current.

Example 4.6. A power amplifier supplies 50 W to an 8-ohm speaker. Find

(i) a.c. output voltage
(ii) (ii) a.c. output current.

Solution.

(i) $P = V^2/R$

$\therefore$ a.c. output voltage, $V = \sqrt{PR} = \sqrt{50 \times 8} = \textbf{20 V}$

(ii) a.c. output current, $I = V/R = 20/8 = \textbf{2.5 A}$

Performance Quantities of Power Amplifiers:

As mentioned previously, the prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are: ***collector efficiency, distortion*** and ***power dissipation capability*****.**

(i) Collector efficiency. The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output. Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as **collector efficiency** and may be defined as under:

The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as collector efficiency.
Collector efficiency means as to how well an amplifier converts d.c. power from the battery into a.c. output power. For instance, if the d.c. power supplied by the battery is 10W and a.c. output power is 2W, then collector efficiency is 20%. The greater the collector efficiency, the larger is the a.c. power output. It is obvious that for power amplifiers, maximum collector efficiency is the desired goal.

(ii) Distortion. *The change of output wave shape from the input wave shape of an amplifier is known as* **distortion.** A transistor like other electronic devices is essentially a non-linear device. Therefore, whenever a signal is applied to the input of the transistor, the output signal is not exactly like the input signal *i.e*. distortion occurs. Distortion is not a problem for small signals (*i.e*. voltage amplifiers) since transistor is a linear device for small variations about the operating point. However, a power amplifier handles large signals and, therefore, the problem of distortion immediately arises. For the comparison of two power amplifiers, the one which has the less distortion is the better. We shall discuss the method of reducing distortion in amplifiers in the chapter of negative feedback in amplifiers.

(iii) Power dissipation capability. *The ability of a power transistor to dissipate heat is known as* **power dissipation capability.** As stated before, a power transistor handles large currents and heats up during operation. As any temperature change influences the operation of transistor, therefore, the transistor must dissipate this heat to its surroundings. To achieve this, generally a *heat sink* (a metal case) is attached to a power transistor case. The increased surface area allows heat to escape easily and keeps the case temperature of the transistor within permissible limits.

Classification of Power Amplifiers

Transistor power amplifiers handle large signals. Many of them are driven so hard by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle. Therefore, such amplifiers are generally classified according to their mode of operation *i.e*. the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as:

Amplifier circuits may be classified in terms of the portion of the cycle for which the active device conducts.

Class A: It is one, in which the active device conducts for the full 360°.

Class B: Conduction for 1800

Class C: Conduction for < 1800

Class AB: Conduction angle is between 1800 and 3600

(*i*) Class A power amplifier **(*ii*)** Class B power amplifier **(*iii*)** Class C power amplifier

(i) Class A power amplifier. *If the collector current flows at all times during the full cycle of the signal, the power amplifier is known as* **class A power amplifier.**

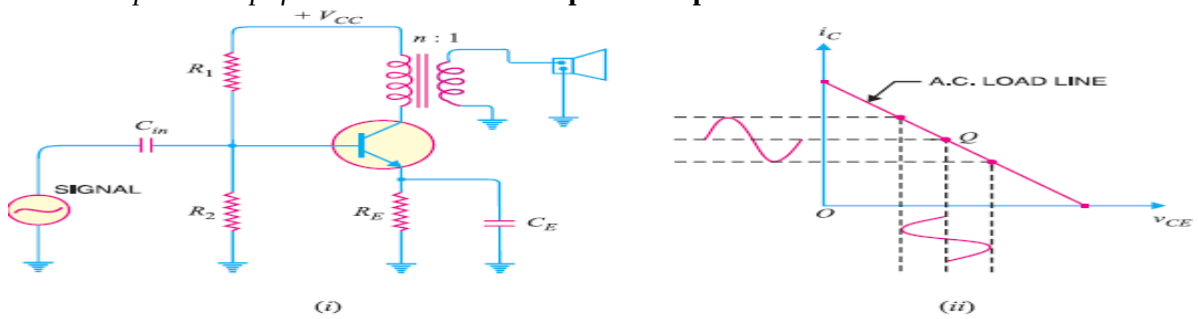


Fig. 4.4

Obviously, for this to happen, the power amplifier must be biased in such a way that no part of the signal is cut off. Fig. 4.4 (*i*) shows circuit of class *A* power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers. The use of transformer permits impedance matching, resulting in the transference of maximum power to the load *e.g*. loudspeaker. Fig. 4.4 (*ii*) shows the class *A* operation in terms of *a.c*. load line. The operating point *Q* is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion. However, they have the disadvantage of low power output and low collector efficiency (about 35%).

(ii) **Class B power amplifier.** *If the collector current flows only during the positive half-cycle of the input signal, it is called a* **class B power amplifier.** In class *B* operation, the transistor bias is so adjusted that zero signal collector current is zero *i.e*. no biasing circuit is needed at all. During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows. Fig. 4.5 shows the class *B* operation in terms of a.c. load line. Obviously, the operating point *Q* shall be located at collector cut off voltage. It is easy to see that output from a class *B* amplifier is amplified half-wave rectification. In a class *B* amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs. However, class *B* amplifiers provide higher power output and collector efficiency (50 −60%). Such amplifiers are mostly used for power amplification in push-pull

arrangement. In such an Arrangement, 2 transistors are used in class *B* operation. One transistor amplifies the positive half cycle of the signal while the other amplifies the negative half-cycle.

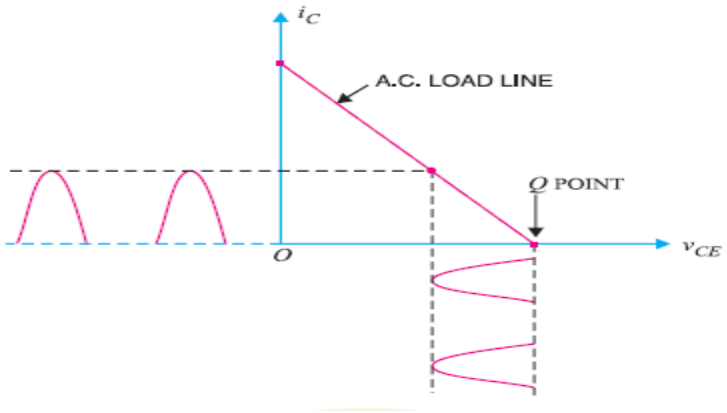
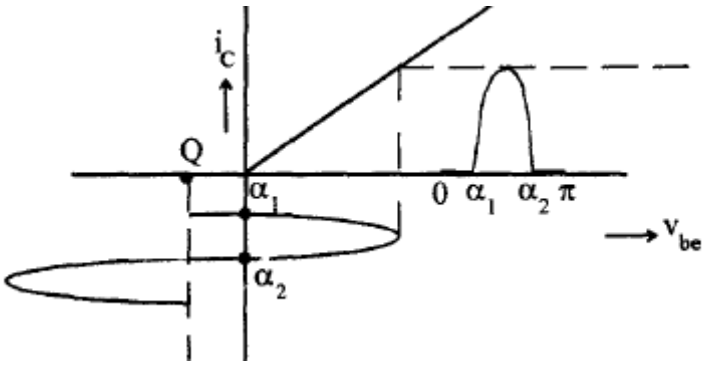


Fig. 4.5

(iii) **Class C power amplifier.** *If the collector current flows for less than half-cycle of the input signal, it is called* **class C power amplifier.** In class *C* amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts. Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers *i.e.* to amplify a narrow band of frequencies near the resonant frequency.



Expression for Collector Efficiency

For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.

Now, Collector efficiency

$$* P_o = [(0.5 \times 0.707) v_{ce\,(p-p)}] [(0.5 \times 0.707) i_{c\,(p-p)}]$$

$$= \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$$

$$\text{Collector } \eta = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8 V_{CC} I_C}$$

where *Vce* is the *r.m.s.* value of signal output voltage and *Ic* is the *r.m.s.* value of output signal current. In terms of peak-to-peak values (which are often convenient values in load-line work), the a.c. power output can be expressed as:

$$\text{Collector efficiency, } \eta = \frac{\text{a.c. power output}}{\text{d.c. power input}}$$

$$= \frac{P_o}{P_{dc}}$$

$$* P_{dc} = V_{CC} I_C$$

$$P_o = V_{ce} I_c$$

Series-Fed Class A Amplifier :

Fig. 4.6 (*i*) shows a series – fed class *A* amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency. Nevertheless, it will help the reader to understand the class *A* operation. The d.c. load line of the circuit is shown in Fig. 4.6 (*ii*). When an *ac* signal is applied to the amplifier, the output current and voltage will vary about the operating point *Q*. In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the *Q* point should be located at the centre of the *dc* load line. In that case, operating point is *IC* =*VCC*/2*RC* and *VCE* = *VCC*/2.

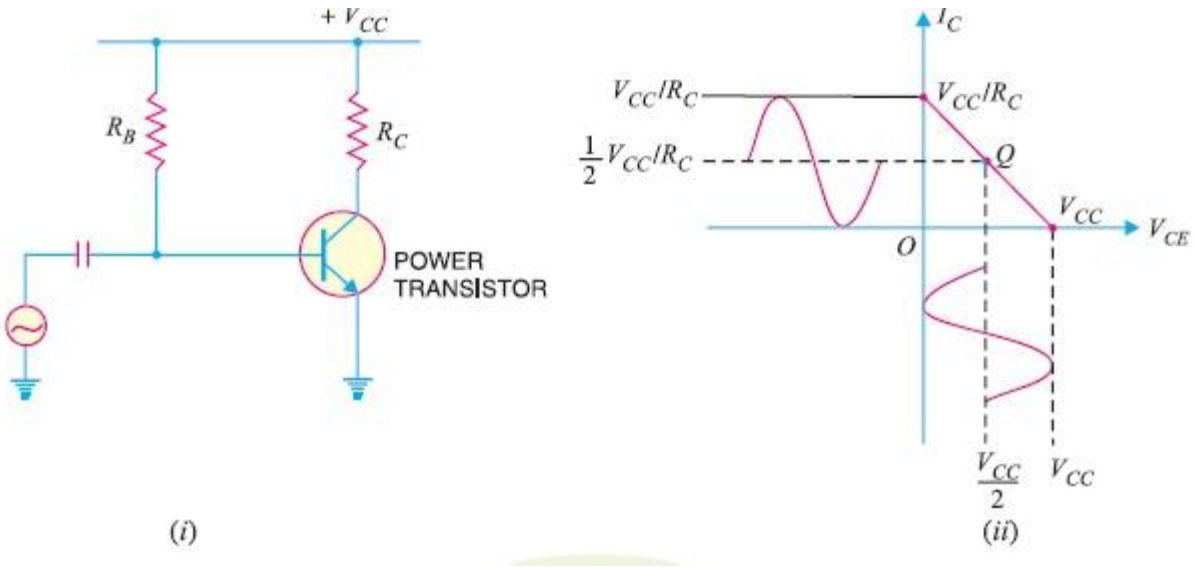


Fig. 4.6

$$\text{Maximum } v_{ce\,(p-p)} = V_{CC}$$

$$\text{Maximum } i_{c\,(p-p)} = V_{CC}/R_C$$

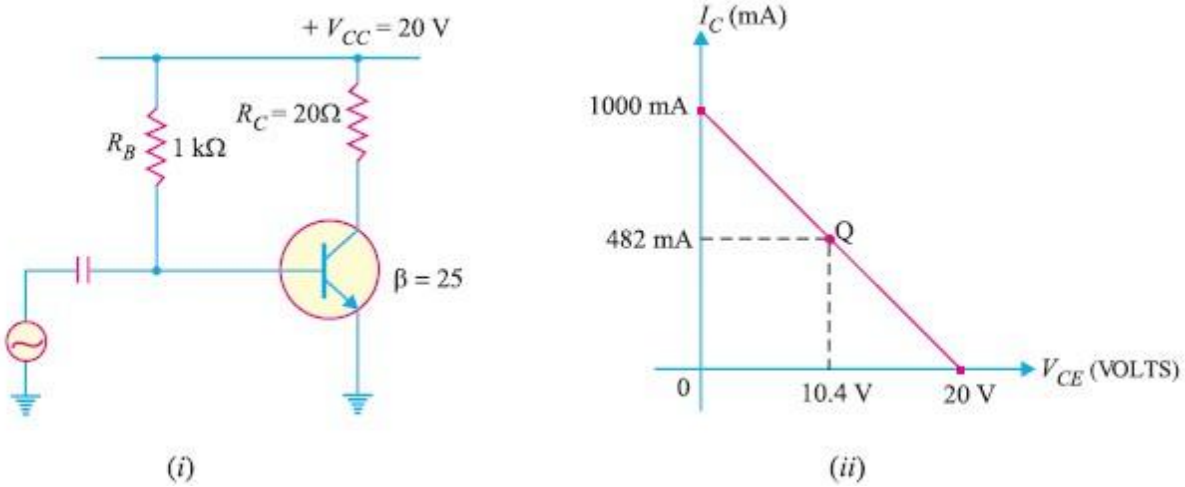
$$\text{Max. } ac \text{ output power, } P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8R_C}$$

$$\text{D.C. power supplied, } P_{dc} = V_{CC}\, I_C = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C}$$

$$\therefore \quad \text{Maximum collector } \eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = 25\%$$

Thus the maximum collector efficiency of a class *A* series-fed amplifier is 25%. In actual practice, the collector efficiency is far less than this value.

Example 4.7. Calculate the (i) output power (ii) input power and (iii) collector efficiency of the amplifier circuit shown in Fig. 12.7 (i). It is given that input voltage results in a base current of 10 mA peak.



Solution. First draw the *d.c.* load line by locating the two end points *viz.*, $I_{C\,(sat)} = V_{CC}/R_C = 20\text{ V}/20\,\Omega = 1\text{ A} = 1000\text{ mA}$ and $V_{CE} = V_{CC} = 20\text{ V}$ as shown in Fig. 12.7 (*ii*). The operating point *Q* of the circuit can be located as under :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1\,\text{k}\Omega} = 19.3\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 25\,(19.3\text{ mA}) = 482\text{ mA}$$

$$\text{Also} \quad V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - (482\text{ mA})\,(20\,\Omega) = 10.4\text{ V}$$

The operating point *Q* (10.4 V, 482 mA) is shown on the d.c. load line.

(*i*) $i_c\text{-}(peak) = \beta\, i_b\,(peak) = 25 \times (10\text{ mA}) = 250\text{ mA}$

$$\therefore \quad P_{o\,(ac)} = \frac{i_c^2(peak)}{2} R_C = \frac{(250\times10^{-3})^2}{2} \times 20 = \mathbf{0.625\text{ W}}$$

(*ii*) $P_{dc} = V_{CC} I_C = (20\text{ V})\,(482\times10^{-3}) = \mathbf{9.6\text{ W}}$

(*iii*) $\text{Collector } \eta = \frac{P_o(ac)}{P_{dc}} \times 100 = \frac{0.625}{9.6} \times 100 = \mathbf{6.5\ \%}$

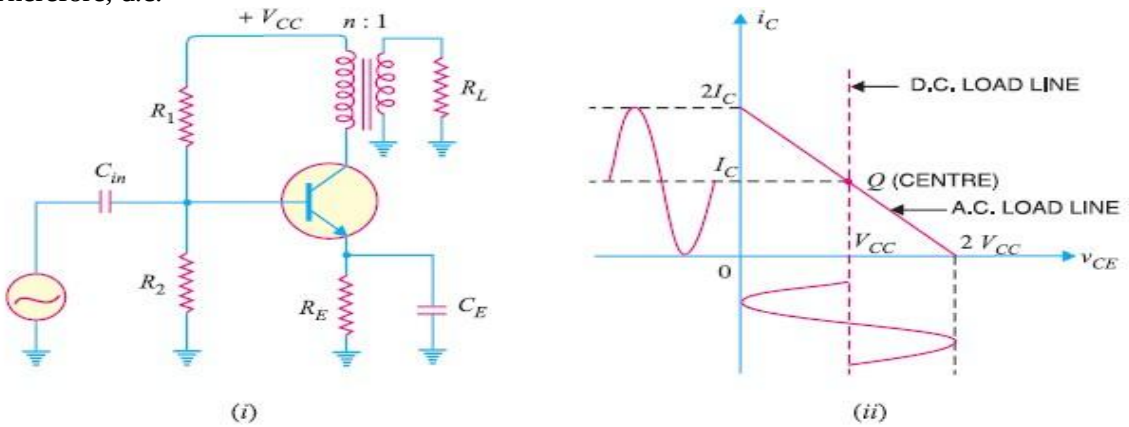
Fig. 4.7

Maximum Collector Efficiency of Transformer Coupled Class A Power Amplifier:

In class A power amplifier, the load can be either connected directly in the collector or it can be transformer coupled. The latter method is often preferred for two main reasons. First, transformer coupling permits impedance matching and secondly it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.

Fig. 4.8 (i) shows the transformer coupled class A power amplifier. In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig. 4.8 (ii). Under zero signal conditions, the effective resistance in the collector circuit is that of the primary winding of the transformer. The primary resistance has a v line is a vertical line rising from VCC as shown in Fig. 4.8 (ii). When signal is applied, the collector current will vary about the operating point Q.

In order to get maximum a.c. power output (and hence maximum collector), the peak value of collector current due to signal alone should be equal to the zero signal collector current I_C. In terms of a.c. load line, the operating point Q should be located at the centre of a.c. load line.ery small value and is assumed zero. Therefore, d.c.



load

Fig. 4.8

During the peak of the positive half-cycle of the signal, the total collector current is 2 I_C and V_{CE} = 0. During the negative peak of the signal, the collector current is zero and $V_{CE} = 2V_{CC}$.
Peak-to-peak collector-emitter voltage is $V_{CE\ (p-p)} = 2VCC$ Peak-to-peak collector current, ic (p - p) = 2 IC

$$= \frac{v_{ce(p-p)}}{R'_L} = \frac{2V_{CC}}{R'_L}$$

where RL' is the reflected value of load RL and appears in the primary of the transformer. If n (= Np/Ns) is the turn ratio of the transformer, then, RL' = n2 RL.

d.c. power input, Pdc = VCC IC

$$= I_C^2 R'_L$$

Max.a.c. output power, Po (max) =

$$P_{o\ (max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8}$$

$$= \frac{2V_{CC} \times 2I_C}{8}$$

$$= \frac{1}{2} V_{CC} I_C$$

$$= \frac{1}{2} I_C^2 R'_L$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\ (max)}}{P_{dc}} \times 100$$

$$= \frac{(1/2)\, I_C^2\, R'_L}{I_C^2\, R'_L} \times 100 = 50\%$$

Important Points About Class A Power Amplifier

(i) A *transformer coupled class *A* power amplifier has a maximum collector efficiency of 50% *i.e.*, maximum of 50% d.c. supply power is converted into a.c. power output. In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.

(ii) The power dissipated by a transistor is given by :
Pdis = *Pdc* - *Pac* where *Pdc* = available d.c. power *Pac* = available a.c. power
Clearly, in class *A* operation, the transistor must dissipate less heat when signal is applied and therefore runs cooler.

(iii) When no signal is applied to a class *A* power amplifier, *Pac* = 0.
Pdis = *Pdc*
Thus in class *A* operation, maximum power dissipation in the transistor occurs under zero signal conditions. Therefore, the power dissipation capability of a power transistor (for class *A* operation) must be atleast equal to the zero signal rating. For example, if the zero signal power dissipation of a transistor is 1

W, then transistor needs a rating of atleast 1W. If the power rating of the transistor is less than 1 W, it is likely to be damaged.

(iv) When a class *A* power amplifier is used in the final stage, it is called **single ended class A power amplifier.**

Example 4.8. A power transistor working in class A operation has zero signal power dissipation of 10 watts. If the a.c. output power is 4 watts, find :
(i) collector efficiency (ii) power rating of transistor

Solution.

Zero signal power dissipation, *Pdc* = 10 W

a.c. power output, *Po* = 4 W

(i) Collector efficiency =

$$\frac{P_o}{P_{dc}} \times 100 = \frac{4}{10} \times 100 = 40\%$$

(ii) The zero signal power represents the worst case *i.e.* maximum power dissipation in a transistor occurs under zero signal conditions.

∴ Power rating of transistor = **10 W**

It means to avoid damage, the transistor must have a power rating of atleast 10 W.

Example 4.9. A class A power amplifier has a transformer as the load. If the transformer has a turn ratio of 10 and the secondary load is 100 Ω, find the maximum a.c. power output. Given that zero signal collector current is 100 mA.

Solution.

Secondary load, $R_L = 100\ \Omega$

Transformer turn ratio, $n = 10$

Zero signal collector current, $I_C = 100\,\text{mA}$

Load as seen by the primary of the transformer is

$$R'_L = n^2 R_L = (10)^2 \times 100 = 10{,}000\ \Omega$$

$$\therefore \quad \text{Max. a.c. power output} = \frac{1}{2} I_C^2 R'_L = \frac{1}{2}\left(\frac{100}{1000}\right)^2 \times 10{,}000$$

$$= 50\ \text{W}$$

Class B Push-Pull Power Amplifier

The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. 4.9 shows the circuit of a push-pull amplifier. Two transistors *Tr*1 and *Tr*2 placed back to back are employed. Both transistors are operated in class *B* operation *i.e*. collector current is nearly zero in the absence of the signal. The centre-tapped secondary of driver transformer *T*1 supplies equal and opposite voltages to the base circuits of two transistors. The output transformer *T*2 has the centre-tapped primary winding. The supply voltage *VCC* is connected between the bases and this centre tap. The loudspeaker is connected across the secondary of this transformer.

Circuit operation: The input signal appears across the secondary *AB* of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end *A* becomes positive and end *B* negative. This will make the base-emitter junction of *Tr*1 reverse biased and that of *Tr*2 forward biased. The circuit will conduct current due to *Tr*2 only and is shown by solid arrows. Therefore, this half-cycle of the signal is amplified by *Tr*2 and appears in the lower half of the primary of output transformer. In the next half cycle of the signal, *Tr*1 is forward biased whereas *Tr*2 is reverse biased. Therefore, *Tr*1 conducts and is shown by dotted arrows. Consequently, this half- cycle of the signal is amplified by *Tr*1 and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.

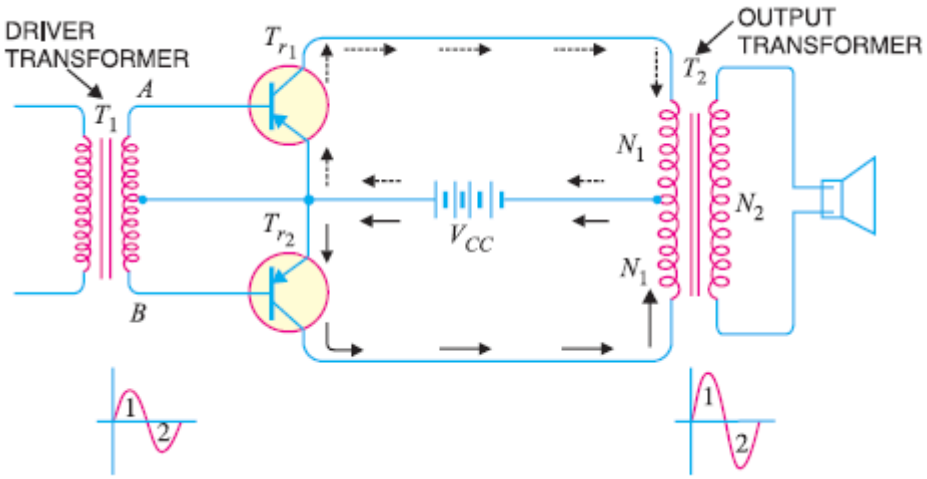


Fig. 4.9

It may be noted here that push-pull arrangement also permits a maximum transfer of power to the load through impedance matching. If *RL* is the resistance appearing across secondary of output transformer, then resistance *R'L* of primary shall become :

$$R'_L = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

where N_1 = Number of turns between either end of primary winding and centre-tap

N_2 = Number of secondary turns

Advantages

(i) The efficiency of the circuit is quite high (i.e 75%) due to class *B* operation.
(ii) A high a.c. output power is obtained.

Disadvantages

(i) Two transistors have to be used.
(ii) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.
(iii) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.
(iv) The circuit gives more distortion.
(v) Transformers used are bulky and expensive.

Maximum Efficiency for Class B Power Amplifier:

We have already seen that a push-pull circuit uses two transistors working in class *B* operation. For class *B* operation, the Q-point is located at cut-off on both d.c. and a.c. load lines. For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. 4.15 (*i*). It is clear that a.c. output voltage has a peak value of *VCE* and a.c. output current has a peak

value of *IC* (*sat*). The same information is also conveyed through the a.c. load line for the circuit [See Fig. 4.10 (*ii*)].

$$\therefore \quad \text{Peak a.c. output voltage} = V_{CE}$$

$$\text{Peak a.c. output current} = I_{C\,(sat)} = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{2\,R_L} \qquad \left(\because V_{CE} = \frac{V_{CC}}{2}\right)$$

Maximum average a.c. output power $P_{o\,(max)}$ is

$$P_{o\,(max)} = \text{Product of r.m.s. values of a.c. output voltage and a.c. output current}$$

$$= \frac{V_{CE}}{\sqrt{2}} \times \frac{I_{C\,(sat)}}{\sqrt{2}} = \frac{V_{CE}\,I_{C\,(sat)}}{2}$$

$$= \frac{V_{CC}}{2} \times \frac{I_{C\,(sat)}}{2} = \frac{V_{CE}\,I_{C\,(sat)}}{4} \qquad \left(\because V_{CE} = \frac{V_{CC}}{2}\right)$$

$$\therefore \quad P_{o\,(max)} = 0.25\,V_{CC}\,I_{C\,(sat)}$$

The input d.c. power from the supply V_{CC} is

$$P_{dc} = V_{CC}\,I_{dc}$$

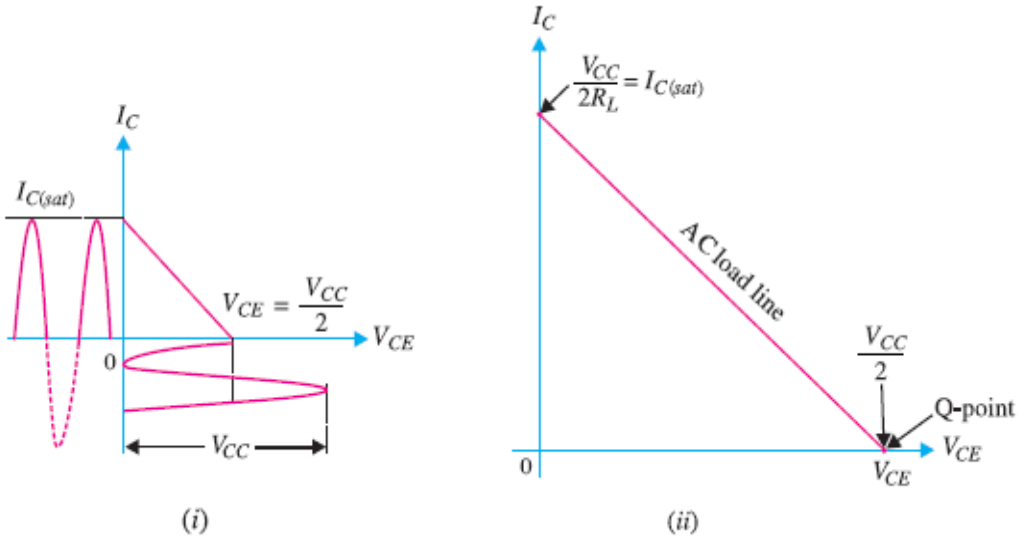


Fig. 4.10

where I_{dc} is the average current drawn from the supply *VCC*. Since the transistor is on for alternating half-cycles, it effectively acts as a half-wave rectifier.

$$\therefore \quad I_{dc} = \frac{I_{C\,(sat)}}{\pi}$$

$$\therefore \quad P_{dc} = \frac{V_{CC}\,I_{C\,(sat)}}{\pi}$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{0.25\,V_{CC}\,I_{C\,(sat)}}{(V_{CC}\,I_{C\,(sat)})/\pi} \times 100 = 0.25\pi \times 100 = 78.5\%$$

Thus the maximum collector efficiency of class *B* power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

Power dissipated by transistors. The power dissipated (as heat) by the transistors in class *B* amplifier is the difference between the input power delivered by *VCC* and the output power delivered to the load *i.e.*

$$P_{2T} = P_{dc} - P_{ac}$$

where P_{2T} = power dissipated by the two transistors

∴ Power dissipated by each transistor is

$$P_T = \frac{P_{2T}}{2} = \frac{P_{dc} - P_{ac}}{2}$$

Example 4.18. For a class B amplifier using a supply of VCC = 12V and driving a load of 8Ω, determine (i) maximum load power (ii) d.c. input power (iii) collector efficiency.

Solution. $V_{CC} = 12\text{ V}\ ;\ R_L = 8\Omega$

(i) Maximum load power, $P_{o\,(max)} = 0.25\ V_{CC}\ I_{C\,(sat)}$

$$= 0.25\ V_{CC} \times \frac{V_{CC}}{2\ R_L} \qquad \left(\because I_{C\,(sat)} = \frac{V_{CC}}{2\ R_L}\right)$$

$$= 0.25 \times 12 \times \frac{12}{2 \times 8} = \mathbf{2.25\ W}$$

(ii) D.C. input power, $P_{dc} = \frac{V_{CC}\ I_{C\,(sat)}}{\pi} = \frac{V_{CC}}{\pi} \times \frac{V_{CC}}{2\ R_L}$

$$= \frac{12}{\pi} \times \frac{12}{2 \times 8} = \mathbf{2.87\ W}$$

(iii) Collector η $= \frac{P_{o\,(max)}}{P_{dc}} \times 100 = \frac{2.25}{2.87} \times 100 = \mathbf{78.4\%}$

Example 4.19. A class B push-pull amplifier with transformer coupled load uses two transistors rated 10 W each. What is the maximum power output one can obtain at the load from the circuit?

Solution. The power dissipation by each transistor is $P_T = 10\text{W}$. Therefore, power dissipated by two transistors is $P_{2T} = 2 \times 10 = 20\text{W}$.

Now $P_{dc} = P_{o\,(max)} + P_{2T}\ ;$ Max. $\eta = 0.785$

∴ $\text{Max } \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + P_{2T}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$

or $0.785 = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$

or $0.785\ P_{o\,(max)} + 15.7 = P_{o\,(max)}$

or $P_{o\,(max)}\ (1 - 0.785) = 15.7$

∴ $P_{o\,(max)} = \frac{15.7}{1 - 0.785} = \frac{15.7}{0.215} = \mathbf{73.02\ W}$

Example 4.20. A class B amplifier has an efficiency of 60% and each transistor has a rating of 2.5W. Find the a.c. output power and d.c. input power

Solution. The power dissipated by each transistor is $P_T = 2.5\text{W}$.

Therefore, power dissipated by the two transistors is $P_{2T} = 2 \times 2.5 = 5\text{W}$.

Now $P_{dc} = P_{ac} + P_{2T}$; $\eta = 0.6$

$\therefore$ $\eta = \frac{P_{ac}}{P_{dc}} = \frac{P_{ac}}{P_{ac} + P_{2T}}$

or $0.6 = \frac{P_{ac}}{P_{ac} + 5}$ or $0.6\ P_{ac} + 3 = P_{ac}$

$\therefore$ $P_{ac} = \frac{3}{1 - 0.6} = \frac{3}{0.4} = \mathbf{7.5\ W}$

and $P_{dc} = P_{ac} + P_{2T} = 7.5 + 5 = \mathbf{12.5\ W}$

Example 4.21. A class B amplifier uses VCC = 10V and drives a load of 10Ω. Determine the end point values of the a.c. load line.

Solution.

$$I_{C\,(sat)} = \frac{V_{CC}}{2R_L} = \frac{10\text{V}}{2(10\ \Omega)} = \mathbf{500\ mA}$$

This locates one end-point of the a.c. load line on the collector current axis.

$$V_{CE\,(off)} = \frac{V_{CC}}{2} = \frac{10\text{V}}{2} = \mathbf{5V}$$

Complementary-Symmetry Amplifier:

By complementary symmetry is meant a principle of assembling push-pull class *B* amplifier without requiring centre-tapped transformers at the input and output stages. Fig. 4.11 shows the transistor push-pull amplifier using complementary symmetry. It employs one *npn* and one *pnp* transistor and requires no centre-tapped transformers. The circuit action is as follows. During the positive-half of the input signal, transistor *T*1 (the *npn* transistor) conducts current while *T*2 (the *pnp* transistor) is cut off. During the negative half-cycle of the signal, *T*2 conducts while *T*1 is cut off. In this way, *npn* transistor amplifies the positive half-cycles of the signal while the *pnp* transistor amplifies the negative half-cycles of the signal. Note that we generally use an output transformer (not centre-tapped) for impedance matching.

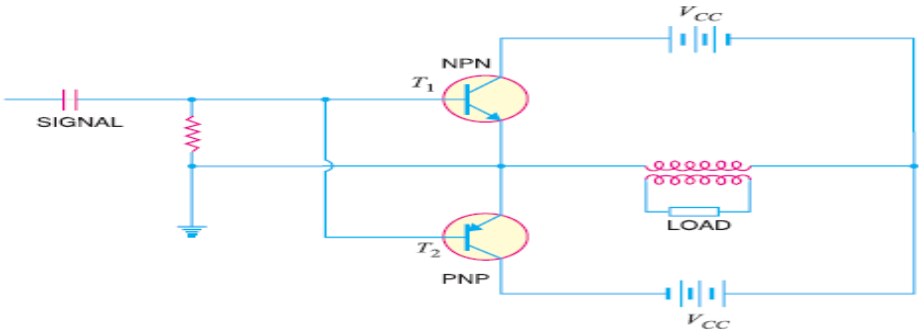


Fig. 4.11

Advantages

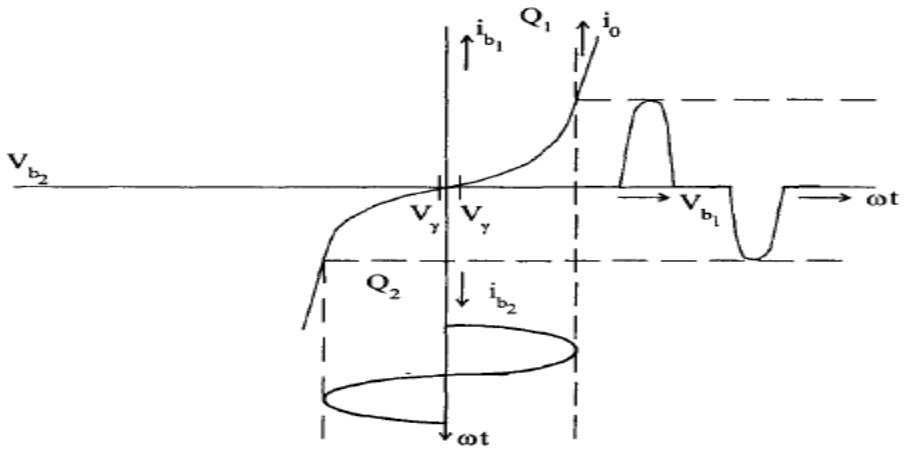
(i) This circuit does not require transformer. This saves on weight and cost.
(ii) Equal and opposite input signal voltages are not required.

Disadvantages

(i) It is difficult to get a pair of transistors (*npn* and *pnp*) that have similar characteristics.
(ii) We require both positive and negative supply voltages.

DISTORTION:

Let i_{b1} Vc, V_{b1} be the input characteristic of the first transistor and i_{b2}, Vs, V_{b2} is the input characteristic of the second transistor. Vy is the cut)n voltage. These are t6e two tiansistors of the class B push pull amplifier. Now the base input voltage being given to the transistor is sinusoidal, i.e., base drive is sinusoidal. So because of the *cut in voltage,* even though input voltage is present, output will not be transmitted or there is distortion in the output current of the transistor. This is known as *crossover distortion.* But this will not occur if the base current drive is sinusoidal. Since in the graphical analysis the input current is taken in the I quadrant. No distortion if the operating point is in the active region. Cross-over distortion can also be laminated in class AB operation. A small stand by current flows at zero excitation. The input signal is shifted by constant DC bias so that the input signal is shifted by an amount V γ.



Thermal Runaway:

All semiconductor devices are very sensitive to temperature variations. If the temperature of a transistor exceeds the permissible limit, the transistor may be *permanently damaged. Silicon transistors can withstand temperatures up to 250ºC while the germanium transistors can withstand temperatures up to 100ºC.

There are two factors which determine the operating temperature of a transistor *viz*.

(i) Surrounding temperature and
(ii) Power dissipated by the transistor.

When the transistor is in operation, almost the entire heat is produced at the collector-base junction. This power dissipation causes the junction temperature to rise. This in turn increases the collector current since more electron-hole pairs are generated due to the rise in temperature. This produces increased power dissipation in the transistor and consequently a further rise in temperature. Unless adequate cooling is provided or the transistor has built-in temperature compensation circuits to prevent excessive collector current rise, the junction temperature will continue to increase until the maximum permissible temperature is exceeded. If this situation occurs, the transistor will be permanently damaged.

The unstable condition where, owing to rise in temperature, the collector current rises and continues to increase is known as **thermal runaway.**

Thermal runaway must always be avoided. If it occurs, permanent damage is caused and the transistor must be replaced.

Tuned Amplifiers

INTRODUCTION:

An audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies. However, sometimes it is desired that an amplifier should be selective *i.e*. it should select a desired frequency or narrow band of frequencies for amplification. For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side. Therefore, the use of tuned circuits in conjunction with a transistor makes possible the selection and efficient amplification of a particular desired radio frequency. Such an amplifier is called a *tuned amplifier*. In this chapter, we shall focus our attention on transistor tuned amplifiers and their increasing applications in high frequency electronic circuits.

Advantages of Tuned Amplifiers

In high frequency applications, it is generally required to amplify a single frequency, rejecting all other frequencies present. For such purposes, tuned amplifiers are used. These amplifiers use tuned parallel circuit as the collector load and offer the following advantages:

(i) Small power loss. A tuned parallel circuit employs reactive components *L* and *C*. Consequently, the power loss in such a circuit is quite low. On the other hand, if a resistive load is used in the collector circuit, there will be considerable loss of power. Therefore, tuned amplifiers are highly efficient.

(ii) High selectivity. A tuned circuit has the property of selectivity *i.e*. it can select the desired frequency for amplification out of a large number of frequencies simultaneously impressed upon it. For instance, if a mixture of frequencies including *fr* is fed to the input of a tuned amplifier, then maximum amplification occurs for *fr*. For all other frequencies, the tuned circuit offers very low impedance and hence these are amplified to a little extent and may be thought as rejected by the circuit. On the other hand, if we use resistive load in the collector, all the frequencies will be amplified equally well *i.e*. the circuit will not have the ability to select the desired frequency.

(iii) Smaller collector supply voltage. Because of little resistance in the parallel tuned circuit, it requires small collector supply voltage VCC. On the other hand, if a high load resistance is used in the collector for amplifying even one frequency, it would mean large voltage drop across it due to zero signal collector current. Consequently, a higher collector supply will be needed.

Why not Tuned Circuits for Low Frequency Amplification?

The tuned amplifiers are used to select and amplify a specific high frequency or narrow band of frequencies. The reader may be inclined to think as to why tuned circuits are not used to amplify low frequencies. This is due to the following reasons:

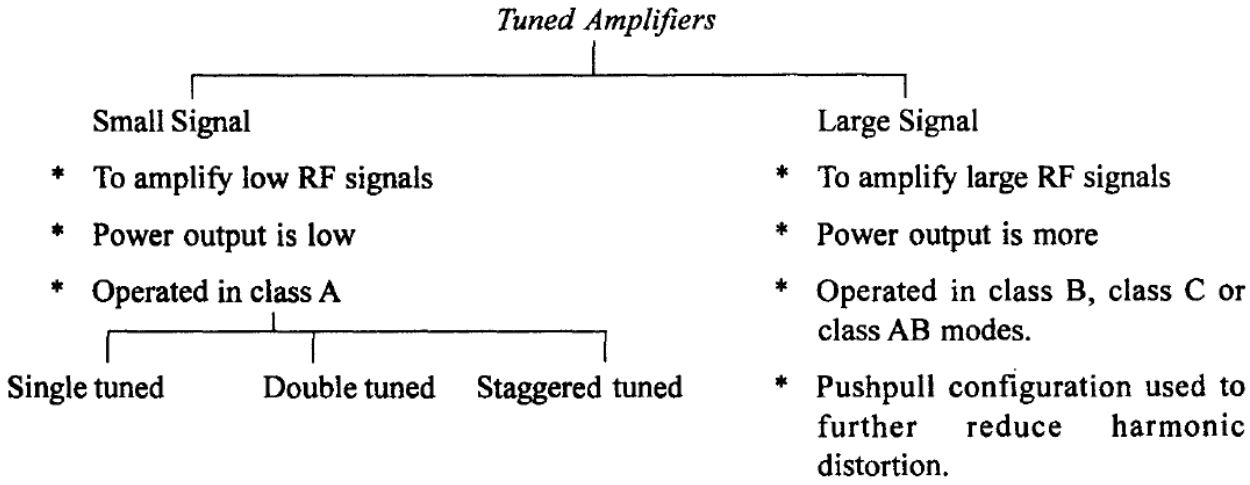
(i) *Low frequencies are never single.* A tuned amplifier selects and amplifies a single frequency. However, the low frequencies found in practice are the audio frequencies which are a mixture of frequencies from 20 Hz to 20 kHz and are not single. It is desired that all these frequencies should be equally amplified for proper reproduction of the signal. Consequently, tuned amplifiers cannot be used for the purpose.

(ii) *High values of L and C.* The resonant frequency of a parallel tuned circuit is given by;

$$fr = 1/2\pi\, LC$$

For low frequency amplification, we require large values of L and C. This will make the tuned Circuit bulky and expensive. It is worthwhile to mention here that *R-C* and transformer coupled Amplifiers, which are comparatively cheap, can be conveniently used for low frequency applications.

Classification:



Tuned Amplifiers:

Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.** Tuned amplifiers are mostly used for the amplification of high or radio frequencies.

It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single.

Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies. Fig. 4.12 shows the circuit of a simple transistor tuned amplifier. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at *resonant frequency* and very small impedance at all other frequencies. If the signal has the same frequency as the resonant frequency of *LC* circuit, large amplification will result due to high impedance of *LC* circuit at this frequency. When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while *rejecting all others. Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.

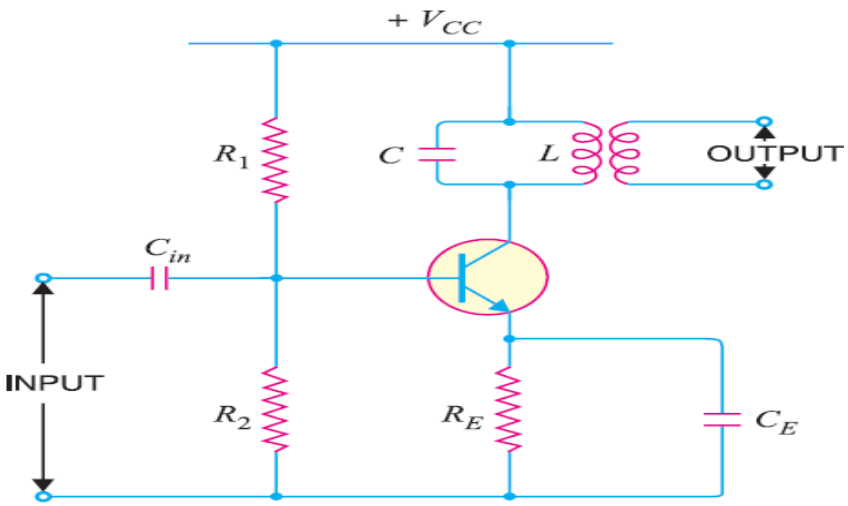


Fig. 4.12

Distinction between Tuned Amplifiers and other Amplifiers:

We have seen that amplifiers (*e.g.*, voltage amplifier, power amplifier *etc.*) provide the constant gain over a limited band of frequencies *i.e.*, from lower cut-off frequency $f1$ to upper cut-off frequency $f2$. Now bandwidth of the amplifier, $BW = f2 - f1$. The reader may wonder, then, what distinguishes a tuned amplifier from other amplifiers? The difference is that tuned amplifiers are designed to have specific, usually narrow bandwidth. This point is illustrated in Fig.4.13. Note that *BWS* is the bandwidth of standard frequency response while *BWT* is the bandwidth of the tuned amplifier. In many applications, the narrower the bandwidth of a tuned amplifier, the better it is.

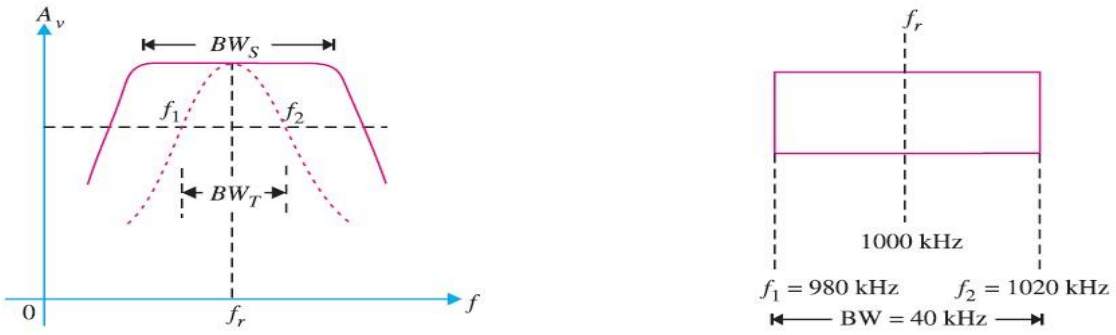


Fig. 4.13

Illustration. Consider a tuned amplifier that is designed to amplify only those frequencies that are within ± 20 kHz of the central frequency of 1000 kHz (*i.e.*, *fr* = 1000 kHz). Here [See Fig. 5.3], *f*1 = 980 kHz, *fr* = 1000 kHz, *f*2 = 1020 kHz, *BW* = 40 kHz

This means that so long as the input signal is within the range of 980 – 1020 kHz, it will be amplified. If the frequency of input signal goes out of this range, amplification will be drastically reduced.

Analysis of Parallel Tuned Circuit:

A parallel tuned circuit consists of a capacitor *C* and inductor *L* in parallel as shown in Fig. 4.14 (*i*).In practice, some resistance *R* is always present with the coil. If an alternating voltage is applied across this parallel circuit, the frequency of oscillations will be that of the applied voltage. However, if the frequency of applied voltage is equal to the natural or resonant frequency of *LC* circuit, then *electrical resonance* will occur. Under such conditions, the impedance of the tuned circuit becomes maximum and the line current is minimum. The circuit then draws just enough energy from a.c. supply necessary to overcome the losses in the resistance *R*.

Parallel resonance. A parallel circuit containing reactive elements (*L* and *C)* is *resonant when the circuit power factor is MODULEy *i.e*. applied voltage and the supply current are in phase. The phasor diagram of the parallel circuit is shown in Fig. 4. 14 (*ii*). The coil current *IL* has two rectangular components *viz* active component *IL* cos □*L* and reactive component *IL* sin w*L*. This parallel circuit will resonate when the circuit power factor is MODULEy. This is possible only when the net reactive component of the circuit current is zero *i.e*.

$$I_C - I_L \sin \phi_L = 0$$
$$I_C = I_L \sin \phi_L$$

Resonance in parallel circuit can be obtained by changing the supply frequency. At some frequency *fr* (called resonant frequency), *IC* = *IL* sin w*L* and resonance occurs.

Resonant frequency. The frequency at which parallel resonance occurs (*i.e.* reactive component of circuit current becomes zero) is called the *resonant frequency fr*.

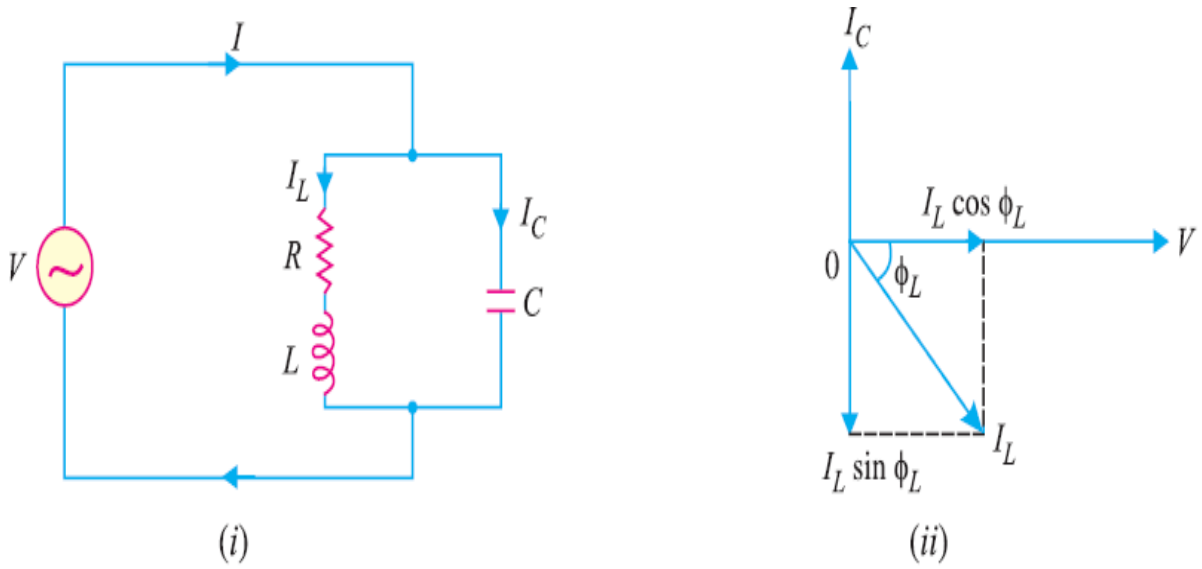


Fig. 4.14

At parallel resonance, we have, $I_C = I_L \sin \phi_L$

Now $I_L = V/Z_L$; $\sin \phi_L = X_L/Z_L$ and $I_C = V/X_C$

$$\therefore \quad \frac{V}{X_C} = \frac{V}{Z_L} \times \frac{X_L}{Z_L}$$

$$\text{or} \quad X_L X_C = Z_L^2$$

$$\text{or} \quad \frac{\omega L}{\omega C} = Z_L^2 = R^2 + X_L^2 \qquad ...(i)$$

$$\text{or} \quad \frac{L}{C} = R^2 + (2\pi f_r L)^2$$

$$\text{or} \quad (2\pi f_r L)^2 = \frac{L}{C} - R^2$$

$$\text{or} \quad 2\pi f_r L = \sqrt{\frac{L}{C} - R^2}$$

$$\text{or} \quad f_r = \frac{1}{2\pi L}\sqrt{\frac{L}{C} - R^2}$$

$$\therefore \quad \text{Resonant frequency, } f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \qquad ...(ii)$$

If coil resistance R is small (as is generally the case), then,

$$f_r = \frac{1}{2\pi\sqrt{L\,C}} \qquad ...(iii)$$

The resonant frequency will be in Hz if *R*, *L* and *C* are in ohms, Henry and farad respectively.

Note. If in the problem, the value of *R* is given, then eq. (*ii*) should be used to find *fr*. However, if *R* is not given, then eq. (*iii*) may be used to find *fr*.

Characteristics of Parallel Resonant Circuit:

It is now desirable to discuss some important characteristics of parallel resonant circuit.

(i) Impedance of tuned circuit. The impedance offered by the parallel *LC* circuit is given by the supply voltage divided by the line current *i.e.*, *V/I*. Since at resonance, line current is minimum, therefore, impedance is maximum at resonant frequency. This fact is shown by the impedance-frequency curve of Fig 4.15. It is clear from impedance-frequency curve that impedance rises to a steep peak at resonant frequency *fr*. However, the impedance of the circuit decreases rapidly when the frequency is changed above or below the resonant frequency. This characteristic of parallel tuned circuit provides it the selective properties *i.e.* to select the resonant frequency and reject all others.

$$\text{Line current, } I = I_L \cos \phi_L$$

$$\text{or} \quad \frac{V}{Z_r} = \frac{V}{Z_L} \times \frac{R}{Z_L}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{Z_L^2}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{L/C} = \frac{CR}{L}$$

$$\left[\because Z_L^2 = \frac{L}{C} \text{ from eq. } (i)\right]$$

$$\therefore \quad \text{Circuit impedance, } Z_r = \frac{L}{CR}$$

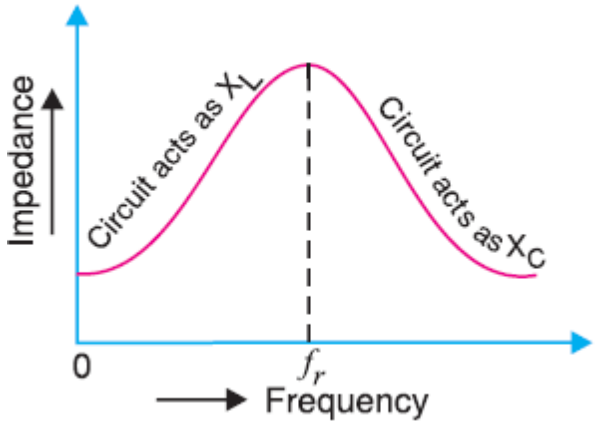


Fig. 4.15

Thus at parallel resonance, the circuit impedance is equal to *L/CR. It may be noted that Zr will be in ohms if R, L and C are measured in ohms, henry and farad respectively.

(i) Circuit Current. At parallel resonance, the circuit or line current I is given by the applied voltage divided by the circuit impedance Zr *i.e.*,

$$\text{Line current, } I = \frac{V}{Z_r} \qquad \text{where } Z_r = \frac{L}{CR}$$

Because Zr is very high, the line current I will be very small.

(ii) Quality factor Q. It is desired that resonance curve of a parallel tuned circuit should be as sharp as possible in order to provide selectivity. The sharp resonance curve means that impedance falls rapidly as the frequency is varied from the resonant frequency. The smaller the resistance of coil, the more sharp is the resonance curve. This is due to the fact that a small resistance consumes less power and draws a relatively small line current. The ratio of inductive reactance and resistance of the coil at resonance, therefore, becomes a measure of the quality of the tuned circuit. This is called *quality factor* and may be defined as under :

The ratio of inductive reactance of the coil at resonance to its resistance is known as ****quality factor Q** *i.e.*,

$$Q = \frac{X_L}{R} = \frac{2\pi f_r L}{R}$$

The quality factor *Q* of a parallel tuned circuit is very important because the sharpness of resonance curve and hence selectivity of the circuit depends upon it. The higher the value of *Q*, the more selective is the tuned circuit. Fig. 5.6 shows the effect of resistance *R* of the coil on the sharpness of the resonance curve. It is clear that when the resistance is small, the resonance curve is very sharp. However, if the coil has large resistance, the resonance curve is less sharp. It may be emphasized that where high selectivity is desired, the value of *Q* should be very large.

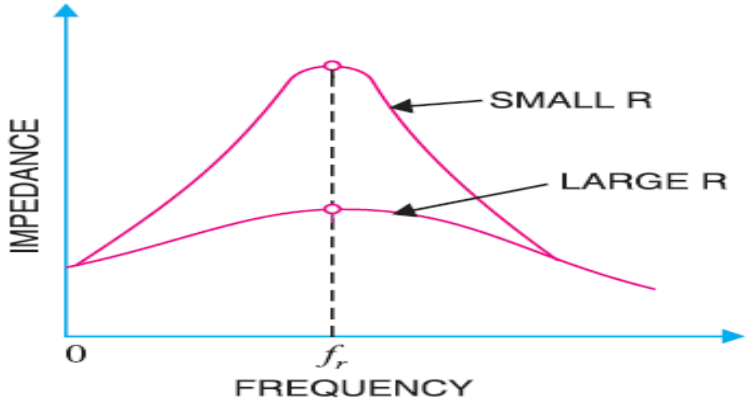


Fig. 4.16

Two things are worth noting. First, *Zr* (= *L*/*CR*) is a pure resistance because there is no frequency term present. Secondly, the value of *Zr* is very high because the ratio *L*/*C* is very large at parallel resonance.

** Strictly speaking, the *Q* of a tank circuit is defined as the ratio of the energy stored in the circuit to the energy lost in the circuit *i.e.*,

$$Q = \frac{\text{Energy stored}}{\text{Energy lost}} = \frac{\text{Reactive Power}}{\text{Resistive Power}} = \frac{I_L^2 X_L}{I_L^2 R} \quad \text{or} \quad Q = \frac{X_L}{R}$$

Example 5.1. A parallel resonant circuit has a capacitor of 250pF in one branch and inductance of 1.25mH plus a resistance of 10ohm□ in the parallel branch. Find (i) resonant frequency (ii) impedance of the circuit at resonance (iii) Q-factor of the circuit.

Solution.

$R = 10\Omega$; $L = 1.25 \times 10^{-3}$H; $C = 250 \times 10^{-12}$ F **Fig. 15.6**

(i) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}} \text{ Hz}$$

$$= 284.7 \times 10^3 \text{ Hz} = \mathbf{284.7\ kHz}$$

(ii) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{1.25 \times 10^{-3}}{250 \times 10^{-12} \times 10} = 500 \times 10^3\ \Omega$$

$$= \mathbf{500\ k\Omega}$$

(iii) Quality factor of the circuit is

$$Q = \frac{2\pi f_r L}{R} = \frac{2\pi (284.7 \times 10^3) \times 1.25 \times 10^{-3}}{10} = \mathbf{223.6}$$

Example 5.2. A parallel resonant circuit has a capacitor of 100 pF in one branch and inductance of 100 μH plus a resistance of 10 ohm□ in parallel branch.If the supply voltage is 10 V, calculate

(i) resonant frequency (ii) impedance of the circuit and line current at resonance.

Solution.

$R = 10\,\Omega$, $L = 100 \times 10^{-6}$ H ; $C = 100 \times 10^{-12}$ F

(i) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{100 \times 10^{-6} \times 100} - \frac{10^2}{(100 \times 10^{-6})^2}} \text{ Hz}$$

$$= 1592.28 \times 10^3 \text{ Hz} = \mathbf{1592.28\ kHz}$$

(ii) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{L}{C} \times \frac{1}{R} = \frac{100 \times 10^{-6}}{100 \times 10^{-12}} \times \frac{1}{R}$$

$$= 10^6 \times \frac{1}{R} = 10^6 \times \frac{1}{10} = 10^5\ \Omega = \mathbf{0.1\ M\Omega}$$

Note that the circuit impedance *Zr* is very high at resonance. It is because the ratio *L*/*C* is very large at resonance.Line current at resonance is

$$I = \frac{V}{Z_r} = \frac{10\ \text{V}}{10^5\ \Omega} = \mathbf{100\ \mu A}$$

Example 5.3. The *dynamic impedance of a parallel resonant circuit is 500 k□ . The circuit consists of a 250 pF capacitor in parallel with a coil of resistance 10ohm. Calculate (i) the coil inductance (ii) the resonant frequency and (iii) Q-factor of the circuit.

Solution.

(*i*) Dynamic impedance, $Z_r = \dfrac{L}{CR}$

$\therefore$ Inductance of coil, $L = Z_r CR = (500 \times 10^3) \times (250 \times 10^{-12}) \times 10$

$= 1.25 \times 10^{-3}$ H = **1.25 mH**

(*ii*) Resonant frequency, $f_r = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC} - \dfrac{R^2}{L^2}}$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}}$$

$= 284.7 \times 10^3$ Hz = **284.7 kHz**

(*iii*) Q-factor of the circuit $= \dfrac{2\pi f_r L}{R} = \dfrac{2\pi \times (284.7 \times 10^3) \times (1.25 \times 10^{-3})}{10} = \mathbf{223.6}$

Frequency Response of Tuned Amplifier:

The voltage gain of an amplifier depends upon □ , input impedance and effective collector load. In a tuned amplifier, tuned circuit is used in the collector. Therefore, voltage gain of such an amplifier is given by:

$$\text{Voltage gain} = \frac{\beta\, Z_C}{Z_{in}}$$

where Z_C = effective collector load

Z_{in} = input impedance of the amplifier

The value of *ZC* and hence gain strongly depends upon frequency in the tuned amplifier. As Z_C is maximum at resonant frequency, therefore, voltage gain will be maximum at this frequency. The value of Z_C and gain decrease as the frequency is varied above and below the resonant frequency. Fig. 4.17 shows the frequency response of a tuned amplifier. It is clear that voltage gain is maximum at resonant frequency and falls off as the frequency is varied in either direction from resonance.

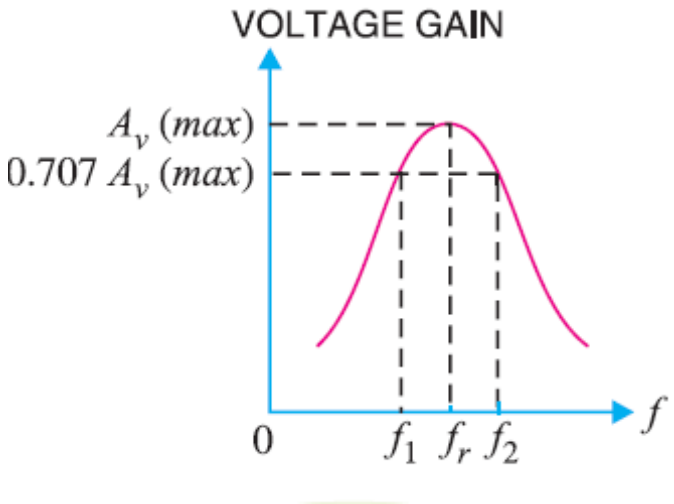


Fig. 4.17

Bandwidth. The range of frequencies at which the voltage gain of the tuned amplifier falls to 70.7 % of the maximum gain is called its *bandwidth*. Referring to Fig.4.17, the bandwidth of tuned amplifier is $f1 - f2$. The amplifier will amplify nicely any signal in this frequency range. The bandwidth of tuned amplifier depends upon the value of *Q* of *LC* circuit *i.e*. upon the sharpness of the frequency response. The greater the value of *Q* of tuned circuit, the lesser is the bandwidth of the amplifier and *vice-versa*. In practice, the value of *Q* of *LC* circuit is made such so as to permit the amplification of desired narrow band of high frequencies. The practical importance of bandwidth of tuned amplifiers is found in communication system. In radio and TV transmission, a very high frequency wave, called *carrier wave* is used to carry the audio or picture signal. In radio transmission, the audio signal has a frequency range of 10 kHz. If the carrier wave frequency is 710 kHz, then the resultant radio wave has a frequency range *between (710 –5) kHz and (710 +5) kHz. Consequently, the tuned amplifier must have a bandwidth of 705 kHz to 715 kHz (*i.e*. 10 kHz). The *Q* of the tuned circuit should be such that bandwidth of the amplifier lies in this range.

Relation between Q and Bandwidth

The quality factor *Q* of a tuned amplifier is equal to the ratio of resonant frequency (*fr*) to bandwidth (*BW*) *i.e.*,

$$Q = \frac{f_r}{BW}$$

The Q of an amplifier is determined by the circuit component values. It may be noted here that Q of a tuned amplifier is generally greater than 10. When this condition is met, the resonant frequency at parallel resonance is approximately given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Example 5.4. The Q of a tuned amplifier is 60. If the resonant frequency for the amplifier is 1200 kHz, find (i) bandwidth and (ii) cut-off frequencies.

Solution.

(*i*) $$BW = \frac{f_r}{Q} = \frac{1200\text{ kHz}}{60} = \mathbf{20\text{ kHz}}$$

(*ii*) Lower cut-off frequency, $f_1 = 1200 - 10 = \mathbf{1190\text{ kHz}}$

Upper cut-off frequency, $f_2 = 1200 + 10 = \mathbf{1210\text{ kHz}}$

Example 5.5. A tuned amplifier has maximum voltage gain at a frequency of 2 MHz and the bandwidth is 50 kHz. Find the Q factor.

Solution. The maximum voltage gain occurs at the resonant frequency. Therefore, fr = 2 MHz = 2×10^6 Hz and BW = 50 kHz = 50×10^3 Hz.

Now

$$BW = \frac{f_r}{Q}$$

$$Q = \frac{f_r}{BW} = \frac{2 \times 10^6}{50 \times 10^3} = \mathbf{40}$$

MODULE V

MULTIVIBRATORS

MULTIVIBRATORS

Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using transistors.

Multi means many; *vibrator* means oscillator. A circuit which can oscillate at a number of frequencies is called a *multivibrator*. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

In this chapter we will discuss multivibrators with two-stage regenerative amplifiers.

They have two cross-coupled inverters, i.e. the output of the first stage is coupled to the input of the second stage and the output of the second stage is coupled to the input of the first stage. In bistable circuits both the coupling elements are resistors (i.e. both are dc couplings). In monostable circuits, one coupling element is a capacitor (ac coupling) and the other coupling element is a resistor (dc coupling) In astable multivibrators both the coupling elements are capacitors (i.e. both are ac couplings).

A bistable multivibrator requires a triggering signal to change from one stable state to another. It requires another triggering signal for the reverse transition. A monostable multivibrator requires a triggering signal to change from the stable state to the quasi stable state but no triggering signal is required for the reverse transition, i.e. to bring it from the quasi stable state to the stable state. The astable multivibrator does not require any triggering signal at all. It keeps changing from one quasi stable state to another quasi stable state on its own the moment it is connected to the supply.

A bistable multivibrator is the basic memory element. It is used to perform many digital operations such as counting and storing of binary data. It also finds extensive applications in the generation and processing of pulse type waveforms. The monostable multivibrator finds extensive applications in pulse circuits. Mostly it is used as a gating circuit or a delay circuit. The astable circuit is used as a

master oscillator to generate square waves. It is often a basic source of fast waveforms. It is a free running oscillator. It is called a *square wave generator.* It is also termed a *relaxation oscillator.*

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

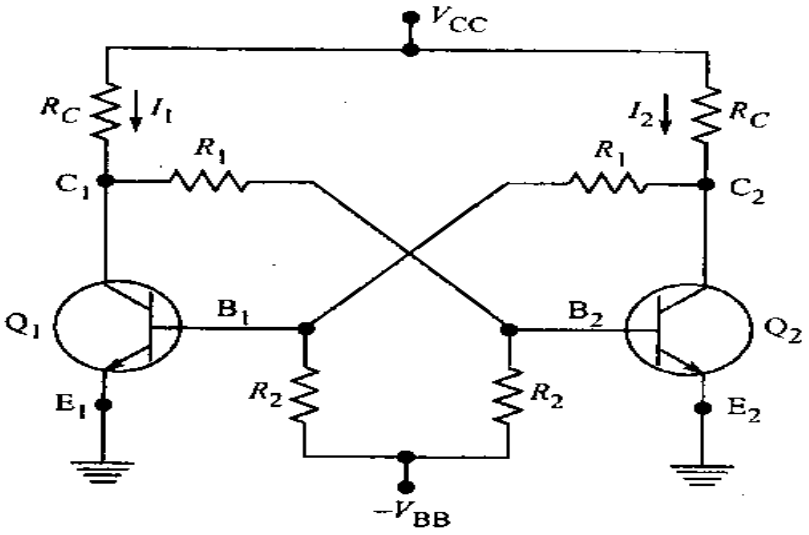
A FIXED-BIAS BISTABLE MULTIVIBRATOR

Figure 4.1 shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states, transistor Q[is ON (i.e. in saturation) and Q_2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q_2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents /[and 7_2 and suppose there is a minute fluctuation in the current *1*\~—let us say it increases by a small amount—then the voltage at the collector of Qi decreases. This will result in a decrease in voltage at the base of Q_2. So Q_2 conducts less and $/_2$ decreases and hence the potential at the collector of Q_2 increases. This results in an increase in the base potential of *Qi.*

So, Qi conducts still more and /[is further increased and the potential at the collector of Q_t is further reduced, and so on. So, the current *I*\ keeps on increasing and the current $/_2$ keeps on decreasing till $Q_($ goes into saturation and Q_2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one.*A stable*

state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than MODULEy is satisfied.

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may be so much that the device operating in the active region may gc into cut-off, and with both the devices in cut-off the circuit will be useless.



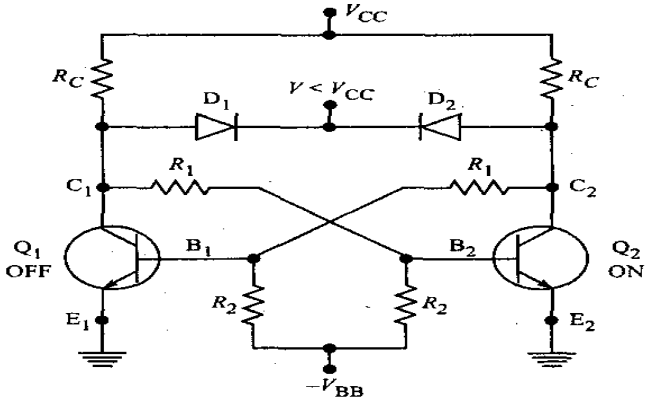
Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage Vcc will appear across the transistor that is OFF. Since this supply voltage Vcc is to be reasonably smaller than the collector breakdown voltage SVce. Vcc *s restricted to a maximum of a few tens of volts. Under saturation conditions the collector current Ic is maximum. Hence RC must be chosen so that this value of 7C (= VCC/^G) does not exceed the maximum permissible limit. The values of R\, /?2 and VBB must be selected such that in one stat>le state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing Vw is the change in collector voltage resulting from a transistor going from one state to the other, i.e. Vw = VCi - ^C2- If the loading caused by RI can be neglected, then the collector voltage of the OFF transistor is Vcc.

Since the collector saturation voltage is few tenths of a volt, then the swing Vw = Vcc, independently of RQ- The component values, the supply voltages and the values of /CBO, h^, VBE(sat), and VCE(sat) are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage VC1 of the OFF transistor. This will result in reduction of the output voltage swing. A reduced VC[will decrease 7B2 and it is possible that Q2 may not be driven into saturation- Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one-transistor remains in saturation while the other is in cut-off. Since the resistor Rl also loads the OFF transistor, to reduce loading, the value of R] should be as large as possible compared to the value of Rc. But to ensure a loop gain in excess of MODULEy during the transition between the states, R^ should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing V\v = V, arid a constant base saturation current IB2 can be obtained by clamping the collectors to an auxiliary voltage V < Vcc through the diodes DI and D2 as indicated in Figure 4.2. As Qi cuts OFF, its collector voltage rises and when it reaches V, the "collector catching diode" D| conducts and clamps the output to V.



Transistor as an ON-OFF switch

In digital circuits transistors operate either in the cut-off region or in the saturation region. Specially designed transistors called switching transistors with negligible active region are used. In the cut-off region the transistor does not conduct and acts as a open switch. In the saturation region the transistor conducts heavily and acts as a closed switch-In a binary which uses two cross-coupled transistors, each of the transistors is alternately cut-off and driven into saturation. Because of regenerative feedback provided both the transistors cannot be.ON or both cannot be OFF simultaneously. When one transistor is ON, the other is OFF and vice versa.

Standard specifications

In the cut-off region, i.e. for the OFF state

V_{BE} (cut-off) : $\leq$ 0 V for silicon transistor
$\leq$ – 0.1 V for germanium transistor

In the saturation region, i.e. for the ON state

V_{BE} (sat) : 0.7 V for silicon transistor
0.3 V for germanium transistor
V_{CE} (sat) : 0.3 V for silicon transistor
0.1 V for germanium transistor

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B$ (min), where i_B (min) = i_C/h_{FE} (min) the transistor is really in saturation.
If $i_B \leq i_B$ (min), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

COMMUTATING CAPACITORS

We know that the bistable multivibrator has got two stable states and that it can remain in either of its two stable states indefinitely. It can change state only when a triggering signal such as a pulse from some external source is applied. When a triggering signal is applied, conduction has to transfer from one device to another. The transition time is defined as the interval during which conduction transfers from one transistor to another. The reason for this transition time is—even 'though the input signal at the base of a transistor may be transferred to the collector with zero rise time, the signal at the collector of the transistor cannot be transferred to the base of the other transistor instantaneously. This is because the input capacitance C, present at the base of the transistor makes the *R\-R2* attenuator act as an uncompensated attenuator and so it will have a finite rise time, $t_r = (R_f \backslash\backslash R_2)C_i$. The transition time may be reduced by compensating this att'.nuator by introducing a small capacitor in parallel with the coupling resistors R_f and *R* of the binary as shown in Figure 4.21. Since these capacitors are introduced to increase the speed of operation of the device, they are called *speed-up* capacitors. They are also called *transpose* or *commutating* capacitors. So, commutating capacitors are small capacitors connected in parallel with the coupling resistors in order to increase the speed of operation. The commutating capacitors hasten the removal of charge stored at the base of the ON transistor due to minority carriers. If the commutating capacitors are arbitrarily large, the /?]-/?2 network acts as an overcompensated attenuator and the signal at the collector

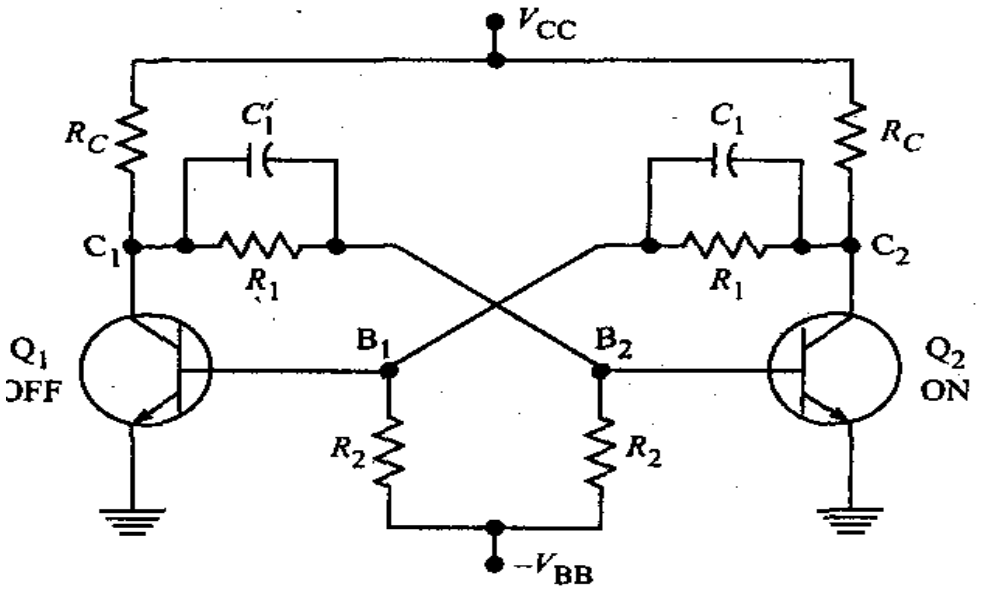
will be transmitted to the base of the other transistor very rapidly, but large values of capacitors have some disadvantages.

In the flip-flop shown in Figure 4.21, if for example Oj is OFF and Q_2 is ON, the voltages across C] and *C'*\ are not alike because, when Q_2 is ON and Qj is OFF, the voltage across *C[* is V_{CK2}(sat) - V_{Bi}(off) which is very small = 0.3 - (-1) = 1.3 V, and the voltage across *C*\ is equal to V_{cc} - V_{BE2}(sat) ~ 12 - 0.7 = 11.3 V. When the circuit is triggered so that Q_2 is OFF and Oj is ON, then the voltage-across C[must be 11.3 V and that across *C[* must be 1.3 V. The flip-flop would not have settled in its new state until the interchange of voltages had been completed.

A transistor having been induced to change the state by a triggering signal, a certain minimum time must elapse before a succeeding signal is able to reliably induce the reverse transition. The smallest allowable interval between triggers is called the *resolving time* of the flip-flop, and its reciprocal is the maximum frequency at which the binary will respond.

The 'complete transfer of conduction from one device to another involves two phases. The first of these is the transition time during which conduction transfers from one device to another. For this transfer of conduction to take place, the voltages across the input and output capacitances of the transistor have to change. The voltages across the commutating capacitors C[and Cj need not change during this transfer of conduction. After this transfer of conduction, the capacitors are allowed to interchange their voltages.

This additional time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the *settling time.* Of course, no clear-cut distinction can be made between the transition time and the settling time. The sum of the *transition time* and the *settling time* is called the *resolution time.* If the commutating capacitors are too small, the transition time is increased but the settling time will be small and if the commutating capacitors are too large, -the transition time is reduced but the settling time will be large. So, a compromise is called for.



The maximum frequency of operation /max is given by

Methods of improving resolution

The resolution of a binary can be improved by taking the following steps:

1 . *By reducing all stray , capacitances.* Reductions in the values of stray capacitances reduce their charging time, resulting in a reduction in the time taken by the transistors to go to the opposite state.

2. *By reducing the resistors R^, R2, and Rc.* Reductions in the values of /?j and /?2 result in a reduction in the charging time of the commutating capacitors with a consequent improvement in transition speed. Reducing resistors also reduces the recovery time.

3. *By not allowing the transistors to go into saturation.* When the transistors do not saturate, the storage time will be reduced resulting in fast change from ON to OFF.

A NON-SATURATING BINARY

The binary discussed earlier is a saturated binary. When the transistors are driven into saturation, because of the storage time delay, the speed of operation is reduced. The speed of operation can be increased by not allowing the transistors to go into saturation. Such a binary in which the transistors always operate in the active region only, is called a *non-saturating* binary.

Figure 4.22 shows the circuit diagram of a non-saturating binary. This is obtained adding two zener diodes and two p-n junction diodes to the collector-coupled binary sho' in Figure 4.21. These diodes ensure that the collector ta» junctions are reverse biased hence the transistor is always operating in the active region. Both the zener diodes D3 D4 are always biased in the breakdown direction and each has a voltage Vz < VQC it. The voltage across the diode DI or D2 is very small in the forward direction. When is ON, its emitter junction is forward biased with V_{BE2} * 0 V. So, the left side of D2 is at Vz and the right side is at VcE(sat). Therefore, D2 is ON and acts as a short circuit. Hence C2 = ^z> making the collector junction reverse biased, and the transistor Ch operates in the active region

$$V_{BE1} = -V_{BB}\frac{R_1}{R_1+R_2} + V_{CE2}\frac{R_2}{R_1+R_2} \approx -V_{BB}\frac{R_1}{R_1+R_2}$$

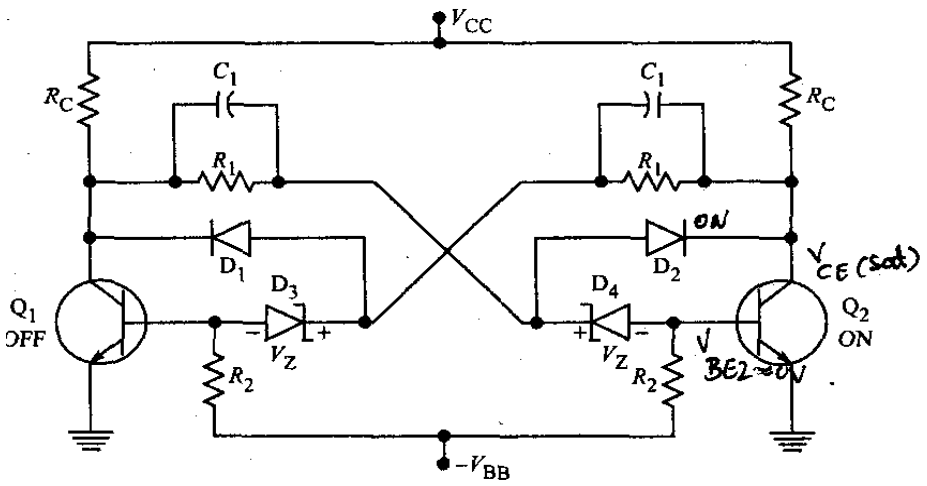


Figure A non-saturated binary

This negative voltage keeps Q_t cut-off. With Q, cut-off, VCEI is HIGH and so the diode DI is back biased. The output swing is approximately equal to VCG - V_z.

The non-saturating binary is preferred over the saturated binary only when an extremely high speed of operation is required because of the following drawbacks:

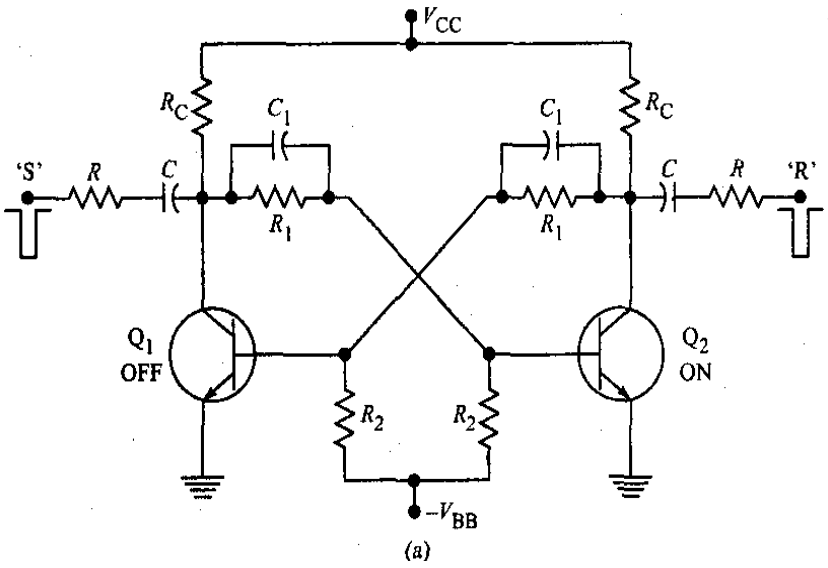
1. The non-saturating circuits are more complicated than the saturated, circuits.

2. The non-saturating circuits consume more power than the saturated circuits.

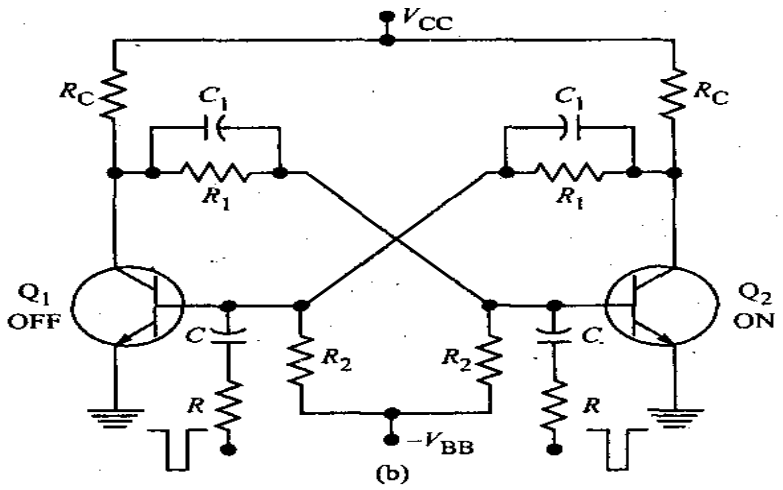
3. The voltage swing is less stable with temperature, ageing and component replacement than in the case of saturated binary.

TRIGGERING THE BINARY

We know that a bistable multivibrator has got two stable states and that it can remain in any one of the states indefinitely. The process of applying an external signal to induce a transition from one state to the other is called *triggering.* The triggering signal, which is usually employed is either a pulse of short duration or a step voltage. There are two methods of triggering—unsymmetrical triggering and symmetrical triggering. Unsymmetrical triggering is one in which the triggering signal is effective in inducing a transition in only one direction. In this, a second triggering signal from a separate source must be introduced in a different manner to achieve reverse transition, Symmetrical triggering is one in which each successive triggering signal induces a transition regardless of the state in which the binary happens to be, i.e..unsymmetrical triggering requires two separate sources whereas symmetrical triggering requires only one source. Unsymmetrical triggering finds extensive applications in logic circuitry (in registers, coding, etc.)- It can be used as a generator of a gate whose



(a)



Unsymmetrical triggering through a resistor and a capacitor (a) at the collectors and (b) at the bases.

width equals the interval between the triggers. Symmetrical triggering is used in binary counting circuits and other applications. .

The sensitivity of the binary to a pulse of such polarity as to turn OFF the conducting device will appreciably exceed the sensitivity to a pulse of opposite polarity. The triggering signal may be applied at the output of a stage or at the input of a stage. In transistor circuits the triggering signal may be applied at the collector of the transistor, or at the base.

An excellent method for triggering a binary unsymmetrically on the leading edge of a pulse is to apply the pulse from a high impedance source to the output of the non-conducting device For p-n-p transistors, a positive pulse needs to be applied.

The triggering signal may be applied through a resistor and a capacitor or through a unilateral device such as a diode. Figure 4.23 shows a method of triggering unsymmetncally through a resistor and a capacitor. If p-n-p transistors are employed, the polarity of the . triggering signal should be reversed.

TRIGGERING UNSYMMETRICALLY THROUGH A UNILATERAL DEVICE (DIODE)

Figure 4.24 shows unsymmetrical triggering through a unilateral device when the signals are applied at the collectors. Suppose in one stable state Q[is ON and Q_2 is OFF. When Q| is ON, the diode D at the collector of Qj is back biased by the drop across R_c because its anode is at $V_{CE}(sat)$ and cathode is at V_{cc}. So the diode will not transmit a positive pulse and even the negative pulse cannot be transmitted unless it has an amplitude larger than this voltage drop which anyway cannot affect the state of Q_2. So no change of state can take place by the application of a pulse at the collector of Qj when Q_1 is ON, When Q_2 is OFF, both anode and cathode of the diode at its collector are at V_{cc} and so the drop across D is zero. The diode will still fail to transmit a positive-going trigger, but will transmit a negative pulse or step to the input (base) of Qj (which is ON) which will result in a change of state. So when Qi is ON and Q_2 is OFF, only a negative pulse applied at 'R' can change the state. The resistor *R* must be large enough not to load down the

trigger source. On the other hand, *R* must be small enough so that any charge which accumulates on *C* during the interval when D conducts will have time to decay during the time between pulses. If the triggering rate is high, then it may be necessary to replace *R* with a diode.

Figure 4.25 shows unsymmetrical triggering through a diode when triggering signals are applied at the bases of the transistors. Here the negative pulse is applied through D to the base of the ON stage. *R* is returned to ground rather than to the supply voltage.

If the trigger amplitude available is small, it may be necessary to amplify the signal before applying it to the flip-flop. In this case a diode need not be used because the amplifier can provide the unilateral action previously supplied by the diode.

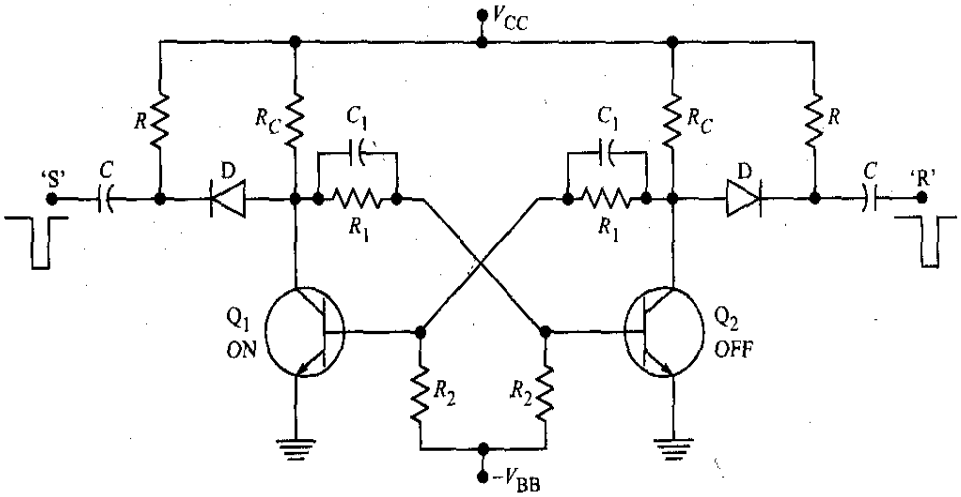
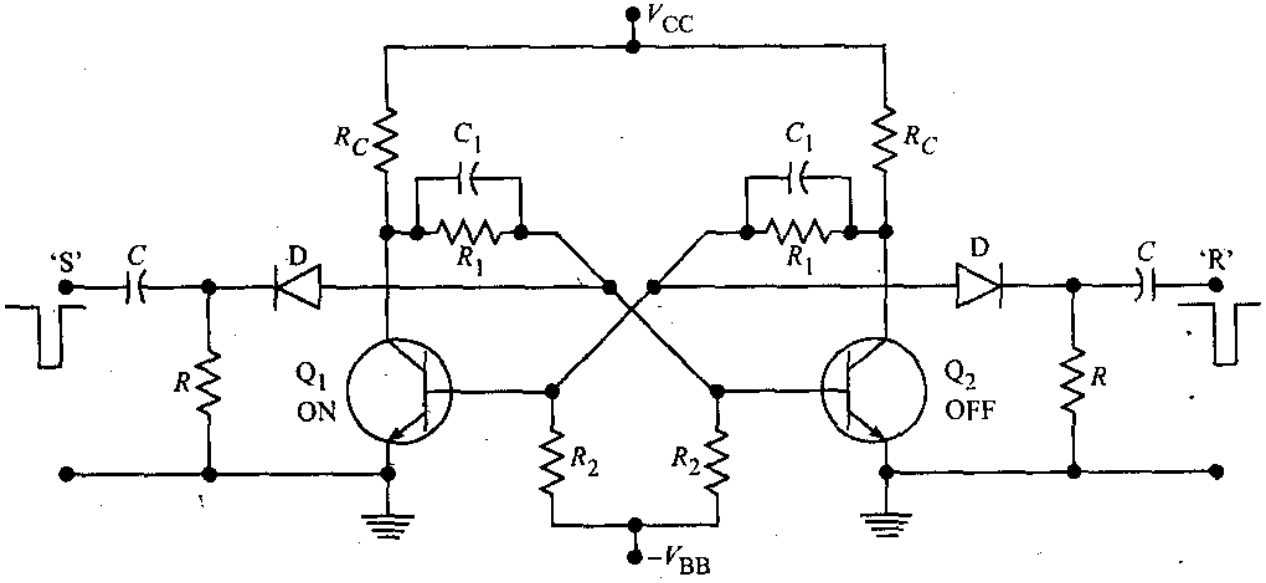
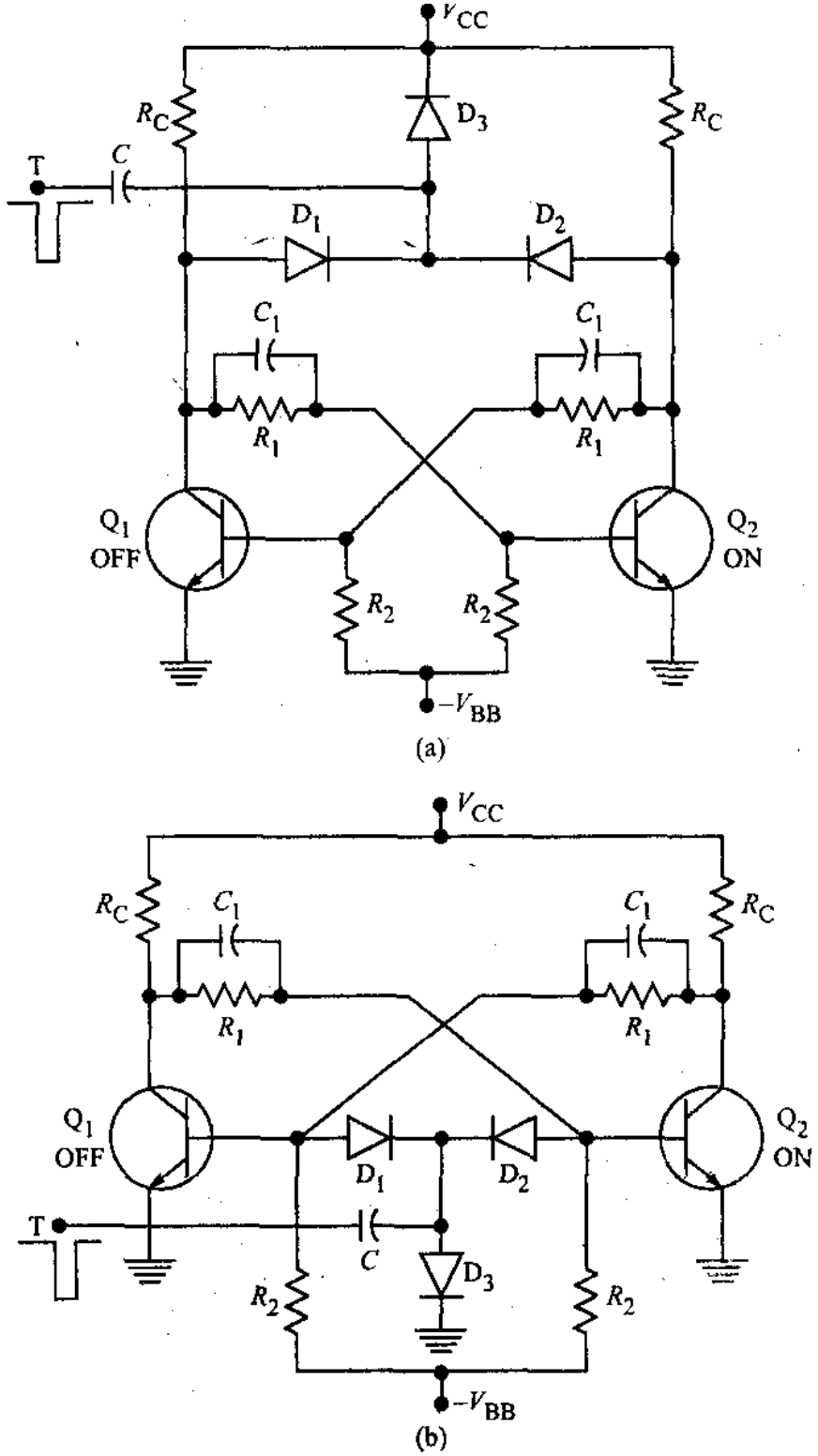


Figure Unsymmetrical triggering at collectors.



Unsymmetrical triggering at bases.

TRIGGERING SYMMETRICALLY THROUGH A UNILATERAL DEVICE



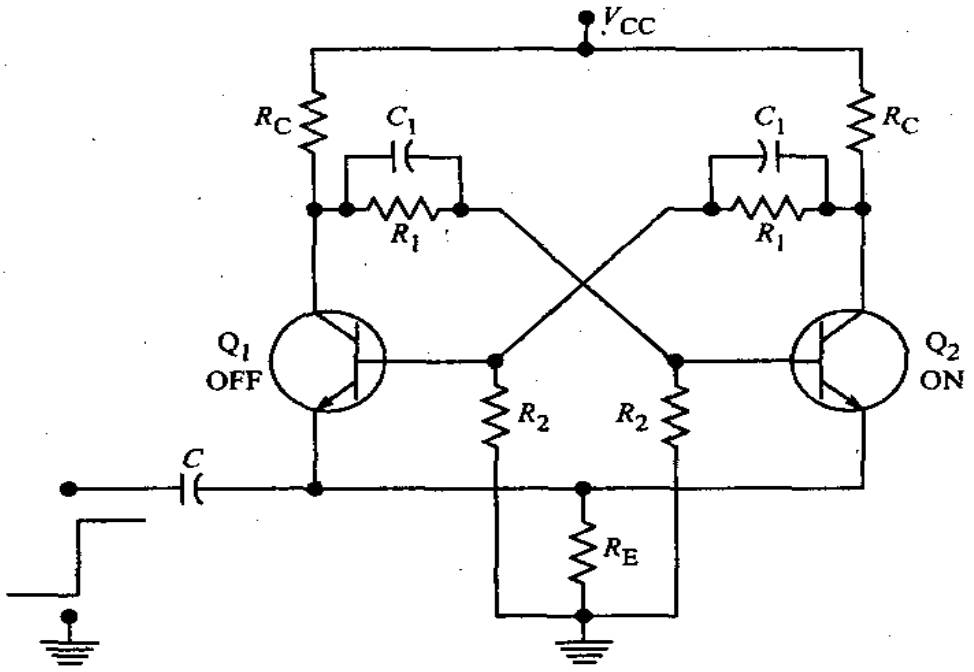
Symmetrical triggering through diodes (a) at the collectors iind (b) at the bases.

Figure 4.26(a) shows an arrangement for symmetrical triggering through diodes at the collectors of the transistors. If Q_2 is ON and Qj is OFF in one of the stable states, the collector of Q_2 is at Vcfi(sat) and the collector of Q[is at V_{CC}- Therefore, D_2 is reverse biased by V_{cc} and D] is at zero bias. Hence a negative

input signal will be transmitted through D] to the collector of Qi and thus to the base of the ON stage Q_2 via the *R\C* combination connecting the output of Qi to the input of Q_2. This negative pulse at the base of Q_2 which is ON, turns it to OFF state thus causing a transition. After the transition is completed, D(will be reverse biased and D_2 will be at zero bias. So the next negative pulse will pass through D_2 instead of through Dj. Hence these diodes are called *steering diodes.*The binary will transfer at each successive negative input pulse or step but will not respond to the triggers of opposite polarity. The diode D_3 serves the purpose of *R* in unsymmetrical triggering. If p-n-p transistors are used, then the diodes must be reversed and a positive triggering signal would be required.Figure 4.26(b) shows the arrangement of symmetrical triggering through the diodes at the bases of the transistors.Triggering may also be done symmetrically without the use of the auxiliary diodes. The presence of commutating capacitors facilitates this, but for this, the commutating capacitors

must be large, and large values of commutating capacitors lengthen the settling time of the binary. Therefore this method of triggering without the auxiliary steering diodes is not employed where the shortest possible resolution time is required.

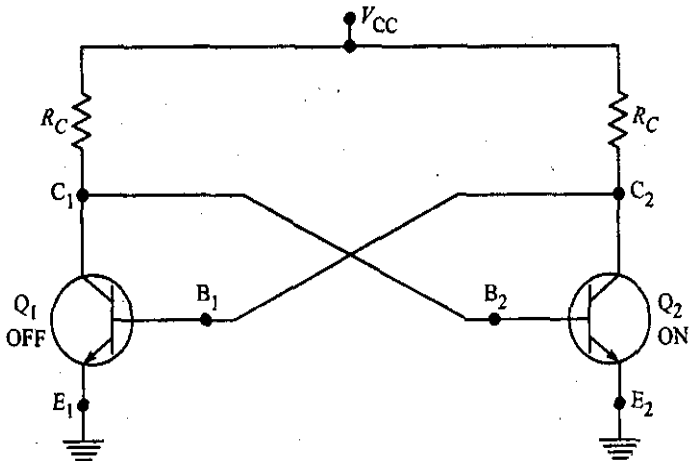
Figure 4.27 shows the arrangement for triggering a self-biased bistable multivibrator without steering diodes. Here a positive step is applied at the common emitters of the flip-flop.



Symmetrical triggering of a self-biased binary.

A DIRECT-CONNECTED BINARY

Figure 4.28 shows a direct-connected binary. No coupling elements are used and the collector of each transistor is connected to the base 6f the other transistor directly by a wire. In one stable state, transistor Qi is in saturation and Q_2 is conducting slightly, and in the other stable state, Q_2 is in saturation and Q! is conducting slightly.



A direct-connected binary.

Initially if we assume that Q] is ON, since its emitter is grounded and since its base and collector are connected to VcC through a resistor R_c, then

$$I_{B1} = \frac{V_{CC} - V_{BE1}}{R_C} \quad \text{and} \quad I_{C1} \approx \frac{V_{CC} - V_{CE1}}{R_C}$$

$$I_{B1} \gg \frac{I_{C1}}{h_{FE}}$$

and hence Q] is driven heavily into saturation. So for a Ge transistor, V_{CE1} = 0.05 V and V_{BE}i = 0.3 V. Because of the direct connection between the collector of Qi and the base of Qi> ^BEZ - ^CEI = 0-05 V; a small positive value. So Q_2 is not OFF and it will be conducting slightly. The output swing = V_{CE2} - V_{CE1} = V_{BE}»,- V_{CE}i = 0.3 - 0.05 = 0.25 V, Even though it has some advantages, there are many serious disadvantages too, and so this circuit is not used these days. It was available in 1C form as DCTL earlier,

The advantages of direct connected binary are:

\. Its extreme simplicity

2. Only one supply voltage of low value about 1.5 V is required.

3. Low power dissipation

4. Transistors with low breakdown voltages may be used.

5. The direct connected binary may be easily constructed as an 1C because of the few elements involved.

The disadvantages of direct connected binary are:

\. As temperature increases, the reverse saturation current /$_{CBO}$ may increase sufficiently to bring Q_t into active region and may even take Q_2 out of saturation.

2. Since Q_2 is driven heavily into saturation, the storage time delay will be large and the switching speed will be low.

3. The output voltages are equal to their saturation base and collector voltages, and these parameters may vary appreciably from transistor to transistor.

4. The voltage swing is only a fraction of a volt and hence the binary is susceptible to spurious voltages.
5. Since an OFF collector is tied directly to an ON base, it is difficult to trigger the binary by the usual method of applying a pulse to the OFF transistor. To supply sufficient current to take the ON transistor out of saturation, an amplifier trigger circuit is usually required.

THE EMITTER-COUPLED BINARY (THE SCHMITT TRIGGER CIRCUIT)

Figure 4.29 shows the circuit diagram of an emitter-coupled bistable multivibrator using n-p-n transistors. Quite commonly it is called *Schmin trigger* after the inventor of its vacuum-tube version. It differs from the basic collector-coupled binary in that the coupling from the output of the second stage to the input of the first stage is missing and the feedback is obtained now through a common emitter resistor R_E. It is a bistable circuit and the existence of only two stable states results form the fact that positive feedback is incorporated into the circuit, and from the further fact that the loop gain of the circuit is greater than MODULEy. There are several ways to adjust the loop gain. One way of adjusting the loop gain is.by varying /?$_{C1}$. Suppose R_C] is selected such that the loop gain is less than MODULEy. When fl$_{cl}$ is small, regeneration is not possible.

For the circuit of Figure 4.29, under quiescent conditions Qi is OFF and Q_2 is ON because it gets the required base drive from V_{CC} through R_{Ci} and /?j. So the output voltage

$$v_o = V_{CC} - I_{C2}R_{C2} \qquad \text{(where } I_{C2} \text{ is the current in } R_{C2} \text{ when } Q_1 \text{ is OFF)}$$

is at its lower level. With Q_2 conducting, there will be a voltage drop across R_E -7$_{B2}$)/?E> and this will elevate the emitter of *Q*\. As the input v is increased from zero, the circuit will not respond until Qi reaches the cut-in point (at v = V_t). Until then the output remains at its lower level. With Oj conducting (for v > V|) the circuit will amplify because Q_2 is already conducting and since the gain Av</Av is positive, the output will rise in response to the rise in input. As v continues to rise, C_t and hence B_2 continue to fall and E_2 continues to rise. Therefore a value of v will be reached at which Qa is turned OFF. At this point v_0 = V_{CC} and the output remains constant at this value of V_{cc}, even if the input is further increased. A plot of v_a versus v is shown in Figure 4.30(a) for loop gain < 1.

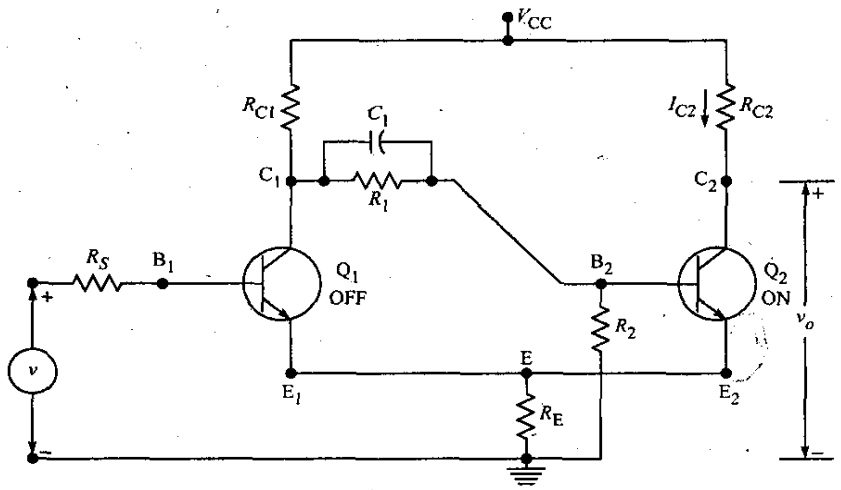
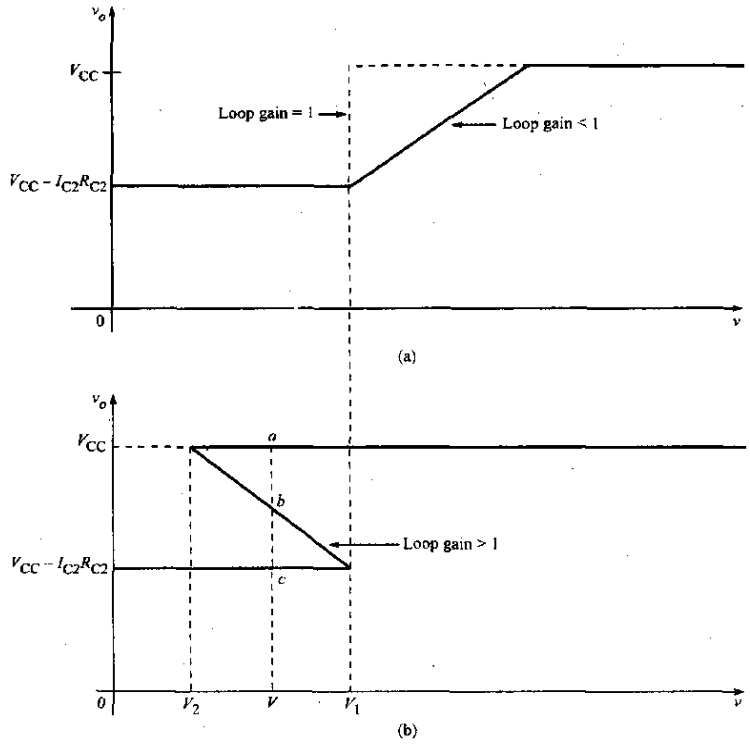


Figure 4.29 An emitter-coupled binary.

Suppose the loop gain is increased by increasing the resistance R_{ci}. Such a change will have negligible effect on the cut-in point V| of Qj. However in the region of amplification (i.e. for v > $V\{$) the amplifier gain Av</Av will increase and so the slope of the rising portion of the plot in Figure 4.30(a) will be steeper. This increase in slope with increase in loop gain continues until at a loop gain of MODULEy where the circuit has just become regenerative the slope will become infinite. And finally when the loop gain becomes greater than MODULEy, the slope becomes negative and the plot of v_a versus v assumes the S shape shown in Figure 4.30(b).



Response of emitter-coupled binary for (a) loop gain < 1 and (b) loop gain > 1.

The behaviour of the circuit may be described by using this S curve. As v rises from **zero** voltage, v_0 will remain at its lower level (= V_{CC} ~ 'c2 ^ca) $_{unt}$*l $_v$ reaches V\. (This value of v = V, at which the transistor **Qi** just enters into conduction is called the upper triggering point, UTP.) As v exceeds V_J the output will make an abrupt .transition to its higher level (= V_{cc}). For v > V_h **Qj** is ON and Q_2 is **OFF.** Similarly if v is initially greater than V], then as v is decreased, the output will remain at its upper level until v attains a **definite** level V_2 at which point the circuit makes an abrupt transition to its lower level. For v < ^2> Qi is **OFF** and **Q2** is **ON.** (This value of v = V_2 at which the transistor Q_2 resumes conduction is called the lower triggering point, LTP.) This circuit exhibits hysteresis, that is, to effect a transition in one direction we must first pass beyond the voltage at which the reverse transition took place.

A vertical line drawn at v = V which lies between V_2 and Vi intersects the S curve at three points *a, b* and *c.* The upper and lower points a and *c* are points of stable equilibrium.

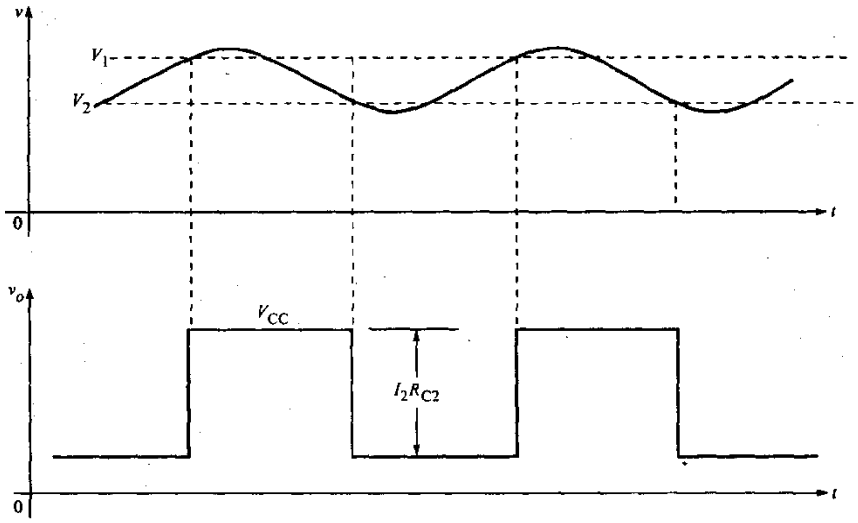
The S curve is a plot of values which satisfy Kirchhoff's laws and which are consistent with the transistor characteristics. At v = V, the circuit will be at a or *c,* depending on the direction of approach of v towards V. When v = V in the range between V_2 and V|, the Schmitt circuit is in one of its two possible stable states and hence is a bistable circuit.

Applications of Schmitt trigger circuit

Schmitt trigger is also a bistable multivibrator. Hence it can be used in applications where a normal binary is used. However for applications where the circuit is to be triggered back-and-forth between stable states, the normal binary is preferred because of its symmetry. Since the base of Q] is not involved in regenerative switching, the Schmitt trigger is preferred for applications in which the advantage of this free terminal can be taken. The resistance $K_{C2\ m\ me}$ output circuit of Q_2 is not required for the operation of the binary. Hence this resistance may be selected over a wide range to obtain different output signal amplitudes.

A most important application of the Schmitt trigger is its use as an amplitude comparator to mark the instant at which an arbitrary waveform attains a particular reference level. As input v rises to Vi or falls to V_2, the circuit makes a fast regenerative transfer to its other state.

Another important application of the Schmitt trigger is as a squaring circuit. It can convert a sine wave into a square wave. In fact, any slowly varying input waveform can be converted into a square wave with faster leading and trailing edges as shown in Figure 4.31, if the input has large enough excursions to carry the input beyond the limits of the hysteresis range, $V_H = V\backslash - V_2$.



Response of the emitter-coupled binary to an arbitrary input waveform.

In another important application, the Schmitt trigger circuit is triggered between its two stable states by alternate positive and negative pulses. If the input is biased at a voltage *V* between V_2 and *V* and if a positive pulse of amplitude greater than *V* - *V* is coupled to the input, then Qj will conduct and Q_2 will be OFF. If now a negative pulse of amplitude larger than *V* - V_2 is coupled to the input, the circuit will be triggered back to the state where Qj is OFF and Q_2 is ON.

Hysteresis

If the amplitude of the periodic input signal is large compared with the hysteresis range V_H, then the hysteresis of the Schmitt trigger is not a matter of concern. In some applications, a large hysteresis range will not allow the circuit to function properly.

Hysteresis may be eliminated by adjusting the loop gain of the circuit to MODULEy. Such an adjustment may be made in a number of ways:

(1) The loop gain may be increased or decreased by increasing or decreasing the resistance

(2) The loop gain may be increased or decreased by adding a resistance /?$_{E1}$ in series with the emitter of Qi, or by adding a resistance 7?^ in series with the emitter of Q_2 and then decreasing or increasing R_{EI} and R_{E2}. Since /?$_{C1}$ and R_{EJ} are in series with Qi, these resistors will have no effect on the circuit when Qi is OFF. Therefore, these resistors will not change *V* but may be used to move V_2 closer to or coincident with *V*. Similarly, R_{E2} will affect *V* but not V_2.

(3) The loop gain may also be varied by varying the ratio *R[/(Ri* + /?$_2$). Such an adjustment will change both *V* and V_2.

(4) The loop gain may be increased by increasing the value of *R$.*

If /?E1 or R_{E2} is larger than the value required to give zero hysteresis, then the gain will be less than MODULEy and the circuit will not change state. So, usually R_E\ or /?E2 is chosen so that a small amount of hysteresis remains in order to ensure that the loop gain is greater than MODULEy.

Vi is independent of R_s but V2 depends on $R\$$ and increases with an increase in the value of R_s. So for a large value of R_s it is possible for V2 to be equal to V\, Hysteresis is thus eliminated and the gain is MODULEy. If R_s exceeds this critical value, the loop gain falls below MODULEy and the circuit cannot bs triggered. If R_s is too small, the speed of operation of the

circuit is reduced.

Derivation of expression for UTP

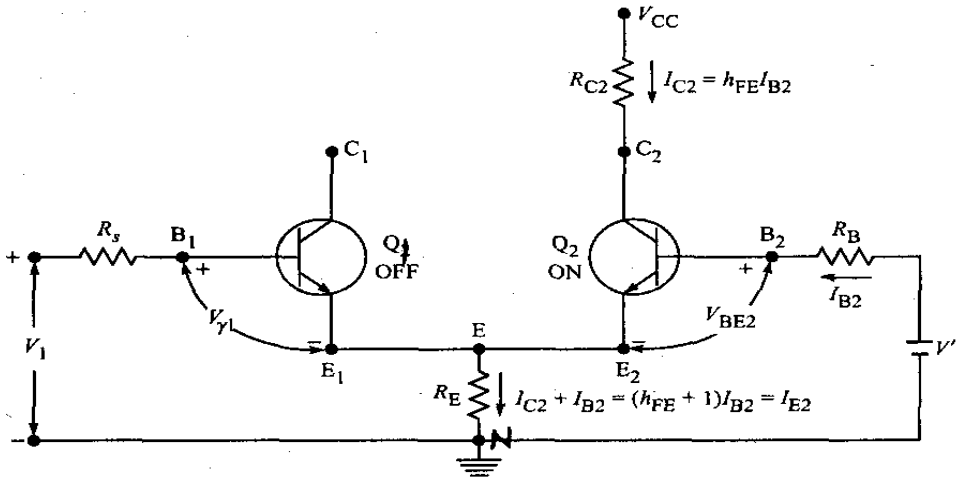
The upper triggering point UTP is defined as the input voltage V_l at which the transistor Qi just enters into conduction. To calculate Vb we have to first find the current in Q2 when Q! just enters into conduction. For this we have to find the Thevenin's equivalent voltage V and the Thevenin's equivalent resistance tfB at the base of Q2, where

$$V' = V_{CC}\frac{R_2}{R_2 + R_{C1} + R_1} \quad \text{and} \quad R_B = R_2 \parallel (R_{C1} + R_1) = \frac{R_2 (R_{C1} + R_1)}{R_2 + R_{C1} + R_1}$$

It is possible for Q2 to be in its active region or to be in saturation. Assuming that Q2 is in its active region

$I_{C2} = h_{FE} I_{B2} \qquad \therefore I_{E2} = I_{C2} + I_{B2} = (h_{FE} + 1) I_{B2}$

In the circuit shown in Figure 4.32, to calculate V\, we replace V_{cc}, KCI> ^i anc* ^2 of Figure 4.29 by V and R_B at the base of Q2.



The equivalent circuit of Figure 4.29 with Q| just at cut-in.

Writing KVL around the base loop of Q2,

$$V' - I_{B2}R_B - V_{BE2} - I_{B2}(h_{FE} + 1)R_E = 0$$

$$\therefore \quad I_{B2} = \frac{V' - V_{BE2}}{(h_{FE} + 1)R_E + R_B}$$

Hence $$V_{EN} = I_{B2}(h_{FE} + 1)R_E = \frac{(V' - V_{BE2})(h_{FE} + 1)R_E}{R_B + R_E(h_{FE} + 1)}$$

Also $$V_{EN1} = V_{EN} = V_{EN2}$$

Since Q_1 is just at cut-in, $I_{B1} = 0$ and $V_{BE1} = V_{\gamma 1}$

$$\therefore \quad V_1 = V_{EN1} + V_{BE1} + I_{B1}R_S = V_{EN} + V_{\gamma 1}$$

If $R_E(h_{FE} + 1) >> R_B$, the drop across R_B may be neglected compared to the drop across R_E.

$$\therefore \quad V_{EN} = V' - V_{BE2}$$

and $$V_1 = V' - V_{BE2} + V_{\gamma 1}$$

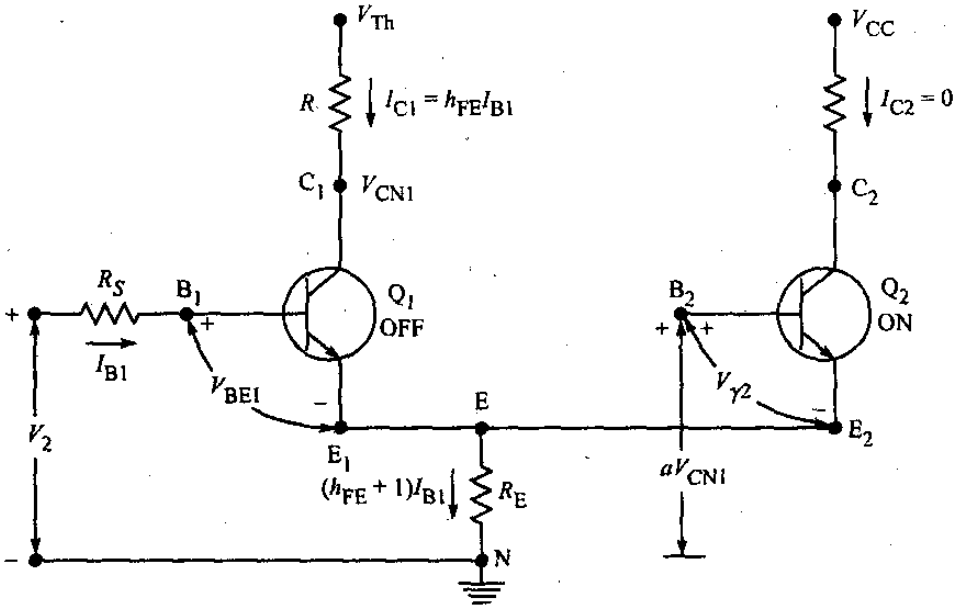
Since V_{yJ} is the voltage from base to emitter at cut-in where the loop gain just exceeds MODULEy, it differs from V_{BE2} in the active region by only 0.1 V for either Ge or Si.

This indicates that V, may be made almost independent of h^, of the emitter resistance R_E, of the temperature and of whether or not a silicon or germanium transistor is used. Hence the discriminator level V_t is stable with transistor replacement, ageing, temperature changes, provided that (/IPE + l)/?E » RB and that V" » 0.1. Since V depends on V_{cc}, *RCI*, *R*\ and R_2, where stability is required it is necessary that a stable supply and stable resistors are selected.

Derivation of expression for LTP

The lower triggering point LTP is defined as the input voltage V_2 at which the transistor Q_2 resumes conduction. *Vi* can be calculated from the circuit shown in Figure 4.33 which is obtained by replacing V_{cc}, J?C1, *RI* and R_2 of Figure 4.29 by Thevenin's equivalent voltage VTH and Thevenin's equivalent resistance *R* at the collector of $Q_($, where

$$V_{Th} = V_{CC}\frac{R_1 + R_2}{R_{C1} + R_1 + R_2} \quad \text{and} \quad R = R_{C1} \| (R_1 + R_2) = \frac{R_{C1}(R_1 + R_2)}{R_{C1} + R_1 + R_2}$$



The voltage ratio from the collector of Qi to the base of Q_2 Figure 4.33, the input signal to Qi is decreasing, and when it reaches V_2 then Q_2 comes out of cut-off.

Writing KVL around the base circuit of Q_2,

$$aV_{CN1} - V_{\gamma 2} - (I_{B1} + I_{C1})R_E = 0$$

where

$$V_{CN1} = V_{Th} - I_{C1}R$$

$\therefore$

$$aV_{Th} - aI_{C1}R - V_{\gamma 2} - I_{C1}\left(1 + \frac{1}{h_{FE}}\right)R_E = 0$$

or

$$I_{C1} = \frac{aV_{Th} - V_{\gamma 2}}{aR + R_E\left(1 + \frac{1}{h_{FE}}\right)}$$

$\therefore$

$$aV_{Th} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}\frac{R_1 + R_2}{R_1 + R_2 + R_{C1}} = V_{CC}\frac{R_2}{R_2 + R_{C1} + R_1} = V'$$

Let

$$R_E\left(1 + \frac{1}{h_{FE}}\right) = R'_E$$

$\therefore$

$$I_{C1} = \frac{V' - V_{\gamma 2}}{aR + R'_E}$$

Therefore from Figure 4.33,

$$V_2 = I_{B1}R_S + V_{BE1} + (I_{B1} + I_{C1})R_E$$

$$= V_{BE1} + I_{C1}\left(R_E\left(1 + \frac{1}{h_{FE}}\right) + \frac{R_S}{h_{FE}}\right)$$

$$= V_{BE1} + I_{C1}\left(R'_E + \frac{R_S}{h_{FE}}\right)$$

$$= V_{BE1} + \frac{V' - V_{\gamma 2}}{aR + R'_E}\left(R'_E + \frac{R_S}{h_{FE}}\right)$$

Since h_{FE} is a large number, $R'_E \approx R_E$ and usually $\frac{R_S}{h_{FE}} << R_E$

$$\therefore \quad V_2 = V_{BE1} + (V' - V_{\gamma 2})\frac{R'_E}{aR + R'_E}$$

Since V_{BE}| is higher for silicon than germanium, the LTP Va is a few tenths of a volt higher for a Schmitt trigger using silicon transistors than for one using germanium transistors.

MONOSTABLE MULTIVIBRATOR

As the name indicates, a monostable multivibrator has got only one permanent stable state, the other state being quasi stable. Under quiescent conditions, the monostable multivibrator will be in its stable state only. A triggering signal is required to induce a transition from the stable state to the quasi stable state.

Once triggered properly the circuit may remain in its quasi stable state for a time which is very long compared with the time of transition between the states, and after that it will return to its original state. No external triggering signal is required to induce this reverse transition. In a monostable multivibrator one coupling element is a resistor and another coupling element is a capacitor.

When triggered, since the circuit returns to its original state by itself after a time *T,* it is known as a one-shot, a single-step, or a univibrator. Since it generates a rectangular waveform which can be used to gate other circuits, it is also called a *gating circuit.* Furthermore, since it generates a fast transition at a predetermin6d time *T* after the input trigger, it is also referred to as a *delay circuit.* The monostable multivibrator may be a collector-coupled one, or an emitter-coupled one.

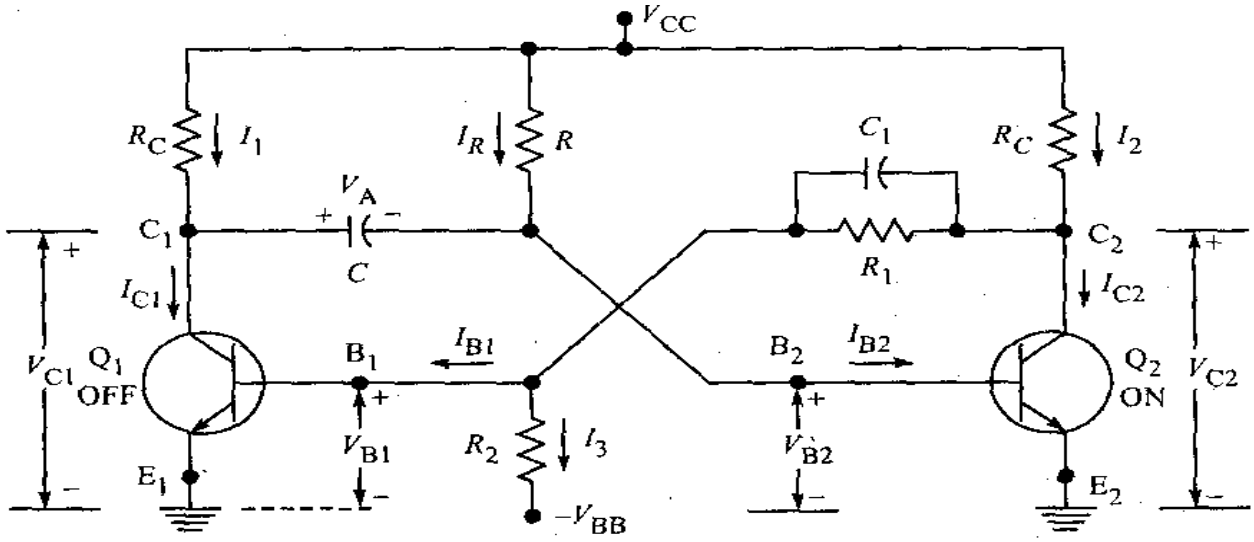
THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

Figure 4.41 shows the circuit diagram of a collector-to-base coupled (simply called collector- coupled) monostable multivibrator using n-p-n transistors. The collector of Q_2 is coupled to the base of Qi by a resistor R_f (dc coupling) and the collector of Q_t is coupled to the base of Q_2 by a capacitor *C* (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to $-V_{BB}$ through a resistor R_2, to ensure that Q! is cut off under quiescent conditions. The base of Q_2 is

connected to V_{CC} through R to ensure that Q_2 is ON under quiescent conditions. In fact, R may be returned to even a small positive voltage but connecting it to V_{cc} is advantageous.

The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q_2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q_2 or at the collector of Q|. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed.

When a negative signal is applied at the base of Q_2 at $t \sim 0$, due to regenerative action Q_2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current /i flows through its R_c and hence its collector voltage drops suddenly by $I\backslash R_C$ This drop will be instantaneously



transmitted through the coupling capacitor C to the base of Q_2. So at $t = 0_+$, the base voltage of Q_2 is

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time *T)* because when Q_t conducts, the coupling capacitor C charges from V_{cc} through the conducting transistor Qi and hence the potential at the base of Q_2 rises exponentially with a time constant

where R_0 is the conducting transistor output impedance including the resistance R_c. When it passes the cut-in voltage V_y of Q_2 (at a time $t = T$), a regenerative action takes place turning Q| OFF and eventually returning the multivibrator to its initial stable state.

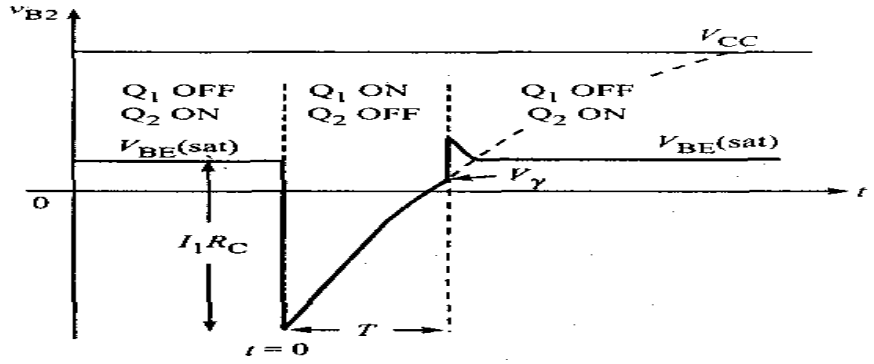
The transition from the stable state to the quasi-stable state takes place at $t = 0$, and the reverse transition from the quasi-stable state to the stable state takes place at $t = T$. The time T for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant $t(= RC)$.

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

Figure 4.42(a) shows the waveform at the base of transistor Q_2 of the monostable multivibrator shown in Figure 4.41.

For $t < 0$, Q_2 is ON and so $v_{B2} = V_{BE}(sat)$. At $t = 0$, a negative signal applied brings Q_2 to OFF state and Q[into saturation. A current /| flows through R_c of Q_t and hence v_{ci} drops abruptly by /|7?c volts and so v_{B2} also drops by $I\backslash R_C$ instantaneously. So at t - 0, $v_{B2} = V_{BE}(sat) - I_jR_C$. For $t > 0$, the capacitor charges with a time constant RC, and hence the base voltage of Q_2 rises exponentially towards V_{CC} with the same time constant. At $t = T$, when this base voltage rises to the cut-in voltage level Vy of the transistor, Q_2 goes to ON state, and Qj to OFF state and the pulse ends. 81

In the interval $0 < t < 7"$, the base voltage of Q_2, i.e. v_{B2} is given by



Voltage variation at the base of Q_2 during the quasi-stable state (neglecting /cuoX

But $I_1R_C = V_{CC} - V_{CE}(sat)$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE}(sat)$)

$$\therefore \quad v_{B2} = V_{CC} - [V_{CC} - \{V_{BE}(sat) - (V_{CC} - V_{CE}(sat))\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE}(sat) + V_{CE}(sat)\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE}(sat) + V_{BE}(sat)\}]e^{-T/\tau}$$

i.e.
$$e^{T/\tau} = \frac{2V_{CC} - [V_{CE}(sat) + V_{BE}(sat)]}{V_{CC} - V_\gamma}$$

$$\therefore \quad \frac{T}{\tau} = \frac{\ln\left[2\left(V_{CC} - \frac{V_{CE}(sat) + V_{BE}(sat)}{2}\right)\right]}{V_{CC} - V_\gamma}$$

i.e.
$$T = \tau \ln 2 + \tau \ln \frac{V_{CC} - \frac{V_{CE}(sat) + V_{BE}(sat)}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction voltages for either Ge or Si transistors,

Neglecting the second term in the expression for *T*

$$T = \tau \ln 2$$

i.e. $$T = (R + R_a)C \ln 2 = 0.693(R + R_a)C$$

but for a transistor in saturation $R_a \ll R$.

Gate width, $T = 0.693KC$

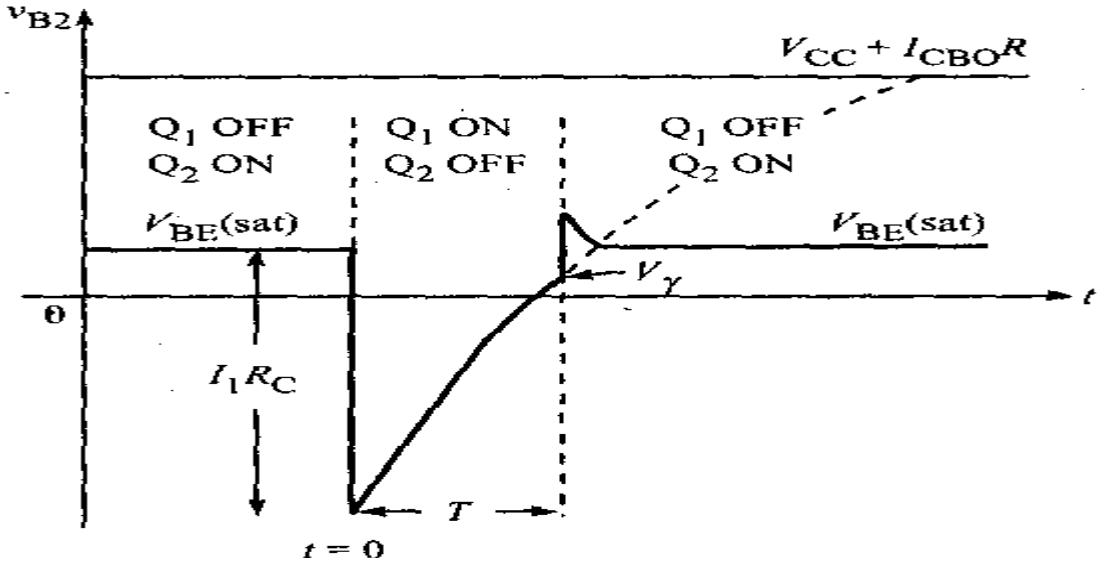
The larger the V_{cc} is, compared to the saturation junction voltages, the more accura the result is.

The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q_1 is driven into saturation during the quasi-stab state.

Expression for the gate width of a monostable multivibrator considering th reverse saturation current /CBO

In the derivation of the expression for gate width *T* above, we neglected the effect of tt reverse saturation current /CBO on the gate width *T.* In fact, as the temperature increases, tt reverse saturation current increases and the gate width decreases.

In the quasi-stable state when Q_2 is OFF, /CBO flows out of its base through *R* to th supply V_{cc}. Hence the base of Q_2 will be not at V_{cc} but at V_{cc} + /CBO^> ^ C *s disconnect from the junction of the base of Q_2 with the resistor *R.* It therefore appears that the capacitt C in effect charges through *R* from a source V_{cc} + /CBO^- See Figure 4.42(b).



So, the expression for the voltage at the base of Q_2 is given by

$$v_{B2} = (V_{CC} + I_{CBO}R) - [(V_{CC} + I_{CBO}R) - (V_{BE}(sat) - I_1R_C)]e^{-t/\tau}$$

$$= (V_{CC} + I_{CBO}R) - [(V_{CC} + I_{CBO}R) - (V_{BE}(sat) - (V_{CC} - V_{CE}(sat))]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} + I_{CBO}R - [2V_{CC} + I_{CBO}R - (V_{CE}(sat) + V_{BE}(sat))]e^{-T/\tau}$$

$$\therefore \quad e^{T/\tau} = \frac{2V_{CC} + I_{CBO}R - (V_{CE}(sat) + V_{BE}(sat))}{V_{CC} + I_{CBO}R - V_\gamma}$$

$$T = \tau \ln \frac{2\left[V_{CC} + \frac{I_{CBO}R}{2} - \frac{V_{BE}(sat) + V_{CE}(sat)}{2}\right]}{V_{CC} + I_{CBO}R - V_\gamma}$$

Neglecting the junction voltages and the cut-in voltage of the transistor,

$$T = \tau \ln \frac{2\left[V_{CC} + \frac{I_{CBO}R}{2}\right]}{V_{CC} + I_{CBO}R}$$

$$= \tau \ln 2 + \tau \ln \frac{1 + \frac{\phi}{2}}{1 + \phi}, \quad \text{where } \phi = \frac{I_{CBO}R}{V_{CC}}$$

$$T = \tau \ln 2 - \tau \ln \frac{1 + \phi}{1 + \frac{\phi}{2}}$$

Since I_{CBO} increases with temperature, we can conclude that the delay time T decreases as temperature increases.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q] and Q_2 of the monostable multivibrator of Figure 4.41 are shown in Figure 4.44.

The triggering signal is applied at $t = 0$, and the reverse transition occurs at $t = T$.

The stable state. For $t < 0$, the monostable circuit is in its stable state with Q_2 ON and Q, OFF. Since Q_2 is ON, the^ase voltage of Q_2 is $v_{B2} = V_{BE2}(sat)$ and the collector voltage of Q_2 is $v_{C2} = V_{CE2}(sat)$. Since Q, is OFF, there is no current in R_c of Q! and its base voltage must be negative. Hence the voltage at the collector of Q| is, $v_{C1} = V_{CC}$

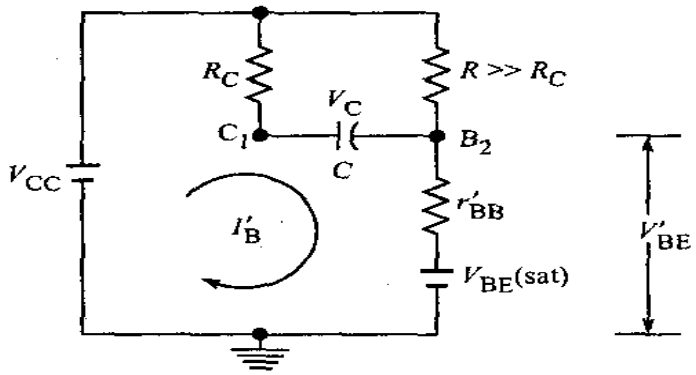
and the voltage at the base of Q] using the superposition theorem is

***The quasi-stable** state.* A negative triggering signal applied at $t = 0$ brings Q_2 to OFF state and Qi to ON state. A current /, flows in tf_c of Q]. So, the collector voltage of Qj drops suddenly by I_JR_C volts. Since the voltage across the coupling capacitor C cannot change instantaneously, the voltage at the base of Q_2 also drops by /itf_c, where $I_tR_C = V_{cc}$ -VcE2($_{sat}$)- Since Qi is ON,

In the interval $0 < t < T$, the voltages VGI, VBI and Vc2 remain constant at their values at f = 0, but the voltage at the base of. Q_2, i.e. v_{B2} rises exponentially towards V_{cc} with a time constant, *t - RC,* until at $t = T$, $v_{B}2$ reaches the cut-in voltage V_x of the transistor.

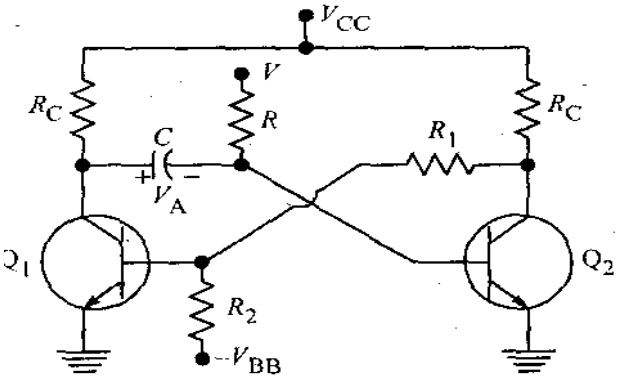
Waveforms for t > T. At / = 7*1", reverse transition -takes place. Q_2 conducts and Qi is cut-off. The collector voltage of Q_2 and the base voltage of Qi return to their voltage levels for / < 0. The voltage v_{cl} now rises abruptly since Q_t is OFF. This increase in voltage is transmitted to the base of Q_2 and drives Q_2 heavily into saturation. Hence an overshoot develops in v_{B2} at t = 7**", which decays as the capacitor recharges because of the base current. The magnitude of the base current may be calculated as follows. Replace the input circuit of Q_2 by the base spreading resistance r_{BB} in series with the voltage VsE(sat) as shown in Figure 4.43. Let 7_B be the base current at *t = 1**. The current in *R* may be neglected compared to $/'_B$.

$$V'_{BE} = I'_B r'_{BB} + V_{BE}(\text{sat}) \quad \text{and} \quad V_C = V_{CC} - I'_B R_C - V'_{BE}$$

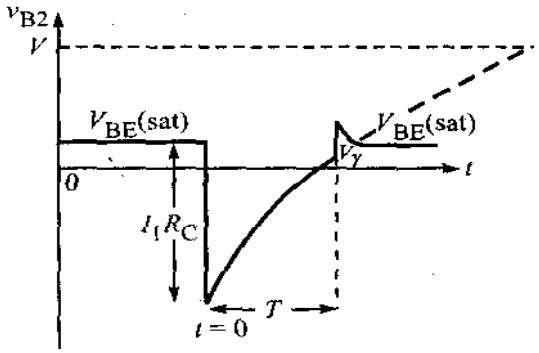


Monostable multivibrator as a voltage-to-time converter (as a pulse width modulator) Figure 4.45(a) shows the circuit diagram of a monostable multivibrator as a voltage- to-time converter. By varying the auxiliary supply voltage *V,* the pulse width can be changed. It can be seen that the resistor *R* is connected to the auxiliary voltage source *V* instead of to

The waveform of the voltage v_{B2} at the base of Q_2 is shown in Figure 4.45(b).



(a)



(b)

In the interval $0 < t < T$, v_{B2} is given by

$$v_{B2} = v_f - (v_f - v_{in})\, e^{-t/\tau}$$

$$\therefore \quad v_{B2} = V - [V - (V_{BE}(\text{sat}) - I_1 R_C)]e^{-t/\tau}$$

But $I_1 R_C = V_{CC} - V_{CE}\ (\text{sat})$

$$\therefore \quad v_{B2} = V - [V - \{V_{BE}(\text{sat}) - (V_{CC} - V_{CE}\ (\text{sat}))\}]\, e^{-t/\tau}$$

$$= V - [V + V_{CC} - (V_{BE}(\text{sat}) + V_{CE}(\text{sat}))]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V - [V + V_{CC} - (V_{BE}(\text{sat}) + V_{CE}\ (\text{sat}))]e^{-T/\tau}$$

$$\therefore \quad e^{T/\tau} = \frac{V + V_{CC} - (V_{BE}\,(\text{sat}) + V_{CE}\,(\text{sat}))}{V - V_\gamma}$$

Neglecting the junction voltages and the cut in voltage

$$T = \tau \log \frac{V + V_{CC}}{V}$$

$$= \tau \log \left(1 + \frac{V_{CC}}{V}\right)$$

Thus the pulse width is a function of auxiliary voltage V. For this reason the monostable multivibrator shown in Figure 4 .45 (a) is termed a *voltdge-to-time converter.* It is also called a pulse width modulator.

THE EMITTER-COUPLED MONOSTABLE MULTIVIBRATOR

Figure 4.51 shows the circuit diagram of an emitter-coupled monostable multivibrator. It differs from the collector-coupled one-shot in that the collector of Q_2 is not coupled to the base of Q] and instead the feedback has been provided through a common emitter resistance *R*& Also, there is no need for a negative power supply. Since the signal at C_2 is not directly involved in the regenerative loop, this collector makes an ideal point from which to obtain an output voltage waveform. Since the base of Qj is not connected to any other point in the circuit, it makes a good point at which to inject a triggering signal. Hence the trigger source cannot load the circuit. The gate width of a one-shot can be controlled through /,. In the case of collector-coupled one-shot it is not possible to stabilize 7j, but in an emitter-coupled one-shot, the presence of the emitter resistance R_E serves to stabilize /]. The current *I*\ may be adjusted through the bias

voltage V, and *T* varies linearly with *V*. Hence an emitter-coupled configuration makes an excellent gate wave generator whose width is easily and linearly controllable by means of an electrical signal.

TRIGGERING THE MONOSTABLE MULTIVIBRATOR

A monostable multivibrator needs to be triggered by a suitable signal in order to switch it from the stable state to the quasi stable state. However after remaining in the quasi stable state for a time $T = 0.693\ RC$, it automatically switches back to the original stable state, without any triggering signal applied. Thus unlike a bistable multivibrator, a monostable multivibrator requires only one triggering signal. Hence only unsymmetrical triggering techniques are adopted for monostable multivibrators. Generally speaking, all the triggering methods which are applicable to the binary are also applicable to the monostable multivibrator. The collector-coupled monostable multivibrator is normally triggered by applying a negative pulse at the collector of the OFF transistor (n-p-n) Qi through an *RC* differentiator circuit which converts it into positive and negative spikes as shown in Figure 4.50. The positive spike is blocked by the diode and the negative spike is transmitted through it and the capacitor C to the base of the ON transistor Q_2. So Q_2 goes to the OFF state and Qi to the ON state. This method has two advantages: one is as we know; the multivibrator is more sensitive to a pulse of such a polarity which brings the ON device to the OFF state. The second is, at the instant of the transition, the collector of Qi drops, the diode no longer conducts, and the multivibrator does not respond to the triggering signal till the quasi-stable state is completed. The emitter-coupled monostable multivibrator may be triggered by applying a positive pulse of sufficient amplitude at the base of Qt to bring the OFF transistor Q! to the ON state as shown in Figure 4.51.

ASTABLE MULTIVIBRATOR

As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator