INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
M.Tech I Semester End Examinations (Regular) - January/February, 2018

Regulation: IARE–R16

HIGH PERFORMANCE ARCHITECTURE
(Computer Science and Engineering)

Time: 3 Hours   **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) How processor parallelism is achieved? Explain with a suitable example for asynchronous processor parallelism. **[7M]**

   (b) Solve the dependence equation for the below code **[7M]**
   DO I = 1 , N
   A(I+1)=A(I)+B
   ENDDO

2. (a) Write advantages and disadvantages of superscalar and VLIW processor. **[7M]**

   (b) Construct all direction vectors for the following loop and indicate the type of dependence associated with each. **[7M]**
   DO K =1,100
   DO J = 1, 100
   DO I = 1, 100
         S: A(I+1,J,K) = A(I,J,5) + B
   ENDDO
   ENDDO
   ENDDO

UNIT – II

3. (a) Discuss briefly ZIV test and SIV test. Differentiate the delta test and multiple- subscript tests. **[7M]**

   (b) Apply the loop peeling for the following loop **[7M]**
   DO 10 I=1,N
   S1: Y(I,N)=Y(1,N) + Y(N,N)
   ENDDO

4. (a) Define the following terms with suitable examples. **[7M]**
      (i) ZIV -subscript (ii) SIV -subscript (iii) MIV-subscript

   (b) Explain briefly the concept of constraints and constraint vectors with suitable examples. **[7M]**

UNIT – III

5. (a) Differentiate Fine-Grained parallelism and Coarse-Grained parallelism. **[7M]**

    (b) List drawbacks of scalar expansion and also state the solutions to prevent these drawbacks.**[7M]**

6. (a) Discuss loop alignment and loop replication algorithm with an example. **[7M]**

    (b) Indiscriminate loop fusion may reduce parallelism - Justify with a suitable example. **[7M]**

UNIT – IV

7. (a) Identify how register allocation plays a vital role in compiler optimization and list the types of cache blocking. **[7M]**

    (b) A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K X 32. **[7M]**
    (i) Formulate all pertinent information required to construct the cache memory.
    (ii) What is the size of cache memory?

8. (a) What are the two ways to remove backward branches? Explain with solutions. **[7M]**

    (b) What is software perfecting? What are its advantages and disadvantages? How can the disadvantages be minimized? **[7M]**

UNIT – V

9. (a) Explain the types of data dependence for register reuse. **[7M]**

    (b) Apply scalar replacement for the following code **[7M]**
    DO I = 1, N
    A(I) = B(I) + C
    X(I) = A(I)*Q
    ENDDO

10. (a) Explain about dependence spanning multiple iterations with example code. **[7M]**

    (b) Identify how data dependence is calculated if registers are reused and how can we improve register reuse in loop carried and loop independent reuse. **[7M]**