INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

M.Tech II Semester End Examinations (Regular) - July, 2017

Regulation: IARE–R16

DISTRIBUTED OPERATED SYSTEM
(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Give the comparison of three different ways of organising n CPUs in distributed systems. **[7M]**
   (b) Illustrate different steps in basic Remote Procedure call operations. **[7M]**

(OR)

2. (a) Briefly discuss the advantages of distributed systems over centralized systems. **[7M]**
   (b) Explain different addressing mechanism in client server communication model. **[7M]**

UNIT – II

3. (a) Explain the working of ring algorithm in electing a leader in election algorithm with an example. **[7M]**
   (b) Explain different approaches involved in handling distributed deadlock prevention. **[7M]**

(OR)

4. (a) Illustrate with an example how Lamport's algorithm synchronises the logical clocks in distributed systems. **[7M]**
   (b) What is Deadlocks in distributed systems? Explain various strategies used to handle deadlocks in distributed systems. **[7M]**

UNIT – III

5. (a) Illustrate the working of a registry-based algorithm for finding and using idle workstations.**[7M]**
   (b) Briefly discuss the advantages of stageful and stateless servers. **[7M]**

(OR)

6. (a) Briefly discuss different design Issues for Processor Allocation Algorithms. **[7M]**
   (b) What are the reasons for replication? Explain different techniques of replication in distributed file system. **[7M]**

UNIT – IV

7. (a) Briefly discuss different consistency models using synchronization operations and consistency models not using synchronization operations. **[7M]**

   (b) Explain the concept of usage of twin pages which are used in Munin release consistency. **[7M]**

(OR)

8. (a) Briefly explain the properties of weak consistency model in distributed synchronization operations. **[7M]**

   (b) Explain the events in write-through cache consistency protocol and the corresponding action taken by a cache in response to its own CPU's operation and remote CPU's operation. **[7M]**

UNIT – V

9. (a) List and briefly explain different principal message types that go from the kernel to the memory manager. **[7M]**

   (b) Write a brief note on conceptual model of memory that Mach user processes in a linear virtual address space. **[7M]**

(OR)

10. (a) Illustrate what are the different components involved in a mach process. **[7M]**

    (b) Explain different Process Management Primitives provided by Mach microkernel-based operating system. **[7M]**

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