INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal, Hyderabad -500 043

CIVIL ENGINEERING

COURSE DESCRIPTOR

Course Title	**BASIC ELECTRONICS ENGINEERING**	
Course Code	AECB01	
Programme	B.Tech	
Semester	III	CE
Course Type	Foundation	
Regulation	IARE - R18	
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	0	3	-	-
Chief Coordinator	Mr. P. Sandeep Kumar, Assistant Professor, ECE	
Course Faculty	Mr. B. Santhosh Kumar, Assistant Professor, ECE	

I. COURSE OVERVIEW:

This course provides the preliminary knowledge on electronics for civil engineering students. The course gives insights into the construction, operation and of the diodes and transistors. It provides the understanding about the integrated circuits applications, focusing on generic applications through operational amplifiers, timers. The course also includes digital electronics.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AHSB04	II	Waves and Optics	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Basic Electronics Engineering	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exam.

Quiz-Online Examination

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT)

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning center. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE(Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed By
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Assignments
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusion using first principles of mathematics, natural sciences, and engineering sciences.	1	Seminar
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Guest lectures

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes (PSOs)	Strength	Proficiency assessed by
PSO 1	**Professional Skills:** Graduates shall demonstrate sound knowledge in analysis, design, laboratory investigations and construction aspects of civil engineering infrastructure, along with good foundation in mathematics, basic sciences and technical communication.	1	Seminar
PSO 2	**Broadness and Diversity:** Graduates will have a broad understanding of economical, environmental, societal, health and safety factors involved in infrastructural development, and shall demonstrate ability to function within multidisciplinary teams with competence in	-	-

	Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
	modern tool usage.			
PSO 3	**Self -learning and Service**: Graduates will be motivated for continuous self-learning in engineering practice and/ or pursue research in advanced areas of civil engineering in order to offer engineering services to the society, ethically and responsibly.		-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Introduce components such as diodes, BJTs and FETs.
II	Know the applications of components.
III	Understand common forms of number representation in logic circuits
IV	Be acquainted to principles and characteristics of op-amp and apply the techniques for the design of comparators, instrumentation amplifier, integrator, and differentiator.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe the concept of diode and its applications	CLO 1	Understand the basic concept of PN junction diode.
		CLO 2	Analyze the characteristics of diode for ideal and practical conditions.
		CLO 3	Understand the applications of diode in rectifiers with and without filters.
		CLO 4	Understand the concept of breakdown mechanism in diodes with applications of Zener breakdown diodes.
CO 2	Describe the operation of various transistors, FETs and their biasing methods.	CLO 5	Describe the classification family table of various transistors.
		CLO 6	Describe the concept of Bipolar Junction transistor with various modes of operation.
		CLO 7	Understand the concept of transistor biasing with voltage divider bias.
		CLO 8	Understand the construction and working of Field Effect Transistor(FET).
		CLO 9	Understand the concept of Metal Oxide Semiconductor FET.
		CLO 10	Illustrate the basic CMOS circuits.
CO 3	Understand the concept of operational amplifier with analysis of applications.	CLO 11	Understand the basic concepts of operational amplifiers.
		CLO 12	Analyze the parameters of practical and ideal op-amps.
		CLO 13	Understand the concept of virtual ground in op-amps.
		CLO 14	Perform basic arithmetic operations on voltages using opamps.
		CLO 15	Examine the working of op-amp as differentiator, integrator, comparator and buffer.
CO 4	Analysis of 555 timer IC for	CLO 16	Understand the internal block diagram of 555 timer IC.

COs	Course Outcome	CLOs	Course Learning Outcome
	multivibrators and op-amp data converters.	CLO 17	Examine the working of 555 timer as astable and monostable multivibrator.
		CLO 18	Understand the principle of data conversions with terminology.
		CLO 19	Analyze the various analog to digital converters.
		CLO 20	Analyze the various resistor ladder digital to analog converters.
CO 5	Explore the digital number systems and various digital logic circuits.	CLO 21	Perform calculations in different number systems.
		CLO 22	Understand the basic concepts of Boolean algebra and combinational logic circuits.
		CLO 23	Understand the basic sequential logic circuits.
		CLO 24	Understand counters, shift registers.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB01.01	CLO 1	Understand the basic concept of PN junction diode.	PO 1	3
AECB01.02	CLO 2	Analyze the characteristics of diode for ideal and practical conditions.	PO 2	1
AECB01.03	CLO 3	Understand the applications of diode in rectifiers with and without filters.	PO 1,PO 4	3
AECB01.04	CLO 4	Understand the concept of breakdown mechanism in diodes with applications of Zener breakdown diodes.	PO 1	3
AECB01.05	CLO 5	Describe the classification family table of various transistors.	PO 1	3
AECB01.06	CLO 6	Describe the concept of Bipolar Junction transistor with various modes of operation.	PO 2	1
AECB01.07	CLO 7	Understand the concept of transistor biasing with voltage divider bias.	PO 2	1
AECB01.08	CLO 8	Understand the construction and working of Field Effect Transistor(FET).	PO 1	3
AECB01.09	CLO 9	Understand the concept of Metal Oxide Semiconductor FET.	PO 1	3
AECB01.10	CLO 10	Illustrate the basic CMOS circuits.	PO 2	1
AECB01.11	CLO 11	Understand the basic concepts of operational amplifiers.	PO 1	3
AECB01.12	CLO 12	Analyze the parameters of practical and ideal op-amps.	PO 2	1
AECB01.13	CLO 13	Understand the concept of virtual ground in op-amps.	PO 1	3
AECB01.14	CLO 14	Perform basic arithmetic operations on voltages using opamps.	PO 1	3
AECB01.15	CLO 15	Examine the working of op-amp as differentiator, integrator, comparator and buffer.	PO 1	3
AECB01.16	CLO 16	Understand the internal block diagram of 555 timer IC.	PO 1	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB01.17	CLO 17	Examine the working of 555 timer as astable and monostable multivibrator.	PO 2	1
AECB01.18	CLO 18	Understand the principle of data conversions with terminology.	PO 2	1
AECB01.19	CLO 19	Analyze the A/D converters.	PO 2	1
AECB01.20	CLO 20	Analyze the resistor ladder D/A converters.	PO 2	1
AECB01.21	CLO 21	Perform calculations in different number systems.	PO 1, PO 4	3
AECB01.22	CLO 22	Understand the basic concepts of Boolean algebra and combinational logic circuits.	PO 1, PO 2	3
AECB01.23	CLO 23	Understand the basic sequential logic circuits.	PO 1, PO 2	3
AECB01.24	CLO 24	Understand counters, shift registers.	PO 1, PO 2	3

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcome(COs)	Program Outcomes (POs)			
	PO 1	PO 2	PO 4	PSO1
CO 1	3	1	1	1
CO 2	2	1		1
CO 3	3	1		1
CO 4	2	1		
CO 5	3	1	1	

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XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3												1		
CLO 2		1													
CLO 3	3	1		1									1		
CLO 4	3														
CLO 5	3	1											1		
CLO 6		1													
CLO 7		1													

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 8	3												1		
CLO 9	3														
CLO 10		1													
CLO 11	3												1		
CLO 12		1											1		
CLO 13	3														
CLO 14	3														
CLO 15	3														
CLO 16	3														
CLO 17		1													
CLO 18		1											1		
CLO 19		1											1		
CLO 20		1											1		
CLO 21	3			1									1		
CLO 22	3	1											1		
CLO 23	3	1													
CLO 24	3	1													

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XIII. ASSESSMENT METHODOLOGIES - DIRECT

CIE Exams	PO1, PO2, PO4,PSO1	SEE Exams	PO1, PO2, PO4,PSO1	Assignments	-	Seminars	PO1, PO2, PO4,PSO1
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Guest Lectures	PO4						

XIV. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS:

MODULE – I	DIODE AND APPLICATIONS	Classes: 08

Semiconductor Diode - Ideal versus Practical, Resistance Levels, Diode Equivalent Circuits, Load Line Analysis; Diode as a Switch, Diode as a Rectifier, Half Wave and Full Wave Rectifiers with and without Filters; Breakdown Mechanisms, Zener Diode – Operation and Applications.

MODULE - II	BIPOLAR JUNCTION TRANSISTOR (BJT)	Classes: 10

Bipolar Junction Transistor (BJT) – Construction, Operation, Amplifying Action, Common Base, Common Emitter and Common Collector Configurations, Operating Point, Voltage Divider Bias Configuration; Field Effect Transistor (FET) – Construction, Characteristics of Junction FET, Depletion and Enhancement type Metal Oxide Semiconductor (MOS) FETs, Introduction to CMOS.

MODULE - III	OPERATIONAL AMPLIFIERS AND APPLICATIONS	Classes: 08

Introduction to Op-Amp, Differential Amplifier Configurations, CMRR, PSRR, Slew Rate; Block Diagram, Pin Configuration of 741 Op-Amp, Characteristics of Ideal OpAmp, Concept of Virtual Ground; Op-Amp Applications- Inverting, Non-Inverting, Summing and Difference Amplifiers, Voltage Follower, Comparator, Differentiator, Integrator.

MODULE - IV	TIMERS AND DATA CONVERTERS	Classes: 10

IC 555 Timer – Block Diagram, Astable and Mono stable Multi vibrator Configurations; Data Converters – Basic Principle of Analogue–to-Digital (ADC) and Digital-to-Analogue (DAC) Conversion, Flash type, Counter-ramp type and Successive Approximation type ADCs, Resistor Ladder Type DAC, Specifications of ADC and DAC.

MODULE - V	BASIC DIGITAL ELECTRONICS	Classes: 09

Binary Number Systems and Codes; Basic Logic Gates and Truth Tables, Boolean Algebra, De Morgan's Theorems, Logic Circuits, Flip-Flops – SR, JK, D type, Clocked and Master-Slave Configurations; Counters –Asynchronous, Synchronous, Ripple, Non-Binary, BCD Decade types; Shift Registers – Right-Shift, Left-Shift, Serial-In-Serial-Out and Serial-In-Parallel-Out Shift Registers; Applications.

Text Books:

1. R. L. Boylestad & Louis Nashlesky, "Electronic Devices &Circuit Theory", Pearson Education, 2007.
2. Santiram Kal, "Basic Electronics- Devices, Circuits and IT Fundamentals", Prentice Hall, India, 2002.

Reference Books:

1. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 2008.
2. Thomas L. Floyd and R. P. Jain, "Digital Fundamentals", Pearson Education, 2009.
3. R. S. Sedha , "A Text Book of Electronic Devices and Circuits", S. Chand & Co., 2010.
4. R. T. Paynter, "Introductory Electronic Devices & Circuits – Conventional Flow Version", Pearson Education, 2009.

Web References:

1. mcsbzu.blogspot.com
2. https://archive.org/details/ElectronicDevicesCircuits
3. https://www.smartzworld.com
4. https://www.crectirupati.com

E-Text Books:

1. https://books.google.co.in/books/about/Switching_Theory_and_Logic_Design
2. http://services.eng.uts.edu.au/pmcl/ec/Downloads/LectureNotes.pdf
3. http://nptel.ac.in/courses/122106025/
4. https://books.google.co.in/books?isbn=8122414702
5. https://books.google.co.in/books?isbn=013186389

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Understand the basic concept of PN junction diode.	CLO 1	T1:1.6
2-5	Analyze the characteristics of diode for ideal and practical conditions.	CLO 2	T1:1.7-1.9
6-9	Understand the applications of diode in rectifiers with and without filters.	CLO 3	T1:1.11, 2.6-2.7
10-11	Understand the concept of breakdown mechanism in diodes with applications of Zener breakdown diodes.	CLO 4	T1:1.15, 2.10
12	Describe the classification family table of various transistors.	CLO 5	T1:3.1
13-16	Describe the concept of Bipolar Junction transistor with various modes of operation.	CLO 6	T1:3.2-3.8
17-20	Understand the concept of transistor biasing with various with voltage divider bias.	CLO 7	T1:4.1-4.5
21-22	Understand the construction and working of Field Effect Transistor(FET).	CLO 8	T1:6.1-6.3
22-24	Understand the concept of Metal Oxide Semiconductor FET.	CLO 9	T1:6.7-6.8
25	Illustrate the basic CMOS circuits.	CLO 10	T1:6.11
26-27	Understand the basic concepts of operational amplifiers.	CLO 11	T2:7.3.1
28-29	Analyze the parameters of practical and ideal op-amps.	CLO 12	T2:7.3.3
30	Understand the concept of virtual ground in op-amps.	CLO 13	T2:7.3.4
31-33	Perform basic arithmetic operations on voltages using opamps.	CLO 14	T2:7.4.3,7.4.4
34-35	Examine the working of op-amp as differentiator, integrator, comparator and buffer.	CLO 15	T2:7.4.5, 7.5.2-3
36-37	Understand the internal block diagram of 555 timer IC.	CLO 16	R1:16-7
38-39	Examine the working of 555 timer as astable and monostable multivibrator.	CLO 17	T2:9.5
40-41	Understand the principle of data conversions with terminology.	CLO 18	T2:10.2
42-46	Analyze the various analog to digital converters.	CLO 19	T2:10.3
47-49	Analyze the various resistor ladder digital to analog converters.	CLO 20	T2:10.5
50-53	Perform calculations in different number systems.	CLO 21	T2:8.2
54-55	Understand the basic concepts of Boolean algebra and combinational logic circuits.	CLO 22	T2:8.3-8.7
56-58	Understand the basic sequential logic circuits.	CLO 23	T2:9.2-9.3
59-60	Understand counters and registers.	CLO 24	T2:9.4

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs	Relevance With PSOs
1	Laboratory practice	Seminars / Online demonstrations	PO 1, PO 2	PSO 1

Prepared by:
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HOD, ECE