Hall Ticket No | | | | | | | | | | | Question Paper Code: BES003

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

M.Tech I Semester End Examinations (Regular) - February, 2018

Regulation: IARE–R16

COMPUTER ARCHITECTURE

(Embedded Systems)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Explain Amdahl's law in detail with suitable applications. **[7M]**
   (b) Explain different addressing modes for instruction set architecture with an example for each. **[7M]**

2. (a) Mention different types of control flow instructions, and explain the supporting addressing modes elaborating the parameters of evaluation. **[7M]**
   (b) Explain type and size of operands explaining their operation in the instruction set. **[7M]**

UNIT – II

3. (a) Explain hardware based speculation and limitations of instruction level parallelism. **[7M]**
   (b) Explain Tomasulo's algorithm with an example and give one real time application to it. **[7M]**

4. (a) Explain cross cutting issue of hardware versus software speculation. **[7M]**
   (b) What is instruction level parallelism? Elaborate instruction level parallelism concepts and challenges. **[7M]**

UNIT – III

5. (a) Which is more important for floating point programs: two-way set associativity or hit under one miss? Assume the following average miss rates for 8kB data cahes: 11.4% for floating-point programs with a direct-mapped cache, 10.7% for these programs with a two-way set-associative cache, 7.4% for integer programs with a direct-mapped cache and 6.0% for integer programs with a two-way set-associative cache. Assume the average memory stall time is just the product of the miss rate and the miss penalty and the cache describe for 16 clock cycles of L2 cache. **[7M]**
   (b) Explain how a protection is achieved via virtual memory. **[7M]**

6. (a) Explain about multi-threading concept with suitable examples. **[7M]**
   (b) What are the limitations in symmetric shared memory multiprocessors and snooping protocols? **[7M]**

UNIT – IV

7. (a) Explain different raid levels, with their fault tolerance and their overhead in redundant disks. **[7M]**

   (b) Explain characteristics of transaction processing council benchmarks. **[7M]**

8. (a) Discuss about I/O performance, reliability measures and bench marks. **[7M]**

   (b) Enumerate the steps to follow in designing an I/O system. Explain in detail. **[7M]**

UNIT – V

9. (a) Explain interconnecting network's practical problems in detail with an example. **[7M]**

   (b) Write a note on designing procedure of a cluster with an example. **[7M]**

10. (a) Interpret the interconnection network media. How it will affect the interconnection networking media. **[7M]**

    (b) Describe the various challenges of clusters and explain how to provide solutions to these challenges. **[7M]**