Hall Ticket No | | | | | | | | | | | Question Paper Code: BES005

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

M.Tech II Semester End Examinations (Regular) - July, 2017

Regulation: IARE–R16

FPGA ACHITECTURE AND APPLICATIONS

(Embedded Systems)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Explain the logic diagram of a typical sequential Programmable Array Logic, the 16R4. **[7M]**
   (b) Write a brief note on sharable expanders in CPLD. **[7M]**
2. (a) Explain the structure of Read-Only Memory consisting of n-input lines and m-output lines. **[7M]**
   (b) Explain the architecture of Xilinx cool runner XCR3064XL CPLD. **[7M]**

UNIT – II

3. (a) Briefly discuss the desirable properties of technological Programmable Elements in FPGAs. **[7M]**
   (b) Explain the general structure of FPGA chip consisting of a large number of programmable logic blocks surrounded by programmable I/O block. **[7M]**
4. (a) Give the comparison among different programmable connections in FPGA. **[7M]**
   (b) Briefly discuss different applications of FPGAs. **[7M]**

UNIT – III

5. (a) Briefly discuss the features of different families XC3000-series FPGAs. **[7M]**
   (b) Explain the architecture of XC4000-series FPGA highlighting different programmable logic blocks. **[7M]**
6. (a) Write a brief note on Static-RAM implementation of FPGA technology. **[7M]**
   (b) List the key features of XC2000-series FPGA architecture and explain different components of XC2000-series FPGA architecture. **[7M]**

UNIT – IV

7. (a) Explain the features of anti-fuse programmed FPGAs. **[7M]**
   (b) Explain the implementation of an ACT 1 logic module using pass transistors. **[7M]**
8. (a) Illustarte the routing architecture of an Actel ACT FPGA. **[7M]**
   (b) Briefly discuss the features of ACT-2 anti-fuse programmed FPGA. **[7M]**

UNIT – V

9. (a) Explain the architecture of a full page high-resolution display video controller. **[7M]**

   (b) Explain the design flow for Actel synthesis. **[7M]**

10. (a) Explain the concept of position tracking for a robot manipulator in controlling a high precision robot with 16 degrees of freedom. **[7M]**

    (b) With the help of diagram explain the architecture of high-speed DMA controller. **[7M]**

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