Hall Ticket No | | | | | | | | | | | Question Paper Code: BES005

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

M.Tech II Semester End Examinations (Regular / Supplementary) - July, 2018

Regulation: IARE–R16

FPGA ARCHITECURE AND APPLICATIONS

(ES)

Time: 3 Hours **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Implement the following boolean expressions using PAL **[7M]**
   $F_1(A, B, C) = A' + AB + BC$
   $F_2(A, B, C) = AC + AB$
   Also write PAL programmable table.
   (b) Draw and explain the general block diagram of CPLD. **[7M]**
2. (a) Distinguish between ROM, PLA and PAL. **[7M]**
   (b) What are advantages of CPLD over PLA and PAL? **[7M]**

UNIT – II

3. (a) With examples, explain about look up tables in FPGA. **[7M]**
   (b) Distinguish between Anti-fuse technology and SRAM technology. **[7M]**
4. (a) Implement the realization of Half Adder circuit using FPGA. **[7M]**
   (b) Explain the need of programmable interconnects in FPGA. **[7M]**

UNIT – III

5. (a) With a block diagram, explain about Xilinx 4000 series input/output block. **[7M]**
   (b) Explain about general purpose interconnect in Xilinx 3000 Series. **[7M]**
6. (a) With block diagram, explain about CLB block in Xilinx 3000 series. **[7M]**
   (b) With block diagram, explain about XC2000 series input/output block. **[7M]**

UNIT – IV

7. (a) Explain how Actel ACT-1 logic module acts as a boolean function generator. **[7M]**
   (b) Explain about Actel ACT-1 programmable interconnect architecture. **[7M]**
8. (a) Explain about sequential logic module of Actel ACT-2. **[7M]**
   (b) Explain about the speed performance of Actel ACT-1, 2, 3. **[7M]**

UNIT – V

9. (a) Explain the procedure of designing adders with ACT devices. **[7M]**

   (b) Write short notes on design issues in implementing a digital design. **[7M]**

10. (a) Describe the operation of fast video controller for a robot manipulator. **[7M]**

    (b) Write short notes on fast DMA controller mechanism with relavant block diagrams. **[7M]**

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