INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

ADVANCED COMPUTER ARCHITECTURE								
V Semester: CSE / IT								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
ACSD24	**Elective**	3	0	0	3	40	60	100
Contact Classes: 48	**Tutorial Classes: Nil**	**Practical Classes: Nil**				**Total Classes: 48**		
Prerequisite: There is no prerequisite to take this course								

I. COURSE OVERVIEW:

This course provides a comprehensive understanding of parallel computing architectures and models essential for high-performance computing. It begins with the evolution of parallel computer models and explores concepts of parallelism in programming, speedup performance laws, and system performance evaluation. The course delves into memory system design, cache organization, and bus architectures critical for data communication in multiprocessor systems. Advanced processor designs such as RISC, CISC, superscalar, VLIW, and SIMD are studied in detail, along with pipeline processing techniques. Students will also explore multiprocessor and multicomputer architectures, message-passing mechanisms, and interconnection networks. The final module cover data flow computing and VLSI-based computational models, including systolic arrays and reconfigurable architectures, enabling learners to design efficient parallel algorithms and systems.

II. COURSE OBJECTIVES:

The students will try to learn:

I. The principles of parallel computer models, including SIMD, MIMD, and PRAM architectures, and evaluate program parallelism using speedup performance laws such as Amdahl's and Gustafson's.

II. The memory hierarchy designs, including cache memory mapping techniques, interleaved shared memory, and bus-based communication for optimizing data access in parallel systems.

III. The advanced processor architectures (CISC, RISC, VLIW, Cray Y-MP), pipelined execution, inter-processor communication methods, and VLSI-based systolic and reconfigurable computing systems.

III. COURSE OUTCOMES:

At the end of the course students should be able to:

CO1 Describe parallel computer models and evaluate system performance using speedup laws such as Amdahl's Law, Gustafson's Law, and memory-bounded speedup models.

CO2 Analyze various memory hierarchy models, cache memory architectures, and shared memory organization techniques used in parallel systems.

CO3 Differentiate between instruction set architectures (CISC, RISC), and explain advanced processor designs such as superscalar, VLIW, and SIMD architectures.

CO4 Examine multiprocessor system interconnects, pipeline architectures, and message-passing mechanisms for efficient parallel processing.

CO5 Understand and apply concepts of data flow computing, including static and dynamic models, to parallel program execution.

CO6 Demonstrate the application of VLSI-based architectures like systolic arrays and reconfigurable processor arrays for solving matrix-based computations.

IV. COURSE CONTENT:

MODULE –I: PARALLEL COMPUTER MODELS (10)

Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl ‘s law, Gustafson ‘s law-Memory bounded speedup Model.

MODULE –II: MEMORY SYSTEMS AND BUSES (09)

Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Backplane bus systems-Bus addressing, arbitration and transaction.

MODULE –III: ADVANCED PROCESSORS: (09)

Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture.

Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication.

MODULE –IV: MULTI PROCESSOR AND MULTI COMPUTERS (10)

Multiprocessor system interconnects- Cross bar switch, Multiport Memory-Hot spot problem, Message passing mechanisms-Pipelined Processors-Linear pipeline, on linear pipeline Instruction pipeline design-Arithmetic pipeline design.

MODULE –V: DATA FLOW COMPUTERS AND VLSI COMPUTATIONS (10)

Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors-VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines.

V. TEXT BOOKS:

1. David E. Culler, Jaswinder Pal Singh, and Anoop Gupta. “Parallel Computer Architecture: A Hardware/Software Approach”, Part of: The Morgan Kaufmann Series in Computer Architecture and Design.

VI. REFERENCE BOOKS:

1. D. Sima, T. Fountain, P. Kacsuk, “Advanced Computer Architecture”, Addison-Wesley, 1997.
2. H.S. Stone, “High-performance Computer Architecture”, 3rd Edition, Addison-Wesley, 1993.

VII. ELECTRONICS RESOURCES:

1. https://nptel.ac.in/courses/106/103/106103206/
2. https://nptel.ac.in/courses/106/105/106105033/

VIII. MATERIALS ONLINE:

1. Course template
2. Tutorial question bank
3. Tech-talk topics
4. Open-ended experiments
5. Definitions and terminology
6. Assignments
7. Model question paper – I
8. Model question paper – II
9. Lecture notes