INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

DIGITAL SYSTEM DESIGN LABORATORY								
III Semester: ECE								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
AECD07	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		-	-	2	1	40	60	100
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 45**				**Total Classes: 45**		
Prerequisite:								

I. COURSE OVERVIEW:

The digital system design laboratory introduces the hardware description language for the design and development of digital integrated circuits and field programmable devices. It provides VHDL language elements, synthesizable register transfer logic models in structural, dataflow, behavioral modeling of combinational and sequential circuits. Includes applications in the area of VLSI system design.

II. COURSES OBJECTIVES:

The students will try to learn

I. The fundamental principles of the VHDL and its constructs used in design implementation of digital logic systems.

II. The concepts of behavioral, dataflow and structural modeling of fundamental digital logic circuits using VHDL.

III. The exposure to various stages of a typical state of the art CAD VLSI tool for simulation, synthesis, place and route, layout and power and clock routing module.

III. COURSE OUTCOMES:

At the end of the course students should be able to:

CO 1 Utilize the concept of Boolean algebra to verify the truth table of Boolean expressions using logic gates in Hardware Description Language.

CO 2 Make use of dataflow, structural and behavioral modelling styles of HDL for simulating the combinational logic circuits.

CO 3 Analyze the truth tables and characteristic equations of flip flops for the functional simulationand timing analysis of sequential circuits.

CO 4 Construct the synchronous and asynchronous sequential circuits using the flip flops.

CO 5 Model a finite state machine with melay and moore machines a finite state machine with melay and moore machines for detecting a given sequence.

CO 6 Examine the functionality of real time traffic light controller, chess clock controller FSM,elevator operations using HDL code.

IV. LIST OF EXPERIMENTS:

1. Getting Started Exercises

To be proficient in VHDL programming, you need to be able to operate on basic gates:

1. Basic gates realization
2. Realization of Product of Sum (POS) Boolean expression
3. Realization of Sum of Product (SOP) Boolean expression
4. Implementation of code conversions (gray to Boolean, Boolean to gray code)

2. Exercises on Gate Realization

To be skillful in VHDL programming, you need to be able to realize Boolean expressions using gates

1 Basic gates realization using NAND gate
2 Basic gates realization using NOR gate
3 XOR, XNOR gates realization using minimum number of NAND gates
4 Three input NAND gate using min no of 2 input NAND Gate

3. Exercises on Multiplexers and Demultiplexers

To be proficient in programming, you need implement the following data selector circuits:

1. Implementation of 2x1, 4x1 multiplexers, demultiplexers
2. Realization of higher order multiplexers using lower order multiplexers
3. Realization of basic gates using 2x1 multiplexer

4. Exercises on Decoders

To be proficient in programming, you need implement the following digital circuits

1. Implementation of 2 to 4 and 3 to 8 decoders
2. Realization of higher order decoders using lower order decoder
3. Design 7 segment display decoder circuit

5. Exercises on encoders and priority encoders

To be proficient in programming, you need implement the following digital circuits

1. Implementation of 4 to 2 encoders
2. Implementation of 8 to 3 encoders
3. Build 8 to 3 priority encoder
4. Realization of 8 to 3 priority encoder using 2x1 multiplexer

6. Exercises on Adders and Subtractors

To be proficient in programming, you need implement the following digital circuits

1. Implementation of half adder
2. Implementation of full adder
3. Realization of full adder using half adders
4. Design and implement 4-bit ripple carry adder
5. Implementation of half subtractor
6. Implementation of full subtractor
7. Realization of full subtractor using half subtractor
8. Realization of full subtractor using full adder

7. Exercises on barrel shifter and ALU

To be proficient in programming, you need implement the following digital circuits

1. Design a 4- bit barrel shifter with four select lines for supporting 16- functionalities
2. Implementation 8-bit ALU to perform the arithmetic, logical operations

8. Exercises on Latches and Flip-flops

To be proficient in programming, you need implement the following sequential logic circuits

1. Implementation of SR latch, JK latch, D latch and T latch
2. Implementation of SR flip-flop, JK flip-flop, D flip-flop and T flip-flop
3. Realization of D flip-flop using D latch
4. Realization of D flip-flop using JK flip-flop
5. Realization of T flip-flop using JK flip-flop
6. Realization of T flip-flop using D flip-flop

9. Exercises on counters and shift registers

To be proficient in programming, you need implement the following sequential logic circuits

1. Design 4-bit synchronous counter with synchronous reset
2. Design 4-bit synchronous counter with asynchronous reset
3. Design 4-bit asynchronous counter with synchronous reset
4. Design 4-bit asynchronous counter with asynchronous reset
5. Design decade counter
6. Design counter to count the events from 3 to 12
7. Design 4-bit serial in serial out shift register (SISO)
8. Design 4-bit serial in parallel out shift register (SIPO)
9. Design 4-bit parallel in serial out shift register (PISO)
10. Design 4-bit parallel in parallel out shift register (PIPO)

10. Exercises on case study: Pseudo random generator

To be proficient in programming, you need implement the following finite state machines

1 Pseudo random number generator using LFSR

2 Pseudo random number generator for CRC logic

11. Exercises on case study: CARRY-LOOK AHEAD ADDER

Develop a functional model of a 4-bit carry-look-ahead adder. The adder has two 4-bit data inputs, a(3 downto 0) and b(3 downto 0); a 4-bit data output, s(3 downto 0); a carry input, c_in; a carry output, c_out; a carry generate output, g; and a carry propagate output, p. The adder is described by the logic equations and associated propagation delays: where the Gi are the intermediate carry generate signals, the Pi are the intermediate carry propagate signals and the Ci are the intermediate carry signals. C–1 is c_in and C3 is c_out. Your model should use the expanded equation to calculate the intermediate carries, which are then used to calculate the sums.

12. Exercises on case study: VENDING MACHINE CONTROLLER

Vending-Machine Controller sells candy bars for 25 cents. The inputs are nickel_in, dime_in, and quarter_in, indicating the type of coin that was deposited, plus clock (clk) and reset (rst), to which the circuit responds with the outputs candy_out, to dispense a candy bar, plus nickel_out or dime_out, asserted when change is due. Design this circuit using the FSM approach. Also, estimate the number of flip-flops that will be required.

13. Exercises on case study: Gray-Encoded Counter

Gray-Encoded Counter

Design a 0-to-8 counter with Gray-encoded outputs.

a) Draw the state transition diagram.

b) Estimate the number of flip-flops that will be needed.

c) Write the VHDL code, then compile and simulate it.

d) Check whether the number of DFFs inferred by the compiler matches your prediction.

14. Exercises on case study: ROM DESIGN

Write an entity declaration for a lookup table ROM modeled at an abstract level. The ROM has an address input of type lookup_index, which is an integer range from 0 to 31, and a data output of type real. Include declarations within the declarative part of the entity to define the ROM contents, initialized to numbers of your choice.

EXERCISES FOR DIGITAL SYSTEM DESIGN LABORATORY

Note: Students are encouraged to bring their own laptops for laboratory practice sessions.

1. Getting Started Exercises

1.1 Basic Gates

1. Install Xilinx vivado on your machine.
2. Write a VHDL program using vivado simulator for:
   - Verifying the functionality of design under test (DUT) by writing test bench to pass the stimulus
   - Synthesize the register transfer logic (RTL)using Xilinx XST synthesis tool
   - Elaborate the design and generate bit file to dump RTL code into the Zynq series and Zed Board FPGA
   - Verify the functionality of the design under test (DUT) on FPGA board

1.2 AND-OR-INVERT AND OR-AND-INVERT LOGIC

Write VHDL code to implement the function expressed by the following logic equation

$$Y = \overline{a_0 b_0 + a_1 b_1 + a_2 b_2}$$

Use only simple signal assignment statements in your VHDL data flow model.

Hints

Use and, or and compliment operators for implementation of the logic.

```
Input a0, a1, a2, a3, b0, b1, b2, b3;
Output y;

/**Data  flow model for AOI logic */
entity AOI port (
        a0, a1, a2, a3, b0, b1, b2, b3: in std_logic;
         y: out std_logic);
end AOI;

/**architecture body  */
architecture arch_AOI of AOI is

begin
    Y = not ((a0 & b0) | (a1 & b1) | (a2 & b2) | (a3 & b3));
    . . .

End arch_AOI;

//Write the test bench for providing the stumulus

entity tb_AOI port
end tb_AOI;

architecture arch_AOI of AOI is
   signal a0, a1, a2, a3, b0, b1, b2, b3: std_logic := '0';
```

```
   signal y: std_logic;

   component AOI port (
        a0, a1, a2, a3, b0, b1, b2, b3: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: AOI port map (a0, a1, a2, a3, b0, b1, b2, b3, y);

   a0 = '0'; b0 = '0';
   a1 = '0'; b1 = '0';
   a2 = '0'; b2 = '0';
   a3 = '0'; b3 = '0';
   wait for 10 ns;

   a0 = '0'; b0 = '1';
   a1 = '1'; b1 = '0';
   a2 = '0'; b2 = '1';
   a3 = '1'; b3 = '0';
   wait for 10 ns;

   . . .
   . . .

   a0 = '1'; b0 = '1';
   a1 = '1'; b1 = '1';
   a2 = '1'; b2 = '1';
   a3 = '1'; b3 = '1';
   wait for 10 ns;

End architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design

Elaborate the design and dump the bit file into FPGA
```

Try

Develop a model for a general or-and-invert gate, with two std_logic_vector input ports a and b and a standard-logic output port y. The output of the gate is

1.3 Product of Sum Boolean expression

Write a program to perform product of sum which evaluates the given Boolean expressions and write the test-bench to verify the functionality with all possible combinations of the input.

Hints

```
/**
 * Consider the POS expression for F = π(0, 1,2,4,8,9,10,12,13) */
Input a, b, c, d;
Output F;

Minimize the logic for the given F          // POS logic
Implement the logic using basic gates

/**Declare the port signals */
entity POS port (
        a, b, c, d: in std_logic;
         f: out std_logic);
end POS;

/**architecture body  */
architecture arch_POS of POS is

Begin
    Y = F(a, b, c, d);
    . . .

End arch_POS;

//Write the test bench for providing the stumulus

entity tb_POS port
end tb_POS;

architecture arch_POS of POS is
   signal a, b, c, d: std_logic := ‘0’;
   signal f: std_logic;

   component POS port (
        a, b, c, d: in std_logic;
        f: out std_logic);
   end component;

begin
   DUT: POS port map (a, b, c, d, f);

   a = ‘0’; b =’0’; c = ‘0’; d =’0’;
   wait 10 ns;

a = ‘0’; b =’0’; c = ‘0’; d =’1’;
   wait 10 ns;

   . . .
   . . .

a = ‘1’; b =’1’; c = ‘1’; d =’1’;
   wait 10 ns;

End architecture


Provide the stimulus for all 16 possible combinations starting from 0000 to 1111
Simulate the DUT with the given stimulus
Verify the output using waveforms
Synthesize the design
```

```
Elaborate the design and dump the bit file into FPGA
```

Try

Modify the POS expression including the don't care cases F = π(0, 1,2,4,9,10,12,13) + d(3, 7, 11)

1.5Sum of Product Boolean expression

Write a program to perform sum of product which evaluates the given Boolean expressions and write the test-bench to verify the functionality with all possible combinations of the input.

Hints

```
/**
 * Consider the POS expression for F = Σ(0, 1,2,4,8,9,10,12,13) */
Input a, b, c, d;
Output F;

Minimize the logic for the given F          // POS logic
Implement the logic using basic gates

/**Declare the port signals */
entity SOP port (
        a, b, c, d: in std_logic;
         f: out std_logic);
end SOP;

/**architecture body  */
architecture arch_SOP of SOP is

Begin
    Y = F(a, b, c, d);
    . . .

End arch_SOP;

//Write the test bench for providing the stumulus

entity tb_SOP port
end tb_SOP;

architecture arch_SOP of SOP is
   signal a, b, c, d: std_logic := '0';
   signal f: std_logic;

   component SOP port (
        a, b, c, d: in std_logic;
         f: out std_logic);
   end component;

begin
   DUT: SOP port map (a, b, c, d, f);

   a = '0'; b ='0'; c = '0'; d ='0';
   wait 10 ns;

   a = '0'; b ='0'; c = '0'; d ='1';
   wait 10 ns;
```

```
   . . .
   . . .

   a = ‘1’; b =’1’; c = ‘1’; d =’1’;
   wait 10 ns;

End architecture

Simulate the DUT with the given stimulus

Verify the output using waveforms

Synthesize the design

Elaborate the design and dump the bit file into FPGA
```

Try

Modify the POS expression including the don’t care conditionsF = Σ(0, 1,2,4,9,10,12,13) + d(3, 7, 11)

1.6Code Conversions

To familiarize students with code converters. The student should also become familiar with gray to binary conversion, binary to gray conversion.
Given the sequence of three-bit Gray code as (000, 001, 011, 010, 110, 111, 101, 100)

A given Gray code number can be converted into its binary equivalent by going through the following steps:
1. Begin with the most significant bit (MSB). The MSB of the binary number is the same as the MSB of the Gray code number.
2. The bit next to the MSB (the second MSB) in the binary number is obtained by adding the MSB in the binary number to the second MSB in the Gray code number and disregarding the carry, if any.
3. The third MSB in the binary number is obtained by adding the second MSB in the binary number to the third MSB in the Gray code number. Again, carry, if any, is to be ignored.
4. The process continues until we obtain the LSB of the binary number.

Hints

```
/**Declare the port signals */
entity gray2binary port (
        gray_code: in std_logic_vector(3 downto 0);
         binary_code: out std_logic_vector(3 downto 0));
end gray2binary;

/**architecturebody  */
architecture arch_gray2binary of gray2binary is

Begin
    binary_code[3] = gray_code[3];
    binary_code[2] = gray_code[3] xor gray_code[2];
    . . .

End arch_gray2binary;

//Write the test bench for providing the stumulus
```

```
entity tb_gray2binary port
end tb_gray2binary;

architecture arch_gray2binary of gray2binary is
   signal gray_code: std_logic_vector(3 downto 0) := “0000”;
   signal binary_code: std_logic_vector(3 downto 0);

   component gray2binary port (
        gray_code: in std_logic_vector(3 downto 0);
         binary_code: out std_logic_vector(3 downto 0));
   end component;

begin
   DUT: gray2binary port map (gray_code, binary_code);

   Process
   begin
        gray_code = gray_code + 1;
        Wait for 10 ns;

   End process;

End architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design

Elaborate the design and dump the bit file into FPGA
```

Try

1. Design and implement the binary to gray code conversion
2. Design and implement the binary to excess 3-code conversion
3. Design and implement the excess 3-code to binary conversion

2. Exercises on Gate Realization

To be proficient in programming, you need to be able to :

1 Construct basic logic gates realization using NAND gates and NOR gates

2 Utilize min no of 2 input NAND Gates to implement three input NAND gate using

3 Build an user defined logic gate for the given specifications

2.1 Basic gates realization using NAND gate

Realize the inverter gate logic using NAND gate

NAND gate is actually a combination of two logic gates i.e. AND gate followed by NOT gate. So its output is complement of the output of an AND gate. This gate can have minimum two inputs. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, Ex-OR, Ex-NOR, NOR. So this gate is also called as universal gate.

Hint

```
/**Declare the port signals */
entity inv_nand port (
        i: in std_logic;
         y: out std_logic);
end inv_nand;

/**architecture body  */
architecture arch_inv_nand of inv_nand is

component nand_gate port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nand_gate port map (i, i, y);
    . . .

End arch_inv_gate;

//Write the test bench for providing the stumulus

entity tb_inv_nand port
end tb_inv_nand;

architecture arch_inv_nand of inv_nand is
   signal i: std_logic := '0';
   signal y: std_logic;

   component inv_nand port (
        i: in std_logic;
        y: out std_logic);
   end component;

begin
   DUT: inv_nand port map (i, y);

i ='0' after 10 ns;
i ='1' after 10 ns;

   . . .
   . . .

end architecture
```

Try

1. Realize the AND gate logic using NAND gate
2. Realize the OR gate logic using NAND gate

2.2 Gate realization using NOR gate

Realize the inverter gate logic using NOR gate

Hint

```
/**Gate level model for */
entity inv_nor port (
        i: in std_logic;
         y: out std_logic);
end inv_nor;

/**architecture body  */
architecture arch_inv_nor of inv_nand is

component nor_gate port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nor_gate port map (i, i, y);
    . . .

End arch_inv_nor;

//Write the test bench for providing the stumulus

entity tb_inv_nor port
end tb_inv_nor;

architecture arch_inv_nor of inv_nor is
   signal i: std_logic := '0';
   signal y: std_logic;

   component inv_nor port (
        i: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: inv_nor port map (i, y);

   i ='0' after 10 ns;
   i ='1' after 10 ns;

   . . .
   . . .

End architecture
```

Try

1. Realize the AND gate logic using NOR gate
2. Realize the OR gate logic using NOR gate

2.3 XOR gate realization using minimum number of NAND gates

Realize XOR gate using minimum number of NAND gates

Hint

```
/**Declare the port signals */
entity xor_nand port (
        a, b: in std_logic;
         y: out std_logic);
end xor_nand;

/**architecture body  */
architecture arch_xor_nand of xor_nand is

component nand_gate port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nand_gate port map (a, b, y);
    . . .

End arch_xor_nand;

//Write the test bench for providing the stumulus

entity tb_xor_nand port
end tb_xor_nand;

architecture arch_xor_nand of xor_nand is
   signal a, b: std_logic := '0';
   signal y: std_logic;

   component xor_nand port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: xor_nand port map (a, b, y);

a ='0' after 10 ns;
b ='0' after 10 ns;

   . . .
   . . .

End architecture
```

Try

1. Realize XNOR gate using minimum number of NAND gates

2.4 Three input NAND gate using min no of 2 input NAND Gate

To implement 3 input NAND gate realization using minimum number of NAND gates

```
a) A and B to the first NAND gate
b) Output of first Nand gate is given to the two inputs of the second NAND gate
(this basically realizes the inverter functionality)
```

c) Output of second NAND gate is given to the input of the third NAND gate, whose otherinput is C ((A NAND B) NAND (A NAND B)) NAND C Thus, can be implemented using '3'2-input NAND gates.

Hints:

Assume three inputs of the NAND gate are A, B and C and connect these inputs as

```
/**Declare the port signals */
entity nand3 port (
        a, b, c: in std_logic;
         y: out std_logic);
end nand3;

/**architecture body  */
architecture arch_nand3 of nand3 is

component nand2_gate port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nand2_gate port map (a, b, y);
    . . .

End arch_nand3;

//Write the test bench for providing the stumulus

entity tb_nand3 port
end tb_nand3;

architecture arch_tb_nand3 of tb_nand3 is
   signal a, b: std_logic := ‘0’;
   signal y: std_logic;

   component nand2 port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nand2 port map (a, b, y);

   a =’0’ after 10 ns;
   b =’0’ after 10 ns;

   . . .
   . . .

   a = ‘1’ after 10 ns;
   b = ‘1’ after 10 ns;

End architecture
```

Try:

To implement XNOR gate realization using minimum number of NAND gates

2.5 User defined logic gate (Muller-C element cell)

Develop a behavioral model for a two-input Muller-C element cell, with two input ports and one output, all of type bit. The inputs and outputs are initially '0'. When both inputs are '1', the output changes to '1'. It stays '1' until both inputs are '0', at which time it changes back to '0'. Your model should have a propagation delay for rising output transitions of 3.5 ns, and for falling output transitions of 2.5 ns.

Hints:

Assume three inputs of the NAND gate are A, B and C and connect these inputs as

```
Take inputs A and B
Extract the truth table and Boolean expression as per the specifications
Implement the gate using VHDL model
Write the logic for selecting the stimulus for verifying the logic

/**Declare the port signals */
entity mc_cell port (
        a, b, c: in std_logic;
         y: out std_logic);
end mc_cell;

/**architecture body  */
architecture arch_mc_cell of mc_cell is

component mc_cell port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: nand2_gate port map (a, b, y);
    . . .

End arch_mc_cell;

//Write the test bench for providing the stumulus

entity tb_mc_cell port
end tb_mc_cell;

architecture arch_tb_mc_cell of tb_mc_cell is
   signal a, b: std_logic := '0';
   signal y: std_logic;

   component mc_cell port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: mc_cell port map (a, b, y);

   a ='0' after 10 ns;
   b ='0' after 10 ns;

   . . .
   . . .

   a = '1' after 10 ns;
   b = '1' after 10 ns;
```

```
End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

Develop a behavioral model for a two-input Muller-C element cell, with two input ports and one output, all of type bit. The inputs and outputs are initially '1'. When both inputs are '0', the output changes to '0'. It stays '0' until both inputs are '1', at which time it changes back to '1'.

3. Exercises on Multiplexers and Demultiplexers

To be proficient in programming, you need implement the following digital circuits:

1. Implementation of 2x1, 4x1 multiplexers, demultiplexers
2. Realization of higher order multiplexers using lower order multiplexers
3. Realization of basic gates using 2x1 multiplexer

3.1 Implementation of 2x1, 4x1 multiplexers

Develop a behavioral model for a two-input multiplexer, with ports of type bit and a propagation delay from data or select input to data output of 5 ns. You should declare a constant for the propagation delay, rather than writing it as a literal in signal assignments in the model

The inputs to the MUX are data inputs I1, I0 and a one control input SEL(s) The single output is Y

Hints

```
/**Implementation of 2x1 multiplexer**/

Declare the inputs I0, I1 and S
Declare the output Y.

//Write the logic for selecting the data depends on the select line and pass
to the output

entity mux_2x1 port (
        i0, i1, s: in std_logic;
         y: out std_logic);
end mux_2x1;

/**architecture body  */
architecture arch_mux_2x1 of mux_2x1 is

   component nand port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

   component inv port (
```

```
         i: in std_logic;
          y: out std_logic);
   end component;

begin
   DUT1: inv port map (s, sb);
   DUT2: nand2_gate port map (i0, sb, s1); . . .

   . . .
   . . .

End arch_mux2x1;

//Write the test bench for providing the stumulus

entity tb_mux2x1 port
end tb_mux2x1;

architecture arch_tb_mux2x1 of tb_mc_mux2x1 is
   signal i0, i1, s: std_logic := '0';
   signal y: std_logic;

   component mux2x1 port (
        i0, i1, s: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: mux2x1 port map (i0, i1, s, y);

   s ='0' after 10 ns, '1' after 10 ns;
   process
   begin
     i0 = ~i0;
     wait for 10ns;
     i1 = ~i1;
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA


Plot the wave form for all possible select lines

Synthesize the design

Elaborate the design and dump the bit file into FPGA
```

Try

Develop a behavioral model for a four-input multiplexer, with ports of type bit and a propagation delay from data or select input to data output of 4.5 ns. You should declare a constant for the propagation delay, rather than writing it as a literal in signal assignments in the model.

3.2 Implementation of 2x1, 4x1 de multiplexers

Build a behavioral model for a two-input de multiplexers, with ports of type bit and a propagation delay from data or select input to data output of 5 ns.

Hints

```
/**
Implementation of 2x1 demultiplexer.
**/

Declare the inputs I and S
Declare the output Y0, Y1.

//Write the logic for selecting the data depends on the select line and pass
to the output

entity dmux_1x2 port (
        i, s: in std_logic;
         y0, y1: out std_logic);
end dmux_1x2;

/**architecture body  */
architecture arch_dmux_1x2 of dmux_1x2 is

begin
   process(I,s)
   begin
      case S is
        when '0': y0 = I; y1 = 'z';
   . . .
   . . .

End arch_dmux1x2;

//Write the test bench for providing the stumulus

entity tb_dmux1x2 port
end tb_dmux1x2;

architecture arch_tb_dmux1x2 of tb_dmux1x2 is
   signal i, s: std_logic := '0';
   signal y0, y1: std_logic;

   component dmux1x2 port (
        i, s: in std_logic;
         y0, y1: out std_logic);
   end component;

begin
   DUT: dmux1x2 port map (i, s, y0, y1);

   s ='0' after 10 ns, '1' after 10 ns;
```

```
   process
   begin
     i = ~i;
     wait for 10ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA


Plot the wave form for all possible select lines

Synthesize the design

Elaborate the design and dump the bit file into FPGA
```

Try

1 Modify the program to function as 1x4demultiplexers

2 Modify the program to function as 1x8 demultiplexers

3.3 Realization of higher order multiplexers using lower order multiplexers

Realize the higher order multiplexers using lower order multiplexers. Write the VHDL model for the realized circuits. Simulate the test benches for the corresponding and verify the design under test by plotting the wave forms. Figure 1 shows realization of 4x1 mux using 2x1 mux.

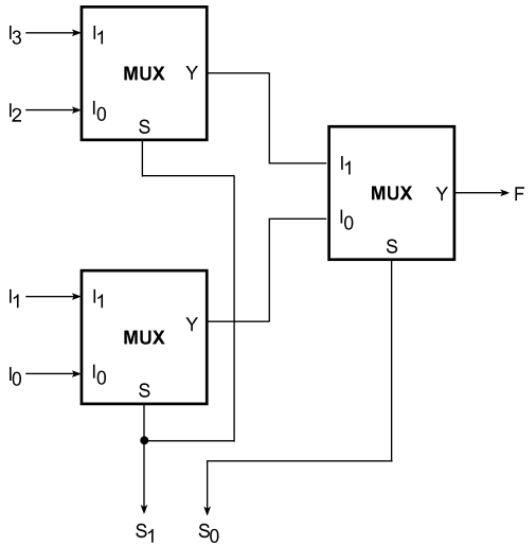

Figure 1: Realization of 4x1 mux using 2x1 mux

```
/**
 Realize the lower order multiplexers for design of higher order multiplexers.
**/

In work library simulate the lower order multiplexer
```

For the realized higher order multiplexer, instance the component in the declaration part of the architecture

By using positional or name mapping instance the component with the signals

Hint

```
//Write the logic for selecting the data depends on the select line and pass to the output

entity mux_4x1 port (
        i0, i1, i2, i3: in std_logic;
         s: in std_logic_vector(1 donwto 0);
         y: out std_logic);
end mux_4x1;

/**architecture body  */
architecture arch_mux_4x1 of mux_4x1 is

   component mux2x1 port (
        i0, i1, s: in std_logic;
         y: out std_logic);
   end component;
   // declare intermediate signals

begin
   DUT1: mux2x1 port map (i0, i1, s(0), s1);
   DUT2: mux2x1 port map (i2, i3, s(1), s2);
   . . .
   . . .
   . . .

End arch_mux4x1;

//Write the test bench for providing the stumulus

entity tb_mux4x1 port
end tb_mux4x1;

architecture arch_tb_mux4x1 of tb_mux4x1 is
   signal i0, i1, i2, i3: std_logic := '0';
   signal s: std_logic_vector(1 donwto 0) := "00";
   signal y: std_logic;

   component mux4x1 port (
        i0, i1, i2, i3: in std_logic;
         s: in std_logic_vector(1 donwto 0);
         y: out std_logic);
   end component;

begin
   DUT: mux4x1 port map (i0, i1, i2, i3, s, y);

   s ='00' after 10 ns, '01' after 10 ns . . .;
   process
   begin
     i0 = ~i0;
     wait for 10ns;
     i1 = ~i1;
```

```
     wait for 12ns;
     i2 = ~i2;
     wait for 14ns;
     i3 = ~i3;
     wait for 16ns;
   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

3.4 Realization of basic gates using 2x1 multiplexer

Realize all the basic gates like AND and inverter using 2x1 multiplexer

```
/** Realize the multiplexers for function as basic logic gates **/

In work library simulate the 2x1 multiplexer

For the realized basic gates using 2x1 multiplexer, instance the component in the
declaration part of the architecture
```

Hints

```
//Write the logic for selecting the data depends on the select line and pass
to the output

entity mux_and port (
        a, b: in std_logic;
         y: out std_logic);
end mux_2x1;

/**architecture body  */
architecture arch_mux_and of mux_and is

   component mux2x1 port (
        i0, i1, s: in std_logic;
         y: out std_logic);
   end component;
   // declare intermediate signals

begin
   DUT1: mux2x1 port map (‘0’, b, a, y);
   . . .
   . . .
   . . .

End arch_mux_and;

//Write the test bench for providing the stumulus

entity tb_mux_and port
end tb_mux_and;

architecture arch_tb_mux_and of tb_mux_and is
   signal a, b: std_logic := ‘0’;
   signal y: std_logic;
```

```
   component mux_and port (
        a, b: in std_logic;
         y: out std_logic);
   end component;

begin
   DUT: mux_and port map (a, b, y);

   process
   begin
a = ~a;
     wait for 10ns;
b = ~b;
     wait for 12ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

1. Realize all the OR gate using 2x1 multiplexer
2. Realize all the basic gates like XOR and XNOR using 2x1 multiplexer
3. Realize all the inverter using 2x1 multiplexer

4. Exercises on decoders

To be proficient in programming, you need implement the following digital circuits

1. Implementation of 2 to 4 and 3 to 8 decoders
2. Realization of higher order decoders using lower order decoders
3. Develop a functional model of a BCD-to-seven-segment decoder for a light emitting diode (LED) display.

4.1 Implementation of 2 to 4 decoder

Write the VHDL code for the circuit contains an input bundle of two input signals and anoutput bundle of four decoded signals. The input bundle, i_0, i_1 represents decoder inputs. The output bus, Y0, Y1, Y2 and Y3, are used to indicate the decoded output for the two inputs. The relationship betweenthe input and output is shown in the table below. Use a selected signalassignment statement in the solution.

```
/**
Implementation of 2 to 4 decoder.
**/

Declare the inputs I0, I1.
Declare the output Y0, Y1, Y2 and Y3.

I1      I0      Y3      Y2      Y1      Y0
0       0       0       0       0       1
0       1       0       0       1       0
1       0       0       1       0       0
1       1       1       0       0       0
```

Hints

```
//Write VHDL model for 2 to 4 decoder gate level model
entity dec2to4 port (
        i0, i1: in std_logic;
         y0, y1, y2, y3: out std_logic);
end dec2to4;

/**architecture body  */
architecture arch_dec2to4 of dec2to4 is

   component nand_gate port (
         a, b: in std_logic;
          y: out std_logic);
   end component;
    // component declaration for inverter
   // declare intermediate signals

begin
   DUT1: nand_gate port map (ni1, ni0, y0);
   . . .
   . . .
   . . .

End arch_dec2to4;

//Write the test bench for providing the stumulus

entity tb_dec2to4 port
end tb_dec2to4;

architecture arch_tb_dec2to4 of tb_dec2to4 is
   signal i0, i1: std_logic := '0';
   signal y0, y1, y2, y3: std_logic;

   component dec2x4 port (
         i0, i1: in std_logic;
          y0, y1, y2, y3: out std_logic);
   end component;

begin
   DUT: dec2to4 port map (i0,i1, y0, y1, y2, y3);

   process
   begin
i0 = ~i0;
     wait for 10ns;
i1 = ~i1;
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

1. Write a program to implement gate level model for 2 to 4 decoder. Plot the waveforms
2. Write a program to implement behavioral model for 2 to 4 decoder. Plot the waveforms

4.2 Implementation of 3 to 8 decoder

Build behavioral model to function as 3 to 8 decoder.

Hints

```
/** Behavioral model implementation of 3 to 8 decoder**/
Declare the inputs I0, I1, I2.
Declare the output Y0, Y1, Y2, Y3, Y4, Y5, Y6 and Y7.

//Write VHDL model for 2 to 4 decoder gate level model
entity dec3to8 port (
        i0, i1, i2: in std_logic;
         y0, y1, y2, y4, y5, y6, y7: out std_logic);
end dec3to8;

/**architecture body  */
architecture arch_dec3to8 of dec3to8 is

   // declare intermediate signals

begin
process(i0, i1, i2)
   begin
      {y0, y1, y2, y4, y5, y6, y7} = “00000000”;

      case {i2, i1, i0} is
        when “000” => Y0 <= ‘1’;
        when “001” => Y0 <= ‘1’;
        when “010” => Y0 <= ‘1’;
        . . .
        . . .
        . . .
      End case
   End process;

End arch_dec3to8;

//Write the test bench for providing the stumulus

entity tb_dec3to8 port
end tb_dec3to8;

architecture arch_tb_dec3to8 of tb_dec3to8 is
   signal i0, i1, i2: std_logic := ‘0’;
   signal y0, y1, y2, y3, y4, y5, y6, y7: std_logic;

   component dec3x8 port (
        i0, i1, i2: in std_logic;
         y0, y1, y2, y3, y4, y5, y6, y7: out std_logic);
   end component;

begin
   DUT: dec3to8 port map (i0,i1, i2, y0, y1, y2, y3, y4, y5, y6, y7);
```

```
   process
   begin
     i0 = ~i0;
     wait for 10ns;
     i1 = ~i1;
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

1. Construct a 4-to-16 line decoder with two 3-to-8 line decoders having active LOW ENABLE inputs
2. Implement the three-variable Boolean function $F = \bar{a}c + a\bar{b}c + a\bar{b}c$using (i) an 8-to-1 multiplexer and (ii) a 4-to-1 multiplexer.

4.3

Construct a 4-to-16 line decoder with two 3-to-8 line decoders having active LOW ENABLE inputs

Try

Construct a 3-to-8 line decoder with two 2-to-4 line decoders having active LOW ENABLE inputs

Try

Realization of BCD-to-seven-segment decoder for a light emitting diode (LED) display

Develop a functional model of a BCD-to-seven-segment decoder for a lightemitting diode (LED) display. The decoder has a 4-bit input that encodes a numeric digit between 0 and 9. There are seven outputs indexed from 'a' to 'g', corresponding to the seven segments of the LED display as shown in the margin. An output bit being '1' causes the corresponding segment to illuminate. For each input digit, the decoder activates the appropriate combination of segment outputs to form the displayed representation of the digit.

Hint:

For example, for the input "0010", which encodes the digit 2, the output is "1101101". Your model should use a selected signal assignment statement to describe the decoder function in truth-table form

5. Exercises on encoders and priority encoders

To be proficient in programming, you need implement the following digital circuits

1. Implementation of 4 to 2 encoders
2. Implementation of 8 to 3 encoders
3. Build 8 to 3 priority encoder
4. Realization of 8 to 3 priority encoder using 2x1 multiplexer

5.1 Implementation of 4 to 2 encoder

An encoder is a digital circuit that converts a set of binary inputs into a unique binary code. The binary code represents the position of the input and is used to identify the specific input that is active. Encoders are commonly used in digital systems to convert a parallel set of inputs into a serial code.

The 4 to 2 Encoder consists of four inputs Y3, Y2, Y1 & Y0, and two outputs A1 & A0. At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The figure below shows the logic symbol of the 4 to 2 encoder.

```
/**Implementation of 4 to 2 decoder **/

Declare the inputs I0, I1, I2, I3.
Declare the output Y0 and Y1

I3      I2      I1      I0      Y1      Y0
0       0       0       1       0       0
0       0       1       0       0       1
0       1       0       0       1       0
1       0       0       0       1       1
```

Hints

```
//Write VHDL model for 2 to 4 decoder gate level model
entity enc4to2 port (
    i : in STD_LOGIC_VECTOR(3 downto 0);
   y : out STD_LOGIC_VECTOR(1 downto 0) );
end enc4to2;

architecture arch_enc4to2 of enc4to2 is
begin

    process(i)
begin
        if (i="1000") then y<= "00";
        elsif (i="0100") then y<= "01";
        elsif (i="0010") then y<= "10";
        elsif (i="0001") then y<= "11";
        else  y<= "ZZ";
        end if;
end process;

End arch_enc4to2;

//Write the test bench for providing the stumulus

entity tb_enc4to2 port
end tb_enc4to2;

architecture arch_tb_enc4to2 of tb_enc4to2 is
   signal i : in STD_LOGIC_VECTOR(3 downto 0) := “0000”;
  signal y : out STD_LOGIC_VECTOR(1 downto 0);

   component enc4to2 port (
        i : in STD_LOGIC_VECTOR(3 downto 0);
         y : out STD_LOGIC_VECTOR(1 downto 0));
   end component;

begin
   DUT: enc4to2 port map (i, y);
```

```
   process
   begin
     i = i + '1';
     wait for 10ns;
   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

1. Modify VHDL behavioral model with gate level model for 4 to 2encoder. Plot the waveforms

2. Decimal to BCD Encoder
   The decimal-to-binary encoder usually consists of 10 input lines and 4 output lines. Each input line corresponds to each decimal digit and 4 outputs correspond to the BCD code. This encoder accepts the decoded decimal data as an input and encodes it to the BCD output which is available on the output lines.

3. Octal to Binary Encoder (8 to 3 Encoder)
   The 8 to 3 Encoder or octal to Binary encoder consists of 8 inputs: Y7 to Y0 and 3 outputs: A2, A1 & A0. Each input line corresponds to each octal digit and three outputs generate corresponding binary code.

5.2 Implementation of 8 to 3 priority encoder

A 8 to 3 priority encoder has eight inputs Y7, Y6, Y5, Y4, Y3, Y2, Y1 & Y0 and two outputs A2, A1 and A0. Here, the input, Y7 has the highest priority, whereas the input, Y0 has the lowest priority. In this case, even if more than one input is '1' at the same time, the output will be the binarycode corresponding to the input, which is having higher priority.
We considered one more output, V in order to know, whether the code available at outputs is valid or not.

- If at least one input of the encoder is '1', then the code available at outputs is a valid one. In this case, the output, V will be equal to 1.
- If all the inputs of encoder are '0', then the code available at outputs is not a valid one. In this case, the output, V will be equal to 0.

The Truth table of 4 to 2 priority encoder is shown below.

```
/**Implementation of 4 to 2 decoder **/

Declare the inputs I0, I1, I2, I3.
Declare the output Y0 and Y1

I3      I2      I1      I0      Y1      Y0
0       0       0       1       0       0
0       0       1       0       0       1
0       1       0       0       1       0
1       0       0       0       1       1
```

Hints


```
//Write VHDL model for 2 to 4 decoder gate level model
```

```
entity penc8to3 port (
    i : in STD_LOGIC_VECTOR(7 downto 0);
   y : out STD_LOGIC_VECTOR(2 downto 0) );
end enc4to2;

architecture arch_penc8to3of penc8to3 is
begin

y<="111" when i(7)='1' else
        "110" when i(6)='1' else
        "101" when i(5)='1' else
        "100" when i(4)='1' else
        "011" when i(3)='1' else
        "010" when i(2)='1' else
        "001" when i(1)='1' else
        "000" ;

End arch_penc8to3;

//Write the test bench for providing the stumulus

entity tb_penc8to3 port
end tb_penc8to3;

architecture arch_tb_penc8to3 of tb_penc8to3 is
   signal i : in STD_LOGIC_VECTOR(7 downto 0) := “00000000”;
  signal y : out STD_LOGIC_VECTOR(2 downto 0);

   component penc8to3 port (
        i : in STD_LOGIC_VECTOR(7 downto 0);
         y : out STD_LOGIC_VECTOR(2 downto 0));
   end component;

begin
   DUT: penc8to3 port map (i, y);

   process
   begin
     i = i + ‘1’;
     wait for 10ns;
   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

Try

1. Modify VHDL behavioral model with gate level model for 8 to 3 encoder. Plot the waveforms.
2. Realize 8to3 priority encoder using 2x1 mux and implement with VHDL gate level model.

6. Exercises on Adders and Subtractors

To be proficient in programming, you need implement the following digital circuits

1 Implementation of half adder
2 Implementation of full adder

3 Realization of full adder using half adder
4 Design and implement 4-bit ripple carry adder
5 Implementation of half subtractor
6 Implementation of full subtractor
7 Realization of full subtractor using half subtractor
8 Realization of full subtractor using full adder

6.1 Implementation of half adder

Design a gate level circuit for half adder and verify for the following truth table and write a test bench for verifying the functionality of the ha1f adder.
A half adder has two inputs for the two bits to be added and two outputs one from the sum ' S' and other from the carry ' c' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

```
Consider the inputs are A, B and outputs are Sum, Cout
A       B       Sum     Cout
0       0       0       0
0       1       1       0
1       0       1       0
1       1       0       1
```

Hints

The *code pattern* for implementinghalf adder:

```
// Declare the port signals
Input a, b;
Output sum, cout

//Write VHDL model for half adder in behavioral flow model
entity ha_df port (
        a, b: in std_logic;
         sum, cout: out std_logic);
end ha_df;

/**architecture body  */
architecture arch_ha_df of ha_df is

begin
   process(a, b)
   begin

      case {a, b} is
        when “00” => sum <= ‘0’; cout <= ‘0’;
        when “01” => sum <= ‘1’; cout <= ‘0’;
        when “10” => sum <= ‘1’; cout <= ‘0’;
        . . .
        . . .
        . . .
      End case
   End process;

End arch_ha_df;

//Write the test bench for providing the stumulus
```

```
entity tb_ha_df port
end tb_ha_df;

architecture arch_tb_ha_df of tb_ha_df is
   signal a, b: std_logic := '0';
   signal sum, cout: std_logic;

   component ha_df port (
          a, b: in std_logic;
          sum, cout: out std_logic);
   end component;

begin
   DUT: ha_df port map (a, b, sum, cout);

   process
   begin
a = ~a;
     wait for 10ns;
b = ~b;
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

6.2 Implementation of full adder

Design a gate level circuit for full adder and verify for the following truth table and write a test bench for verifying the functionality of the full adder

```
Consider the inputs are A, B, C and outputs are Sum, Cout

A       B       C       Sum     Cout
0       0       0       0       0
0       0       1       1       0
0       1       0       1       0
0       1       1       0       1
1       0       0       1       0
1       0       1       0       1
1       1       0       0       1
1       1       1       1       1
```

Hints

The pseudo *code* for printing full adder:

```
// Declare the port signals
Input a, b, c;
Output sum, cout
Work lib should consists of xor, and, or gates modules
```

```
//Write VHDL model for half adder in behavioral flow model
entity fa_gl port (
        a, b, cin: in std_logic;
         sum, cout: out std_logic);
end fa_gl;

/**architecture body  */
architecture arch_fa_gl of ga_gl is
   component xor_gate port (
         a, b: in std_logic;
         y: out std_logic);
   end component;

    component declaration for or_gate, and_gate
begin

    u0: xor_gate port map(a, b, x1);
    u1: xor_gate port map(x1, cin, sum);
    . . .
    . . .

End arch_fa_gl;

//Write the test bench for providing the stumulus

entity tb_fa_gl port
end tb_fa_gl;

architecture arch_tb_fa_gl of tb_fa_gl is
   signal a, b, cin: std_logic := '0';
   signal sum, cout: std_logic;

   component fa_gl port (
         a, b, cin: in std_logic;
         sum, cout: out std_logic);
   end component;

begin
   DUT: fa_gl port map (a, b, cin, sum, cout);

   process
   begin
     a = ~a;
     wait for 5ns;
     b = ~b;
     wait for 10ns;
cin = ~cin;
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```


6.3 Realization of full adder using half adders

Design a gate level circuit for full adder using half adder and verify for the functionality and write a test bench for verifying the functionality of the full adder

Hints

The pseudo *code* for printing full adder:

```
// Declare the port signals
Input a, b, c;
Output sum, cout

Work lib should consists of half adder, or_gate modules

entity fa_ha port (
        a, b, cin: in std_logic;
         sum, cout: out std_logic);
end fa_ha;

/**architecture body  */
architecture arch_fa_ha of ga_ha is
   component ha_df port (
         a, b: in std_logic;
         y: out std_logic);
   end component;

    component declaration for or_gate, and_gate
begin

    u0: xor_gate port map(a, b, x1);
    u1: xor_gate port map(x1, cin, sum);
    . . .
    . . .
End arch_fa_gl;

//Write the test bench for providing the stumulus

entity tb_fa_gl port
end tb_fa_gl;

architecture arch_tb_fa_gl of tb_fa_gl is
   signal a, b, cin: std_logic := '0';
   signal sum, cout: std_logic;

   component fa_gl port (
         a, b, cin: in std_logic;
         sum, cout: out std_logic);
   end component;

begin
   DUT: fa_gl port map (a, b, cin, sum, cout);

   process
   begin
     a = ~a;
     wait for 5ns;
     b = ~b;
     wait for 10ns;
     cin = ~cin;
```

```
     wait for 15ns;

   end process

End architecture

Plot the wave form for all possible select lines
Synthesize the design
Elaborate the design and dump the bit file into FPGA
```

6.4 Design and implement 4-bit ripple carry adder

Design a gate level circuit for ripple carry adder using full adder and verify for the functionality and write a test bench for verifying the functionality of the ripple carry adder

Hints

The pseudo *code* for printing full adder:

```
// Declare the port signals
Input a, b;      //vector of 4-bit size
Input cin;
Output sum;      //vector of 4-bit size
Output cout;

// Declare xor gate, and gate
Component declaration for full adder

// instance xor gate, and gate
Port map for full adder
```

6.5 Implementation of half subtractor

Design a gate level circuit for half subtractor and verify for the following truth table and write a test bench for verifying the functionality of the ha1f subtractor

```
Consider the inputs are A, B and outputs are Diff, Bout

A       B       Diff    Bout
0       0       0       0
0       1       1       1
1       0       1       0
1       1       0       0
```

Hints

The *code pattern* for printing half subtractor:

```
// Declare the port signals
Input a, b;
Output diff, bout
```

```
// Declare xor gate, and gate
Component declaration for xor gate, and gate

// instance xor gate, and gate
Port map for xor gate
Port map for and gate
```

6.6 Implementation of fullsubtractor

Design a gate level circuit for full subtractor and verify for the following truth table and write a test bench for verifying the functionality of the full subtractor

```
Consider the inputs are A, B, Bin and outputs are Diff, Bout

A       B       Bin     Sum     Bout
0       0       0       0       0
0       0       1       1       1
0       1       0       1       1
0       1       1       0       1
1       0       0       1       0
1       0       1       0       0
1       1       0       0       0
1       1       1       1       1
```

Hints

The pseudo *code* for printing full subtractor:

```
// Declare the port signals
Input a, b, bin;
Output diff, bout

// Declare xor gate, and gate
Component declaration for xor gate, and gate

// instance xor gate, and gate
Port map for xor gate
Port map for and gate
```

6.7 Realization of full subtractor using half subtractor

Design a gate level circuit for full subtractor using half subtractorand verify for the functionality and write a test bench for verifying the functionality of the full subtractor

Hints

The pseudo *code* for printing full subtractor:

```
// Declare the port signals
Input a, b, bin;
Output diff, bout

// Declare xor gate, and gate
Component declaration for half subtractor, and gate, or gate

// instance xor gate, and gate
Port map for half subtractor
Port map for and gate
```

```
Port map for or gate
```

Try

Design a gate level circuit for ripple carry adder using full adder and verify for the functionality and write a test bench for verifying the functionality of the ha1f adder

Hints

The pseudo *code* for printing full adder:

```
// Declare the port signals
Input a, b;      //vector of 4-bit size
Input cin;
Output sum;      //vector of 4-bit size
Output cout;

// Declare xor gate, and gate
Component declaration for full adder

// instance xor gate, and gate
Port map for full adder
```

7. Exercises on barrel shifter and ALU

To be proficient in programming, you need implement the following digital circuits

1. Design a 4- bit barrel shifter with four select lines for supporting 16- functionalities
2. Implementation 8-bit ALU to perform the arithmetic, logical operations

7.1. 4- bit barrel shifter

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without use of any sequential logic, only pure combinational logic. There are 3 type of bitwise shift operation: logical shift, arithmetic shift, and circular shift (rotate). The data can be shifted to the left as well as to the right circular shift.

Hints

Consider the port specification as
Input datain // 8 bit wide
Input sel // 3 bit wide to support 16 operations
Input dataout // 8 bit wide

The circuit allows rotating the input data word right, where the amount of rotating is selected by the controlinputs. The circuit can design by three stages of 2:1 multiplexer.

When all multiplexer select inputs are active (low), the input data passes straight through the cascade of themultiplexers and the output data (q_7.....q_0) is equal to the input data (d_7..... d_0). When S_2control signal isselected, the first stage of multiplexers performs a rotate-right by one bit operation, due to theirinter-connection to the next lower input.

The second stage of multiplexers performs a rotate-right by two bits whenS_1 control signal is selected. Here the corresponding multiplexer inputs are connected to their second next-lower input.

Finally, the third stage of multiplexers performs a rotate-right by four bits, when S_0 control signal isselected. The design uses a case statement to exhaustively list all combinations of the amt signal and thecorresponding rotated results.

Try:

1. Modify the barrel shifter by changing the number of select lines to 4 bit wide to support 16 different functionalities.
2. Modify the barrel shifter by changing the number of data lines to 16 bit wide to support 16 different functionalities.

7.2. 8- bit ALU

Arithmetic Logic Unit (ALU) is one of the most important digital logic components in CPUs. It normally executes arithmetic operations such as addition, subtraction, multiplication, division, etc. and logic operations such as and, or, xor, xnor, nand, nor, not, buffer, rotate and shift operations.

Hints

Consider the port specification as
Input A, B // 8 bit wide
Input sel // 4 bit wide to support 16 operations
Input dataout // 8 bit wide

// The logic and arithmetic operations being implemented in the ALU are as follows:

1. Arithmetic Addition:	ALU_Out = A + B;
2. Arithmetic Subtraction	ALU_Out = A - B;
3. Arithmetic Multiplication	ALU_Out = A * B;
4. Arithmetic Division	ALU_Out = A / B;
5. Logical Shift Left	ALU_Out = A logical shifted left by 1;
6. Logical Shift Right	ALU_Out = A logical shifted right by 1;
7. Rotate Left	ALU_Out = A rotated left by 1;
8. Rotate Right	ALU_Out = A rotated right by 1;
9. Logical AND	ALU_Out = A AND B;
10. Logical OR	ALU_Out = A OR B;
11. Logical XOR	ALU_Out = A XOR B;
12. Logical NOR	ALU_Out = A NOR B;
13. Logical NAND	ALU_Out = A NAND B;
14. Logical XNOR	ALU_Out = A XNOR B;
15. Greater comparison	ALU_Out = 1 if A > B else 0;

16. Equal comparison
ALU_Out = 1 A = B else 0;
The second stage of multiplexers performs a rotate-right by two bits whenS_1 control signal is selected. Here the corresponding multiplexer inputs are connected to their second next-lower input.

Finally, the third stage of multiplexers performs a rotate-right by four bits, when S_0 control signal isselected. The design uses a case statement to exhaustively list all combinations of the amt signal and thecorresponding rotated results.

Try:

1. Modify the ALU by changing the number of select lines to 4 bit wide to support 16 different functionalities

2. Modify the ALU by changing the number of data lines to 16 bit wide to support 16 different functionalities

8. Exercises on Latches and Flip-flops

To be proficient in programming, you need implement the following sequential logic circuits

1 Implementation of SR latch, JK latch, D latch and T latch
2 Implementation of JK flip-flop, D flip-flop and T flip-flop
3 Realization of D flip-flop using D latch
4 Realization of D flip-flop using JK flip-flop
5 Realization of T flip-flop using JK flip-flop
6 Realization of T flip-flop using D flip-flop

8.1 SR latch, JK latch, D latch and T latch

Construct an SR latch using NOR gates. Verify its operation and demonstrate the circuit.
Write an entity declaration for a positive level-triggered SR-latch with asynchronous active-low preset and clear inputs, and Q and outputs. Include concurrent assertion statements and passive processes as necessary in the entity declaration to verify that
• The preset and clear inputs are not activated simultaneously,
• The setup time of 6 ns from the J and K inputs to the rising clock edge is observed,
• The hold time of 2 ns for the J and K inputs after the rising clock edge is observed and
• The minimum pulse width of 5 ns on each of the clock, preset and clear inputs is observed.

Write a gate level architecture body for the SR latch and a test bench that exercises the statements in the entity declaration.

Hints

```
// Declare port signal

Input rst_l, clk;
Input s, r;

Output q, qb;

// Component declaration of NAND gates
Component NAND_gate (input a, b; output y);

// component instance in the architecture body of VHDL program
NAND_gate port map(s, qb, q);
NAND_gate port map(r, q, qb);

// Test bench for SR latch
Design a test bench to provide the stimulus for the inputs s, r
Generate a clk signal with 5MHz frequency
Generate the reset logic to reset the latch at initial
```

Try

1. Construct SR latch using NAND gates. Verify its operation and demonstrate the circuit
2. Construct JK latch using NAND gates. Verify its operation and demonstrate the circuit
3. Construct D latch using NAND gates. Verify its operation and demonstrate the circuit
4. Construct T latch using NAND gates. Verify its operation and demonstrate the circuit

8.2 JK flip-flop, D flip-flop and T flip-flop

Construct flip-flops using latches and verify its operation and demonstrate the circuit.

Write an entity declaration for a positive edge-triggered JK-flipflop with asynchronous active-low preset and clear inputs, and Q and outputs. Include concurrent assertion statements and passive processes as necessary in the entity declaration to verify that
• The preset and clear inputs are not activated simultaneously,
• The setup time of 6 ns from the J and K inputs to the rising clock edge is observed,
• The hold time of 2 ns for the J and K inputs after the rising clock edge is observed and
• The minimum pulse width of 5 ns on each of the clock, preset and clear inputs is observed.

Write a structural architecture body for the flipflop and a test bench that exercises the statements in the entity declaration.

Hints

The pseudo code for SR latch

```
// Declare port signal

Input rst_l, clk;
Input s, r;

Output q, qb;

// Component declaration of NAND gates
Component NAND_gate (input a, b; output y);

// component instance in the architecture body of VHDL program
NAND_gate port map(s, qb, q);
NAND_gate port map(r, q, qb);

// Test bench for SR latch
Design a test bench to provide the stimulus for the inputs s, r
Generate a clk signal with 5MHz frequency
Generate the reset logic to reset the latch at initial
```

Try

Design 2-bit register

Write component instantiation statements to model the structure shown by the schematic diagram in Figure. Assume that the entity ttl_74x74 and the corresponding architecture basic have been analyzed into the library work. Figure 2 shows the 2-bit register.

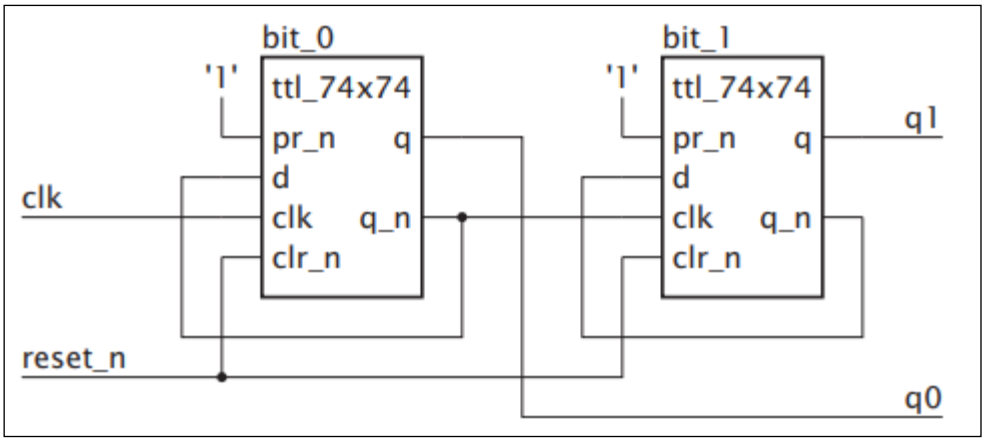

Figure 2: 2-bit register.

9. Exercises on counters and shift registers

To be proficient in programming, you need implement the following sequential logic circuits

1 4-bit synchronous counter with synchronous reset
2 Decade counter
3 4-bit serial in serial out shift register (SISO)

9.1: 4-bit synchronous counter with synchronous reset

Build an entity for a 4-bit counter with synchronous reset input. Include a process in the entity declaration that measures the duration of each reset pulse and reports the duration at the end of each pulse.

Hints

```
/**Declare the port signals */
entity counter_synrst port (
        clk, rst: in std_logic;
         q: out std_logic_vector(3 downto 0));
end counter_synrst;

/**architecturebody  */
architecture arch_counter_synrst of counter_synrst is

Begin
Process (clk, rst)
    Begin

       If clk'event and clk = '1' then
          If rst then
                q = "0000";
          else
                q = q + 1;
       end if;
    end process

End arch_counter_synrst;
//Write the test bench for providing the stumulus

entity tb_counter_synrst port
```

```
end tb_counter_synrst;

architecture arch_tb_counter_synrst of tb_counter_synrst is

   signal clk, rst: std_logic := '0';
   signal q: std_logic_vector(3 downto 0);

   component counter_synrst port (
        clk, rst: in std_logic;
         q: out std_logic_vector(3 downto 0));
   end component;

begin

   DUT: counter_synrst port map (gray_code, binary_code);

   Process
   begin
        clk = ~clk;
        Wait for 10 ns;
end process;

   Process
   begin
        rst = '0';
        Wait for 10 ns;
        rst = '1';
       wait;
   end process;

end architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design
```

Try

1. Design 4-bit synchronous counter with asynchronous reset
2. Design 4-bit asynchronous counter with synchronous reset
3. Design 4-bit asynchronous counter with asynchronous reset

9.2 Decade counter with asynchronous reset

Construct an entity for a decade counter with asynchronous reset input. Include a process in the entity declaration that measures the duration of each reset pulse and reports the duration at the end of each pulse.

Hints

```
/**Declare the port signals */
entity dec_counter_asynrst port (
        clk, rst: in std_logic;
         q: out std_logic_vector(3 downto 0));
end dec_counter_asynrst;

/**architecturebody  */
architecture arch_dec_counter_asynrst of dec_counter_asynrst is

Begin
    Process (clk, rst)
    Begin

       If rst then
                 q = “0000”;
       elif clk’event and clk = ‘1’ then
          if (q = “1010”) then
                 q = “0000”;
          else
                  q = q + 1;
          end if;

       end if;
    end process

End arch_dec_counter_asynrst;

//Write the test bench for providing the stumulus

entity tb_dec_counter_asynrst port
end tb_dec_counter_asynrst;

architecture arch_tb_dec_counter_asynrst of tb_dec_counter_asynrst is

   signal clk, rst: std_logic := ‘0’;
   signal q: std_logic_vector(3 downto 0);

   component dec_counter_asynrst port (
        clk, rst: in std_logic;
         q: out std_logic_vector(3 downto 0));
   end component;

begin

   DUT: dec_counter_asynrst port map (clk, rst, q);

   Process
   begin
        clk = ~clk;
        Wait for 10 ns;
   end process;

   Process
   begin
        rst = ‘0’;
        Wait for 10 ns;
        rst = ‘1’;
       wait;
```

```
   end process;

end architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design
Elaborate the design and create bit file
Dump the bit file in zybo fpga
```

Try

1. Design decade synchronous counter with synchronous reset
2. Design counter to count the events from 3 to 12

9.3 4-bit serial in serial out shift register (SISO)

In digital systems it is often necessary to have circuits that can shift the bits of a vector by one or more bit positions to the left or right. Design a circuit that can shift a four-bit vector W = w3w2w1w0 one bit position to the right when a control signal Shift is equal to 1. Let the outputs of the circuit be a four-bit vector Y = y3y2y1y0 and a signal k, such that if Shift = 1 then y3 = 0, y2 = w3, y1 = w2, y0 = w1, and k = w0. If Shift = 0 then Y = W and k = 0.
Build an entity for a shift register to drive the resister serially and output the data serially. Write a test bench architecture to simulate and verify the design.

Hints

```
/**Declare the port signals */
entity siso port (
        clk, rst: in std_logic;
        sin : in std_logic;
        q: out std_logic_vector(3 downto 0));
end siso;

/**architecturebody  */
architecture arch_siso of siso is

Begin
    Process (clk, rst)
    Begin

       If rst then
                 q = “0000”;
       elif clk’event and clk = ‘1’ then
          q[3] = sin;
          q[2] = q[3];
          q[1] = q[2];
          q[0] = q[1];

       end if;
    end process
```

```
End arch_siso;

//Write the test bench for providing the stumulus

entity tb_siso port
end tb_siso;

architecture arch_tb_siso of tb_siso is

   signal clk, rst: std_logic := ‘0’;
   signal sin: std_logic := ‘0’;
   signal q: std_logic_vector(3 downto 0);

   component siso port (
        clk, rst: in std_logic;
         sin : in std_logic;
         q: out std_logic_vector(3 downto 0));
   end component;

begin

   DUT: siso port map (clk, rst, sin, q);

   Process
   begin
        clk = ~clk;
        Wait for 10 ns;
   end process;

   Process
   begin
        rst = ‘0’;
        Wait for 10 ns;
        rst = ‘1’;
       wait;
   end process;

   Process
   begin
        sin = ~sin;
        Wait for 25 ns;
   end process;
end architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design
Elaborate the design and create bit file
Dump the bit file in zybo FPGA
```

Try

1 Design 4-bit serial in parallel out shift register (SIPO)
2 Design 4-bit parallel in serial out shift register (PISO)
3 Design 4-bit parallel in parallel out shift register (PIPO)

10.Exercises on case study: Pseudo random generator

To be proficient in programming, you need implement the following finite state machines

1 Pseudo random number generator using LFSR
2 Pseudo random number generator for CRC logic

10.1 Pseudo random number generator using LFSR

Build Pseudo random number generator using LFSR

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops.

Linear feedback shift registers make extremely good pseudorandom pattern generators. When the outputs of the flip-flops are loaded with a seed value (anything except all 0s, which would cause the LFSR to produce all 0 patterns) and when the LFSR is clocked, it will generate a pseudorandom pattern of 1s and 0s. Note that the only signal necessary to generate the test patterns is the clock.

Hints

```
Step 1:
The linear feedback shift register is implemented as a series of Flip-Flops inside
of an FPGA that arewired together as a shift register.
Several taps off of the shift register chain are used as inputs to eitheran XOR or
XNOR gate.

The output of this gate is then used as feedback to the beginning of the
shiftregister chain, hence the Feedback in LFSR.


Step 2:
When an LFSR is running, the pattern that is being generated by the individual Flip-
Flops is pseudo-random, meaning that it’s close to random. It’s not completely
random because from any state of theLFSR pattern and can predict the next state.

Step 3:
Longer LFSRs will take longer to run through all iterations. The longest possible
number of iterations foran LFSR of N-bits is 2N-1.

Step 4:
That pattern is all 0’s when using XOR gates, or all 1’s when using XNOR gates as
your feedback gate.
```

Try:

1. Pseudo random number generator for 8-bit CRC logic
2. Pseudo random number generator for 12-bit CRC logic
3. Pseudo random number generator for 16-bit CRC logic

11. Exercises onCARRY-LOOK AHEAD ADDER

11.1 Carry look ahead adder

Build 4- bit carry look ahead adder (CLA) and justify the speed of operation CLA is more than ripple carry adder

Develop a functional model of a 3-bit carry-look-ahead adder. The adder has two 3-bit data inputs, a(2 downto 0) and b(3 downto 0); a 3-bit data output, s(2 downto 0); a carry input, c_in; a carry output, c_out; a carry generate output, g; and a carry propagate output, p. The adder is described by the logic equations and associated propagation delays: where the Gi are the intermediate carry generate signals, the Pi are the intermediate carry propagate signals and the Ci are the intermediate carry signals. C–1 is c_in and C3 is cout. Model should use the expanded equation to calculate the intermediate carries, which are then used to calculate the sums.

$$s_i = a_i \oplus b_i \oplus c_{i-1}$$

$$g_i = a_i \,.\, b_i$$

$$p_i = a_i + b_i$$

$$c_i = g_i + p_i\, c_{i-1}$$

Hints

```
/**Declare the port signals */
entity cla port (
        a, b: in std_logic-vector(2 downto 0);
        sum: out std_logic_vector(2 downto 0);
       cout: out std_logic);
end cla;

/**architecturebody  */
architecture arch_cla of cla is

Begin
g0 = a[0] & b[0];
    p0 = a[0] | b[0];
    c1 = g0 + p0 & c0;
     . . . . . .
     . . . . . .
     . . . . . .

End arch_cla;

//Write the test bench for providing the stumulus

entity tb_cla port
end tb_cla;

architecture arch_tb_cla of tb_cla is

   signal a, b: std_logic_vector(2 downto 0) := “000”;
   signal cin: std_logic := ‘0’;
   signal sum: std_logic_vector(s downto 0);
```

```
   component cla port (
        a, b: in std_logic-vector(2 downto 0);
         sum: out std_logic_vector(2 downto 0);
         cout: out std_logic);
   end component;

begin

   DUT: cla port map (clk, rst, sin, q);

   Process
   begin
        a = a + "0110"
        wait for 10 ns;
        b = b + "1010"
   end process;

end architecture

// After post simulation

Simulate the design using Xilinx software

Plot the wave forms and verify the functionality of the design

Synthesize the design
Elaborate the design and create bit file
Dump the bit file in zybo FPGA
```

Try:

1. Design and implement 4-bit carry look ahead adder
2. Design and implement 4-bit ripple carry adder

12. Exercises onVENDING MACHINE CONTROLLER

Vending-Machine Controller sells candy bars for 25 cents. The inputs are nickel_in, dime_in, and quarter_in, indicating the type of coin that was deposited, plus clock (clk) and reset (rst), to which the circuit responds with the outputs candy_out, to dispense a candy bar, plus nickel_out or dime_out, asserted when change is due. Design this circuit using the FSM approach. Also, estimate the number of flip-flops that will be required. Figure 3. Shows the block level diagram representation of vending machine controller and Figure 4 shows the state diagram of the vending machine.

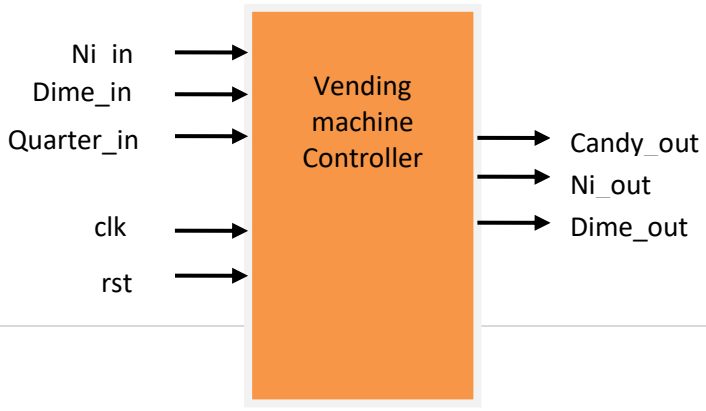

Figure 3: The vending machine controller block diagram

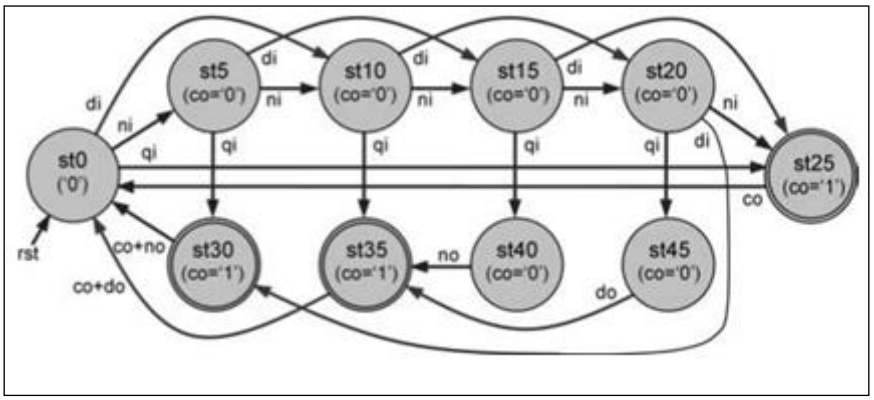

Figure 4: State diagram of the vending machine controller

```
/**VHDL model for gray counter */

entity vend_mach is
port(   Clk, rst : in std_logic;
        Ni_in, Dime_in, Quarter_in : in std_logic;
Candy_out, Ni_out, Dime_out : out std_logic
    );
end vend_mach;

architecture Behavioral of vend_mach is

--type of state machine and signal declaration.
type state_type is (st0, st5, st10, st15, st20, st25, st30, st35, st40, st45);
signal next_state : state_type;
begin

process(Clk, rst)
begin
    if(rising_edge(Clk)) then
        case next_s is
            when st0 =>
                if(Ni_in) then
                    next_state<= st5;
                elsif(Dime_in) then
                    next_state<= st10;
                elsif(Quarter_in) then
                    next_state<= st25;
                end if;
            when st5 =>
 . . .
                 . . .
                 . . .
        end case;
    end if;
end process;

end Behavioral;
```

Try

1. Implement the vending machine using Melay finite state machine

13. Exercises on Gray-Encoded Counter

Design a 0-to-8 counter with Gray-encoded outputs.

a. Draw the state transition diagram.
b. Estimate the number of flip-flops that will be needed.
c. Write the VHDL code, then compile and simulate it.
d. Check whether the number of DFFs inferred by the compiler matches your prediction.

```
/**VHDL model for gray counter */
entity graycounter is
  generic (n: integer := 6);
  port (clk, rst, en: in std_logic;
        output: out std_logic_vector (n-1 downto 0));
end graycounter;

architecture graycounter_beh of graycounter is
  signal currstate, nextstate, hold, next_hold: std_logic_vector (n-1 downto 0);
begin

  statereg: process (clk)
  begin
    if (clk = '1' and clk'event) then
      if (rst = '1') then
        currstate <= (others =>'0');
      elsif (en = '1') then
        currstate <= nextstate;
      end if;
    end if;
  end process;

  hold <= currstate xor ('0' & hold(n-1 downto 1));
  next_hold <= std_logic_vector(unsigned(hold) + 1);
  nextstate <= next_hold xor ('0' & next_hold(n-1 downto 1));
  output <= currstate;

end graycounter_beh;

/**VHDL test bench  */
entity testbench is
end testbench;

architecture arch of testbench is
  component graycounter is
    generic (n: integer := 6);
    port (clk, rst, en: in std_logic;
          output: out std_logic_vector (n-1 downto 0));
  end component;

  signal clk_s, rst_s, en_s: std_logic;
  signal output_s: std_logic_vector(5 downto 0);

begin
  comptotest: graycounter generic map (6) port map (clk_s, rst_s, en_s, output_s);
```

```
  clk_proc: process
  begin
    clk_s <= '1';
    wait for 10 ns;
    clk_s <= '0';
    wait for 10 ns;
  end process clk_proc;

  vector_proc: process
  begin
    rst_s <= '1';
    wait until clk_s='1' and clk_s'event;
    wait for 5 ns;
    rst_s <= '0';
    en_s <= '1';
    for index in 0 to 3 loop
      wait until clk_s='1' and clk_s'event;
    end loop;
    wait for 5 ns;
    wait;
  end process vector_proc;

endarch;
```

Try

1. Design a counter with Johnson-encoded output instead of Gray-encoded.
2. Design a counter with one-hot output instead of Gray output.
3. Modify the counter designed, such that the circuit stays in each state during T ¼ 1 s, with the output displayed on a seven segment display. Assume that the clock frequency is 50 MHz.

14. Exercises on RAM design

Write an entity declaration for a lookup table RAM modeled at an abstract level. The RAM has an address input of type look_up_index, which is an integer range from 0 to 31, and a data output of type real. Include declarations within the declarative part of the entity to define the RAM contents, initialized to numbers of your choice.

```
/**Declare the port signals */
entity single_port_RAM is
  generic (
    addr_width : integer := 2;
    data_width : integer := 3
  );

  port(
    clk: in std_logic;
    we : in std_logic;
    addr : in std_logic_vector(addr_width-1 downto 0);
    din : in std_logic_vector(data_width-1 downto 0);
    dout : out std_logic_vector(data_width-1 downto 0)
    );
end single_port_RAM;
```

```
architecture arch of single_port_RAM is
 type ram_type is array (2**addr_width-1 downto 0) of std_logic_vector (data_width-
1 downto 0);
 signal ram_single_port : ram_type;

begin
  process(clk)
  begin
    if (clk'event and clk='1') then
      if (we='1') then -- write data to address 'addr'
        --convert 'addr' type to integer from std_logic_vector
        ram_single_port(to_integer(unsigned(addr))) <= din;
      end if;
  end if;
  end process;

  -- read data from address 'addr'
  -- convert 'addr' type to integer from std_logic_vector
  dout<=ram_single_port(to_integer(unsigned(addr)));
end arch;
```

Try

1. Extend the functionality of RAM memory block by allowing write and read operations to construct RAM block of size 16 x 8 RAM.

15. Final Notes

The only way to learn programming is program, program and program on challenging problems. The problems in this tutorial are certainly NOT challenging. There are tens of thousands of challenging problems available – used in training for various programming contests (such as International Collegiate Programming Contest (ICPC), International Olympiad in Informatics (IOI)). Check out these sites:

- Cadence certifications (https://www.cadence.com/en_US/home/training/become-cadence-certified.html#dds0
- National Institute of Electronics and Information Technology(https://reg.nielitchennai.edu.in)

Student can have any one of the following certifications:

- NPTEL – Digital design
- NPTEL – HDL programming

V. TEXT BOOKS:

1 Wen-Long Chin, “Principles of Verilog Digital Design”, CRC Press, 1st edition, 2022
2 Charles Roth, “Digital System Design using VHDL”, Tata McGraw Hill, 2nd edition, 2012.
3 M. Morris Mano and Michael D. Ciletti, “Digital Design”, Pearson Education, 6th edition, 2018.
4 John F Wakerly, “Digital Design Principles and practices”, Pearson Education, 4th edition, 2008

VI. REFERENCE BOOKS:

1 Mohammad Karim, Xinghao Chen, “Digital Design: Basic Concepts and Principles”, CRC Press, 2nd edition, 2007.
2 Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education, 2nd edition, 2003.

V. ELECTRONICS RESOURCES:

1 https://www.dsdwebworks.com/resources.php
2 https://github.com/kevinwlu/dsd

VI. MATERIALS ONLINE

1 Course template
2 Lab Manual