# INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

## COURSE CONTENT

| DIGITAL DESIGN THROUGH VHDL | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **VI Semester: ECE** | | | | | | | | |
| **Course Code** | **Category** | **Hours / Week** | | | **Credits** | **Maximum Marks** | | |
| | | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| **AECD34** | **Elective** | 3 | - | - | 3 | 40 | 60 | 100 |
| **Contact Classes: 48** | **Tutorial Classes: Nil** | **Practical Classes: Nil** | | | | **Total Classes: 48** | | |
| **Prerequisites: Digital System Design** | | | | | | | | |

### I. COURSE OVERVIEW:
This course introduces the hardware description language for design and development of digital integrated circuits and field programmable devices. Provides hardware description language elements, synthesizable register transfer logic models in gate level, dataflow, behavioral, switch level modeling of combinational and sequential circuits. Allows to use computer aided design tools at the levels of system design, logic design and IC design.

### II. COURSE OBJECTIVE:
**The students will try to learn:**

I. *T*he fundamentals of hardware description using Verilog, module concepts, and core language elements including dataflow constructs.
II. *The* gate-level design, propagation delays, and modeling of combinational building blocks such as encoders, decoders, (de)multiplexers, and comparators using user-defined primitives.
III. *The* behavioral modeling methods including procedural assignments, timing control, conditional/case logic, and iterative loop structures for digital circuit implementation.
IV. *The* transistor/switch-level abstractions and the design flow of ASIC and FPGA-based systems using industry synthesis environments like Xilinx Vivado.

### III. COURSE OUTCOMES:
**At the end of the course students should be able to:**

CO1 Describe and implement modules using dataflow and behavioral constructs and apply appropriate operators, parameters, and delays in digital design descriptions.
CO2 Design gate-level models including combinational and sequential user-defined primitives (UDP).
CO3 Construct and analyze combinational logic modules such as encoders, decoders, multiplexers, demultiplexers and magnitude comparators.
CO4 Apply looping, conditional, case, and block statements to model real-time digital behavior with accurate timing control.
CO5 Model and simulate transistor-based switches, CMOS pass-gate structures, and bidirectional signal behavior including drive strength and contention cases.
CO6 Summarize FPGA/ASIC design flow and perform logic synthesis using tools such as Intel Quartus Prime and industry workflows from Cadence.

## III. COURSE CONTENT:

**MODULE - I: INTRODUCTION TO VERILOG HDL (10)**
Introduction to Verilog, Popularity of Verilog HDL, Module Concept, Module Modeling Styles, Language Elements: Comments, Identifiers, Keywords, Value Set, Data Types, Memory Element, Constant, Parameter, Operators. Dataflow Modeling: Continuous Assignment, Implicit Continuous Assignment, Delays, Design examples using data flow modeling.

**MODULE - II: GATE-LEVEL MODELING (09)**
Multiple-Input Gates, Gate Delays, Design Examples, User-Defined Primitives: UDP Basics Combinational User-Defined Primitives, Sequential User-Defined Primitives, Combinational Logic Modules: Decoders, Encoders, Multiplexers, Demultiplexers, Magnitude Comparators.

**MODULE - III: BEHAVIORAL MODELING (10)**
Procedural Constructs, Procedural Assignments, Timing Control, Conditional Statements, Case Statement Design examples using behavioral modeling.

Loop Statements: For Loop, While Loop, Repeat Loop, Forever Loop, Block Statements Procedural Continuous Assignment, Design examples using behavioral modeling.

**MODULE - IV: SWITCH LEVEL MODELLING (09)**
Basic Transistor Switches, CMOS Switch, Bi – directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.

**MODULE - V: SEQUENTIAL LOGIC (10)**
Analysis of Synchronous Sequential Machines, Synthesis of Synchronous Sequential Machines, Analysis of Asynchronous Sequential Machines, Synthesis of Asynchronous Sequential Machines, and Synthesis: Design flow of ASICs and FPGA- Based Systems, Design Environment and Constraints, Logic Synthesis.

## IV. TEXT BOOKS:


1. Joseph Cavanagh, “Verilog HDL: Digital Design and Modeling”, CRC Press, 1st Edition, 2007.
2. Michael D. Ciletti, “Advanced Digital Design with Verilog HDL”, PHI, 2005.
3. Joseph Cavanagh, “Digital Design and Verilog HDL Fundamentals”, CRC Press, 1st Edition, 2008.


## V. REFERENCE BOOKS:


1. Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic design with Verilog Design”, TMH, 2nd Edition, 2010.
2. Sunggu Lee “Advanced Digital Logic Design using Verilog, State Machine & Synthesis for FPGA”, Cengage Learning, 2012.
3. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2009.
4. T. R. Padmanabhan and B. Bala Tripura Sundari, “Design through Verilog HDL”, Wiley, 2009.
5. Zainalabdien Navabi, “Verilog Digital System Design”, TMH, 2nd Edition, 2009.


## VI. WEB REFERENCES:

1. https://www.crcpress.com/Verilog-HDL-Digital-Design an Modeling/ Cavanag h/p/book/ 9781420051544
2. https://www.uotechnology.edu.iq
3. https://www.iare.ac.in

## VII. MATERIALS ONLINE

1. Course template
2. Tutorial question bank
3. Definition and terminology
4. Tech-talk topics
5. Assignments
6. Model question paper - I
7. Model question paper - II
8. Lecture notes
9. Early learning readiness videos (ELRV)
10. Power point presentations