INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES								
VI Semester: ECE								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
AECD40	**Elective**	3	-	-	3	40	60	100
Contact Classes: 48	**Tutorial Classes: Nil**	**Practical Classes: Nil**				**Total Classes: 48**		
Prerequisite: Digital Signal Processing								

I. COURSE OVERVIEW:

This course enables the architecture, memory management of single instruction and multiple data, very large instruction word and TMS processors for the implementation of discrete Fourier transform and fast Fourier transform algorithms. It focuses on memory organization, external bus interfacing signals, parallel input/output interface, interrupts, direct memory access, finite impulse response, infinite impulse response filters. In built peripherals of TMS processor used in applications of communication equipment, image processing, control systems and consumer electronic devices.

II. COURSES OBJECTIVES:

The students will try to learn

I. The architectures of digital signal processors and design aspects of digital signal processing algorithms.
II. The memory and external input/output peripheral interface with programmable DSP processor.
III. The realization of digital filters and fast Fourier transform algorithms of the signal spectrum on host DSP processor.
IV. The programming skills using code composer studio environment for TMS320C54XX processor.

III. COURSE OUTCOMES:

At the end of the course students should be able to:

CO 1 Understand the role of DSP in real-time signal processing applications.

CO 2 Analyze the performance of DSP algorithms on the architecture.

CO 3 Explain on-chip peripherals and interfaces, such as ADCs and DACs, in TMS320C54xx processors.

CO 4 Describe various addressing modes used in interfacing memory with programmable DSPs.

CO 5 Explain basic DSP algorithms, such as filtering, convolution, and correlation.

CO 6 Discuss the architecture and features that facilitate DSP algorithm implementation.

IV. COURSE CONTENT:

MODULE - I: INTRODUCTION TO DIGITAL SIGNAL PROCESSOR (10)

Digital signal-processing and processors, Sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and fast Fourier transform (FFT), differences between DSP and other microprocessor architectures; Computational accuracy in DSP implementation-Number formats: Fixed point, floating point and block floating point formats, IEEE-754 floating point, dynamic range and precision, relation between data word size and instruction word size; Sources of error in DSP implementations: A/D conversion errors, DSP computational errors, D/A conversion errors.

MODULE –II: ARCHITECTURE OF PROGRAMMABLE DSP DEVICES (09)

DSP Computational building blocks-Multiplier and multiplier accumulator, modified bus structures and memory access in PDSPs, multiple access memory, multiport memory, SIMD, VLIW architectures, pipelining, special addressing modes in PDSPs, on-chip peripherals.

MODULE –III: OVERVIEW OF TMS320C54XX PROCESSOR (09)

Architecture of TMS320C54XX DSPs, addressing modes, memory space of TMS320C54XX processors.

Program control, instruction set and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation.

MODULE –IV: INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs (10)

Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA). A Multi-channel buffered serial port (McBSP) and CODEC - DSP Interface.

MODULE –V: IMPLEMENTATIONS OF BASIC DSP ALGORITHMS (10)

The Q-notation, convolution, correlation, FIR filters, IIR filters, interpolation filters, decimation filters, an FFT algorithm for DFT filters computation of the signal spectrum. PID controller, Adaptive filters and 2-d signal processing.

V. TEXT BOOKS:

1. Avatar Singh and S. Srinivasan, “Digital Signal Processing”, Thomson Publications, 1st Edition, 2004.
2. Lapsley et al., “DSP Processor Fundamentals Architectures & Features”, S. Chand & Co, 1st Edition, 2000.
3. B. Ventakaramani, M. Bhaskar, “Digital Signal Processors Architecture Programming and Applications”, Tata McGraw-Hill, 1st Edition, 2006.

VI. REFERENCE BOOKS:

1. Jonatham Stein, “Digital Signal Processing”, John Wiley, 1st Edition, 2000.
2. Sen M. Kuo&WoonSergGan, “Digital Signal Processors Architectures, Implementation and Application”, Pearson Practice Hall, 1st Edition, 2013.
3. K Padmanabhan, R.Vijayarajeswaran, Ananthi. S, “A Practical Approach to Digital Signal Processing”, New Age International, 1st Edition, 2006.
4. Ifeachor E. C., Jervis B. W, “Digital Signal Processing: A practical approach”, Pearson Education, PHI/, 2nd Edition, 2002.
5. Peter Pirsch, “Architectures for Digital Signal Processing”, John Weily, 1st Edition, 2007.

VII. ELECTRONICS RESOURCES:

1. https://books.google.co.in/books/about/DigitalSignalProcessors.html?id=2A2-v3raKEC
2. https://www.analog.com/en/design-center/landing-pages/001/beginners-guide-to-dsp.html
3. https://nptel.ac.in/noc/courses/noc19/SEM2/noc19-ee70/
4. https://onlinecourses.nptel.ac.in/noc21_ee20/preview
5. NPTEL :: Electrical Engineering - NOC: Digital Signal Processing and its Applications

6. NPTEL :: Electrical Engineering - NOC: Mapping Signal Processing Algorithms to Architectures

VIII. MATERIALS ONLINE

1. Course template
2. Tutorial question bank
3. Definition and terminology
4. Tech-talk topics
5. Assignments
6. Model question paper - I
7. Model question paper - II
8. Lecture notes
9. Early learning readiness videos (ELRV)
10. Power point presentations