INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

VLSI DESIGN LABORATORY								
VI Semester: ECE								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
AECD44	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		-	-	2	1	40	60	100
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 36**				**Total Classes: 36**		
Prerequisite: Linear IC Applications								

I. COURSE OVERVIEW:
This course provides the hands-on experience on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design. VLSI designs are widely used in automobiles, mobiles and embedded processors.

II. COURSES OBJECTIVES:
The students will try to learn

I. Modern tools for functional level to physical layout with verification at intermediate stages in the VLSI design flow in top-down approach.
II. Design and simulations of analog, digital and mixed circuits for optimum values of area over head, power and time delay.
III. The chip design through a practical approach using advanced modern tools such as vivado and cadence for front end and back end.

III. COURSE OUTCOMES:
At the end of the course students should be able to:

CO 1 Make use of the static, dynamic and noise margin parameters of CMOS circuits for calculating figure of merit
CO 2 Analyze complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays.
CO 3 Utilize existing small building block and circuit symbols with necessary inter connections to realize complex design.
CO 4 Examine the conditions for optimum performance of lathes and registers with the knowledge of digital system design.
CO 5 Identify bandwidth, gain, and common mode rejection ratio parameters for cascode amplifiers to protect amplifier from miller effect.
CO 6 Apply the design rule check and Layout versus schematic check on layout of MOS circuits to verify spacing rules between layers.

EXERCISES FOR VLSI DESIGN LABORATORY

S.NO	Topic Name	Page No
1	**Exercises on NMOSFET** a. NMOSFET schematic using 180nm,90nm technology b. Create symbol c. Perform simulation in transient analysis, dc analysis d. Parametric analysis e. Layout design DRC,LVS,RCX extraction	4
2	**Exercises on CMOS INVERTER** To be proficient in cadence virtuoso, students be able to design a. CMOS Inverter schematic using 180nm,90nm technology b. Create symbol c. Perform simulation in transient analysis, dc analysis d. Parametric analysis e. Layout design DRC,LVS,RCX extraction	5
3	**Exercises on RING OSCILLATOR** To be proficient in cadence virtuoso, students be able to design a. Ring oscillator using 180nm using 3 stages of inverter,5 stages of inverter b.Create symbol c. Perform simulation find Frequency of oscillations d.Delay and power dissipation	6
4	**Exercises on LOGIC GATES** To be proficient in cadence virtuoso, students be able to design a. 2 input NAND gate using 180nm b. Perform simulation find dynamic characteristics c. Propagation delay, rise time, fall time and power consumption d. similarly perform design of 2-input NOR gate	7
5	**Exercises on MULTIPLEXER** To be proficient in cadence virtuoso, students be able to design a. 2×1 multiplexer gate using 180nm b. Perform simulation veriy the function c. 4×1 multiplexer gate using 180nm	8
6	**Exercises on LATCHES** To be proficient in cadence virtuoso, students be able to design a. positive level-sensitive latch using 180nm b. verify logical operation c. Analyze its behavior using static and DC analysis d. negative level-sensitive latch using 180nm	9
7	**Exercises on REGISTERS** To be proficient in cadence virtuoso, students be able to design a. 4 bit SISO shift registers using 180nm b. Perform transient analysis c. calculate Power dissipation, delay d. 4 bit PIPO shift registers using 180nm	10
8	**Exercises on DIFFERENTIAL AMPLIFIER** To be proficient in cadence virtuoso, students be able to design a. Differential amplifier schematic using 180nm technology b. Create symbol c. Simulate differential amplifier d. Measure the output voltage, gain, CMRR	12
9	**Exercises on LAYOUT OF CMOS INVERTER**	13

To be proficient in cadence virtuoso, students be able to design

a. Design the layout of CMOS inverter
b. DRC,LVS checking
c. RCX extraction and find parasitic values
d. Pre-layout and post layout simulation

10 **Exercises on LAYOUT OF NAND/NOR GATES** 14

To be proficient in cadence virtuoso, students be able to design

a. Design the layout of NAND and NOR logic gates
b. DRC,LVS checking
c. RCX extraction and find parasitic values
d. Pre-layout and post layout simulation

11 **Exercises on COMMON SOURCE AMPLIFIER** 15

To be proficient in cadence virtuoso, students be able to design

a. Design common source amplifier using 180nm technology
b. Plot transfer characteristics, dc characteristics
c. DRC,LVS checking
d. RCX extraction and find parasitic values4.

12 **Exercises on COMMON DRAIN AMPLIFIER** 16

To be proficient in cadence virtuoso, students be able to design

a. Design common source amplifier using 180nm technology
b. Plot transfer characteristics, dc characteristics
c. calculate transconductance, voltage gain, bandwidth
d. Perform parametric analysis

13 **Exercises on CURRENT MIRROR** 17

To be proficient in cadence virtuoso, students be able to design

a. Design current mirror amplifier using 180nm technology
b. Plot transfer characteristics, dc characteristics
c. DRC,LVS checking
d. RCX extraction and find parasitic values

14 **Exercises on CASCODED CURRENT MIRROR** 18

To be proficient in cadence virtuoso, students be able to design

a. Design cascaded current mirror amplifier using 180nm technology
b. Plot transfer characteristics, dc characteristics
c. DRC,LVS checking
d. RCX extraction and find parasitic values

EXERCISES FOR VLSI DESIGN LABORATORY

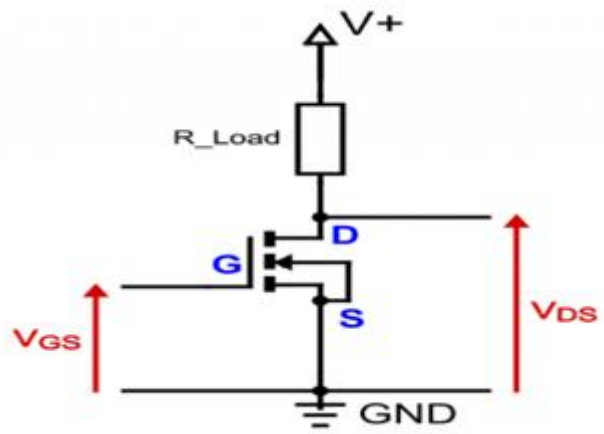
Note: Students are encouraged to do laboratory practice sessions on the Cadence virtuoso licensed software.

This course provides the hands-on experience on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design. VLSI designs are widely used in automobiles, mobiles and embedded processors

1. EXERCISES ON NMOSFET

Implementing a MOSFET in Cadence Virtuoso is significant because it provides a comprehensive and industry-standard platform for accurate design, simulation, and layout of integrated circuits at the transistor level. Cadence Virtuoso enables designers to model the electrical behavior of MOSFETs using precise foundry-provided models, allowing for detailed DC, AC, and transient analyses. This helps in evaluating performance metrics like threshold voltage, switching speed, gain, noise, and power consumption.

1.1 Design, simulate, and analyze the electrical behavior of an NMOSFET using Cadence Virtuoso with 180nm CMOS technology by creating its schematic, generating a symbol, and performing transfer characteristics, DC characteristics, and parametric analysis to evaluate key performance parameters such as threshold voltage, drain current, and switching behavior.



NMOSFET

1.2 Design, simulate, and analyze the electrical behavior of an NMOSFET using Cadence Virtuoso with 90nm CMOS technology by creating its schematic, generating a symbol, and performing transfer characteristics, DC characteristics, and parametric analysis to evaluate key performance parameters such as threshold voltage, drain current, and switching behavior.

.**Try:**

1. To design, simulate, and analyze the electrical behavior of a p-channel depletion-type MOSFET using Cadence Virtuoso with 180nm CMOS technology by creating its schematic, generating a symbol, and performing transfer characteristics and output (DC) characteristics analysis to evaluate key performance parameters such as threshold voltage, drain current, and depletion-mode switching behavior.

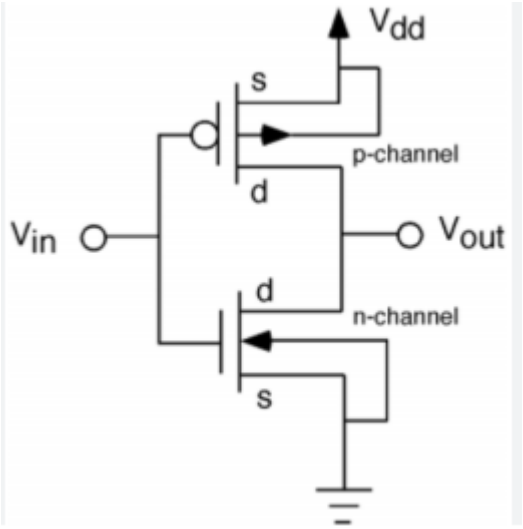
2. To develop a circuit using an enhancement-mode p-type MOSFET biased with a voltage divider,

simulate it using Cadence Virtuoso with 180nm CMOS technology, and analyze the output signal to evaluate the device's switching behavior, threshold voltage, and output response under varying input conditions.

2. EXERCISES ON CMOS INVERTER

Implementing a CMOS inverter in Cadence Virtuoso is significant because it allows for precise and efficient design, simulation, and physical layout of one of the most fundamental building blocks in digital integrated circuits. Cadence Virtuoso provides a platform to accurately model both NMOS and PMOS transistors using foundry-specific models, enabling comprehensive DC, transient, and noise analyses. This helps in evaluating critical performance metrics such as voltage transfer characteristics (VTC), noise margins, propagation delay, rise and fall times, and power dissipation.

2.1 Design, simulate, and analyze the electrical behavior of a CMOS inverter using Cadence Virtuoso with 180nm CMOS technology. The goal is to evaluate the performance of the inverter in terms of key parameters such power dissipation, delay, transfer characteristics, DC characteristics, and parametric analysis



CMOS inverter

2.2 Repeat the above experiment with 90 nm Technology and compare the results in terms of power dissipation, delay.

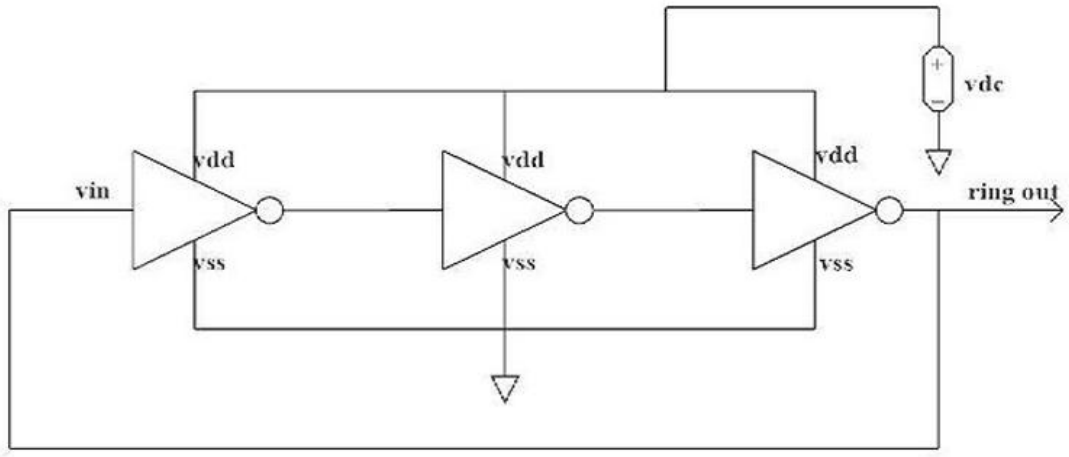
Try:

1. Design and simulate an NMOS inverter with a resistive load using Cadence Virtuoso. Determine its DC output characteristics and voltage transfer characteristics by varying the input voltage, and analyze the impact of the load resistance on inverter behavior.
2. Design and simulate an NMOS inverter with a PMOS active load using Cadence Virtuoso. Analyze the output and voltage transfer characteristics by sweeping the input voltage and observe the behavior of the inverter under static conditions

3. EXERCISES ON RING OSCILLATOR

A ring oscillator, typically composed of an odd number of CMOS inverters connected in a loop, allows designers to measure propagation delay, oscillation frequency, and power consumption, which are essential parameters for assessing the speed and efficiency of a CMOS process. Using Virtuoso's schematic editor and simulation tools like Spectra, designers can perform transient and parametric analyses to study how variations in supply voltage, temperature, or transistor sizing affect oscillator behavior. Additionally, the platform supports layout design and parasitic extraction, allowing post-layout simulations that reflect real-world performance.

3.1 Design and simulate a 3 stage ring oscillator using Cadence Virtuoso with 180nm CMOS technology by creating its schematic, generating a symbol, and determine its frequency of oscillation based on the number of stages and propagation delay.



Ring oscillator

3.2 Design and simulate ring oscillators with different numbers of stages (3-stage,5-stage,7-stage).Analyze the frequency, delay per stage, and power dissipation as the number of stages increases Plot frequency vs. number of stages and delay vs. number of stages

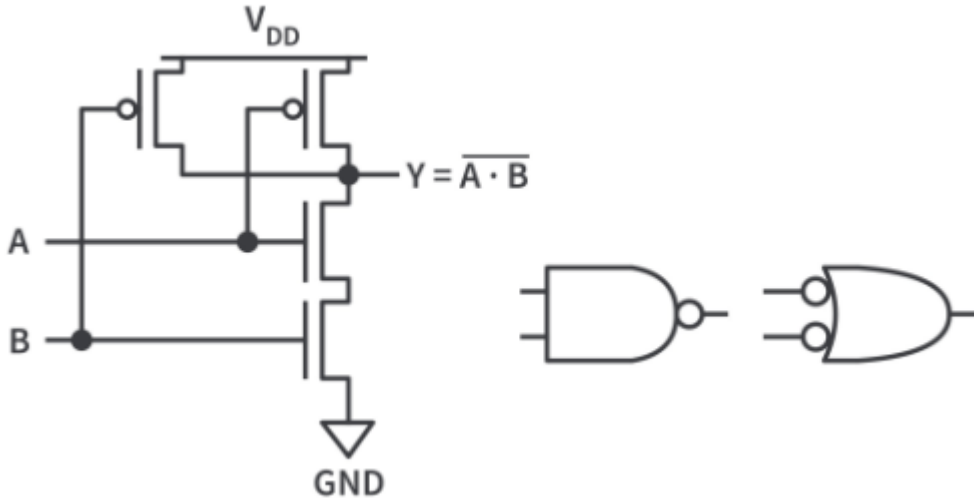
Try:

1. Design and simulate a CMOS ring oscillator using 180nm technology in Cadence Virtuoso. Determine its frequency of oscillation and propagation delay per stage. Further, investigate how varying the load capacitance influences the delay and frequency characteristics.
2. Perform an advanced analysis of the CMOS ring oscillator by evaluating its power dissipation, examining the effect of temperature variation on the frequency of oscillation, and conducting a parametric study by sweeping the supply voltage and varying the number of inverter stage.

4. EXERCISES ON LOGIC GATES

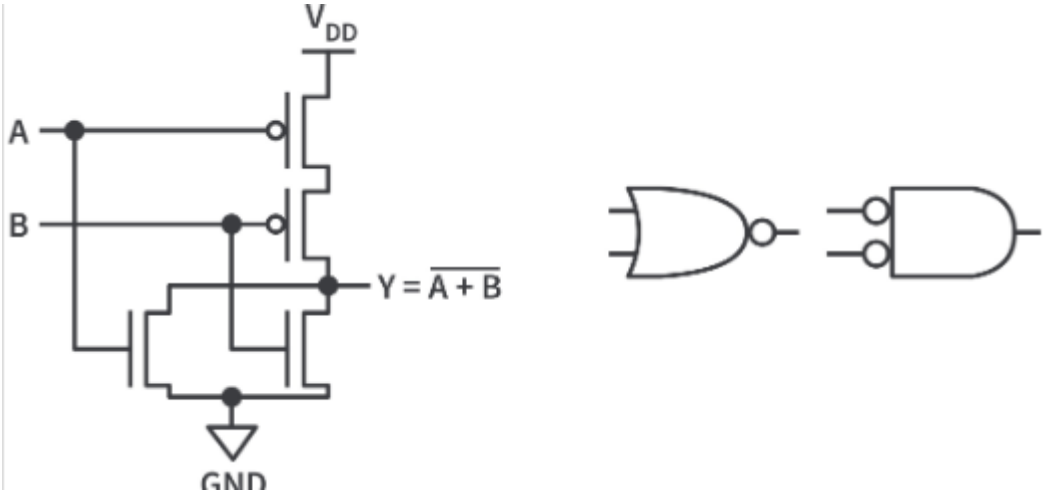
Implementing logic gates in Cadence Virtuoso is significant because it enables precise design, simulation, and layout of fundamental digital building blocks used in complex integrated circuits. Cadence Virtuoso provides a powerful environment to model gates such as AND, OR, NAND, NOR, XOR, and NOT using CMOS technology with accurate foundry models, allowing for detailed functional verification and performance analysis. Through DC and transient simulations, designers can verify logical correctness, evaluate switching behavior, measure propagation delays, rise/fall times, power consumption, and noise margins.

4.1 Design and simulate 2-input NAND gate with CMOS technology in Cadence Virtuoso using 180nm technology, and analyze their dynamic characteristics such as propagation delay, rise/fall time, and power consumption



2-input NAND gate

4.2 Design and simulate 2-input NOR gate with CMOS technology in Cadence Virtuoso using 180nm technology, and analyze their dynamic characteristics such as propagation delay, rise/fall time, and power consumption



2-input NOR gate

Try:

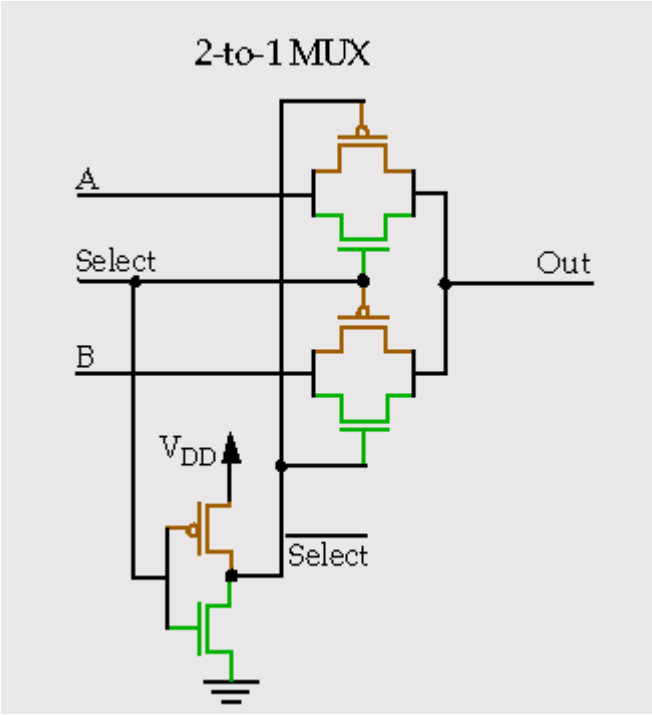
1. Design and simulate 2-input XOR and XNOR gates using CMOS technology in Cadence Virtuoso. Investigate the impact of input transition times and load capacitance on the performance of these gates. Perform parametric analysis across different supply voltages and temperatures to evaluate robustness .

2. Design and simulate 2-input NAND and NOR gates using CMOS technology in Cadence Virtuoso. Analyze their dynamic characteristics such as propagation delay, rise/fall times, and switching power dissipation. Additionally, study the effect of varying load capacitance, input signal rise/fall times, and supply voltage on gate performance. Perform parametric analysis and corner simulations to evaluate the gates under different process, voltage, and temperature (PVT) conditions.

5. MULTIPLEXER (4X1)

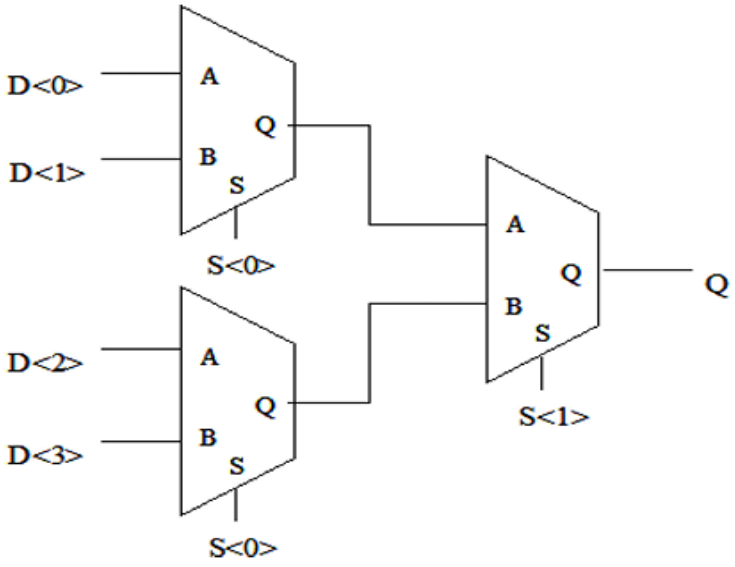
Implementing a 4×1 multiplexer in Cadence Virtuoso is significant because it allows accurate design, simulation, and layout of a fundamental combinational logic circuit used in data selection and routing within digital systems. Using CMOS technology, designers can build the multiplexer by combining logic gates or transmission gates and verify its functionality through transient simulations that test all possible input and select line combinations. Cadence Virtuoso enables precise analysis of propagation delay, power consumption, and output integrity using foundry-specific models.

5.1 Design and simulate a 2×1 multiplexer using CMOS logic in Cadence Virtuoso 180nm technology , and verify the output functionality through transient analysis.



2×1 multiplexer

5.2 Design and implement an 4x1 multiplexer by hierarchically using 2x1 multiplexer in Cadence Virtuoso environment, and verify the correctness of the output through functional simulation



4x1 multiplexer

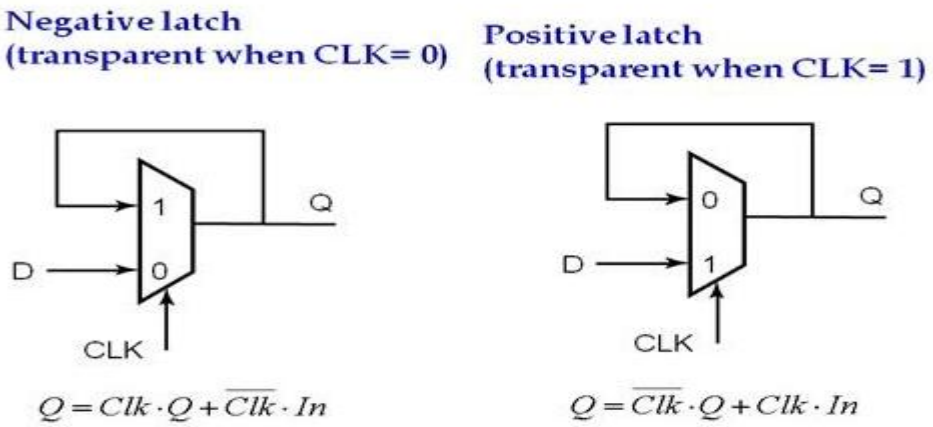
Try:

1. Design and simulate an 8×1 multiplexer using two 4×1 multiplexers and one 2×1 multiplexer in Cadence Virtuoso. In addition to verifying the logical correctness, perform dynamic analysis by measuring propagation delay, rise/fall times, and power dissipation under varying input conditions. Investigate the impact of different load capacitances and supply voltages on performance.
2. Design and implement a hierarchical multiplexer system by cascading multiple 2×1 multiplexers to construct a 4×1 and subsequently an 8×1 multiplexer using CMOS logic in Cadence Virtuoso. Analyze the functional correctness, propagation delay at each level, and cumulative delay. Perform power and timing analysis under various input switching conditions and validate the scalability of the design.

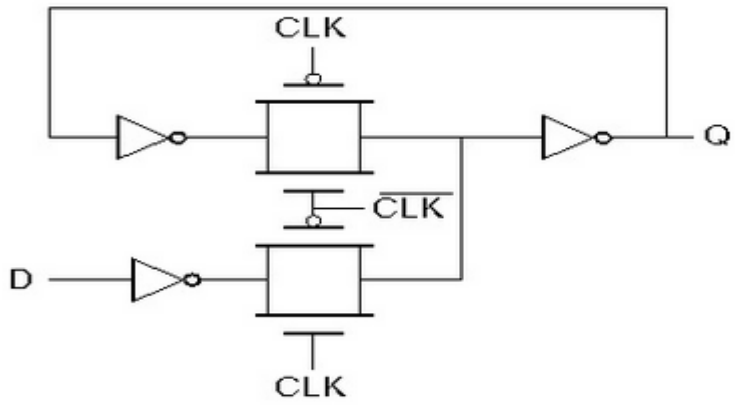
6.LATCHES

Implementing latches in Cadence Virtuoso is significant because it enables accurate design, simulation, and layout of essential sequential logic elements used for data storage and synchronization in digital systems. Using CMOS technology, designers can construct SR, D, or transparent latches and analyze their behavior under various input and control signal conditions through transient simulations. This allows evaluation of critical performance parameters such as setup and hold times, propagation delay, power consumption, and metastability. Cadence Virtuoso provides a robust environment for schematic capture, functional verification, and timing analysis using foundry-accurate transistor models..

6.1 Design a positive level-sensitive latch using multiplexers in CMOS technology and simulate it using Cadence Virtuoso. Verify its logical operation and analyze its behavior using static and DC analysis.



Negative and positive latches based on multiplexers.



Positive built by using transmission gates

6.2 Design a negative level-sensitive latch using multiplexers in CMOS technology and simulate it using Cadence Virtuoso. Verify its functionality and examine its behavior through static and DC analysis.

Try:

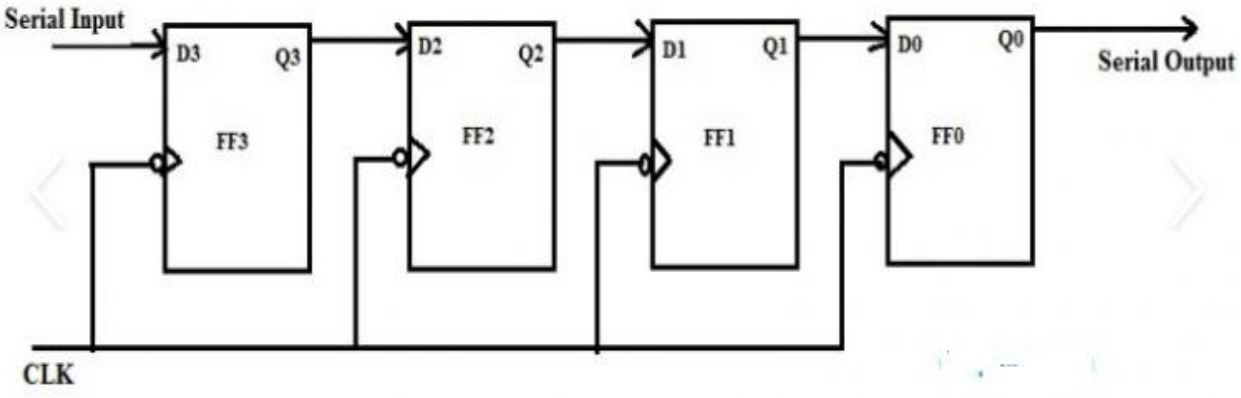
1. Design and simulate a positive level-sensitive latch using multiplexers in CMOS technology with Cadence Virtuoso. Analyze its timing behavior by measuring propagation delay, setup and hold times. Perform parametric sweeps to observe the effects of varying supply voltage and load capacitance on latch performance. Additionally, evaluate the power dissipation and conduct corner analysis to assess robustness under process, voltage, and temperature (PVT) variations.
2. Design and simulate a data synchronization circuit using a positive level-sensitive latch in Cadence Virtuoso. Implement the latch as part of a simple 2-stage synchronizer used to transfer data between two modules operating under different clock domains. Verify the functionality of the design through transient and static analysis. Evaluate the impact of clock skew and setup/hold time violations. Analyze timing performance, power dissipation, and robustness against metastability under varying supply voltages and temperatures.

7. REGISTERS

Implementing registers in Cadence Virtuoso is significant because it allows for precise design, simulation, and layout of critical sequential storage elements used in data buffering, synchronization, and state retention in digital systems. Registers, typically built from cascaded D flip-flops or latches, are designed using CMOS technology and verified through transient simulations to ensure correct data capture on clock edges, as well as to evaluate setup and hold times, clock-to-Q delay, power consumption, and timing

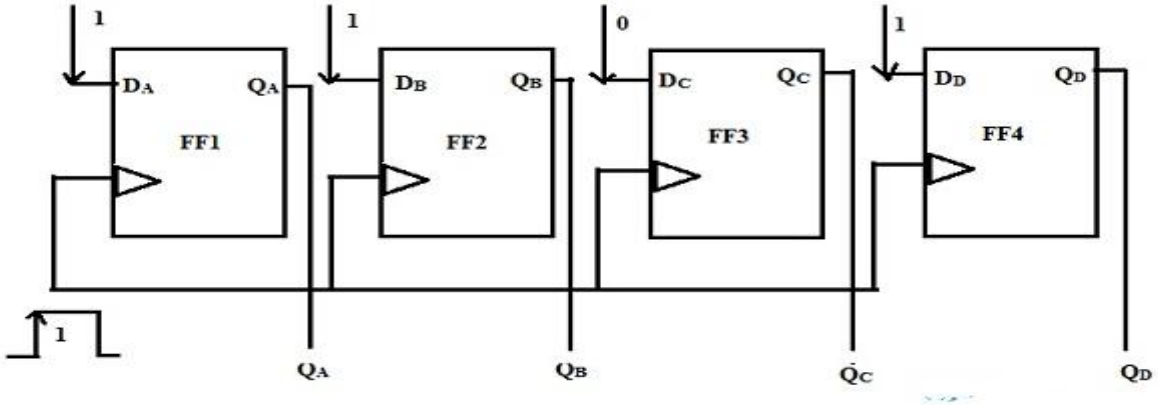
reliability. Cadence Virtuoso provides a comprehensive environment to model these behaviors with foundry-accurate transistor models, enabling early detection of timing violations and functional errors.

7.1 Design 4 bit SISO shift registers using D flip-flop, obtain the transient analysis , analyze the power and delay from the simulation result .



4 bit SISO shift registers

7.2 Design 4 bit PIPO shift registers using D flip-flop, obtain the transient analysis, analyze the power and delay from the simulation result.



4 bit PIPO shift

Try:

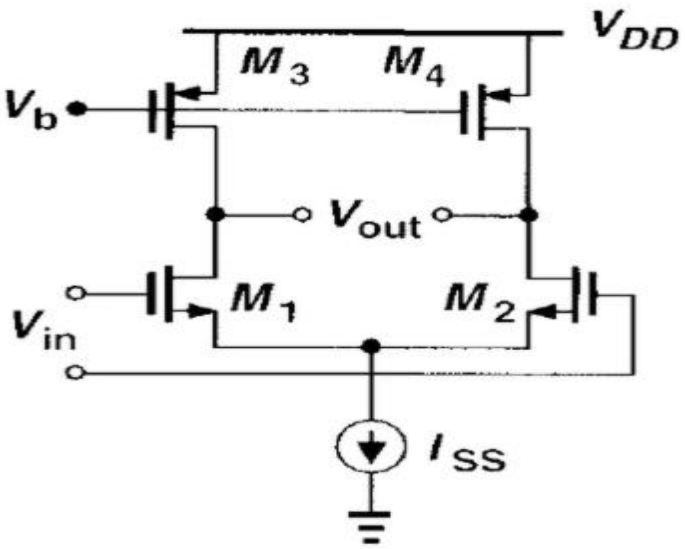
1. Design Master and slave flip flop using D flip flop obtain the transient analysis, analyze the power and delay from the simulation result.
2. Design universal shift register obtain the transient analysis, analyze the power and delay from the simulation result.

8. DIFFERENTIAL AMPLIFIER

A differential amplifier is an analog circuit that amplifies the difference between two input signals while rejecting any signals common to both (common-mode signals). It is commonly used in analog front-end circuits, operational amplifiers, and sensor interfaces due to its high common-mode rejection ratio (CMRR). The basic differential pair consists of two matched transistors (typically NMOS or BJTs) with their sources (or emitters) connected together to a current source. It provides balanced outputs, which can be single-ended or differential. The gain of a differential amplifier depends on the transconductance (gm) of the transistors and

the load resistance. In Cadence Virtuoso, differential amplifiers are analyzed using DC, AC, and transient simulations to evaluate parameters like gain, CMRR, input offset, and bandwidth. They are essential in noise-sensitive and high-precision analog applications**.**

8.1 Design Differential amplifier schematic using cadence virtuoso 180nm technology, create symbol , Simulate differential amplifier measure the output voltage, gain, CMRR of Differential amplifiers.



Differential amplifier

8.2 Design Differential amplifier using MOSFETS. Simulate differential amplifier by giving differential input and common mode parameters as input and analyze various circuit parameters.

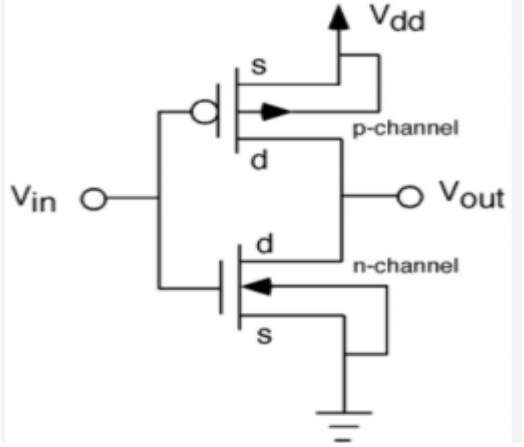
Try:

1. Design a two stage operational amplifier and do the transient ,ac analysis and dc analysis of amplifier.

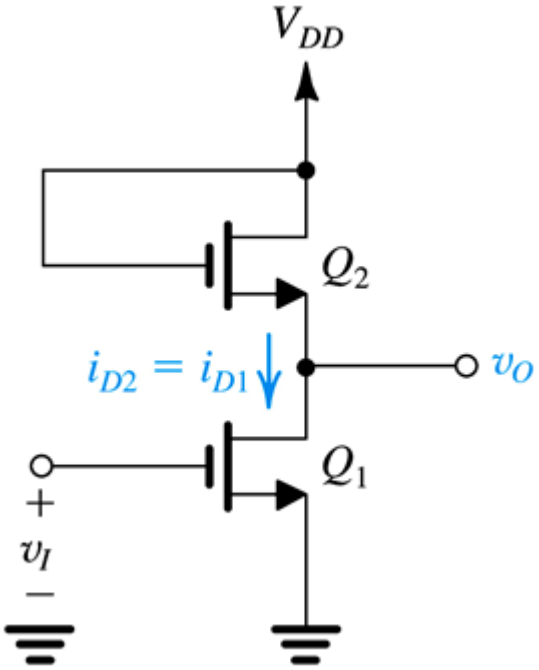
2. Design layout of differential amplifier and do the prelayout and post layout simulations.

9. LAYOUT OF CMOS INVERTER

9.1 Use the lambda based design rules ,design the layout of CMOS inverter and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.



9.2 Use the lambda based design rules ,design the layout of nMOS inverter and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.



nMOS inverter

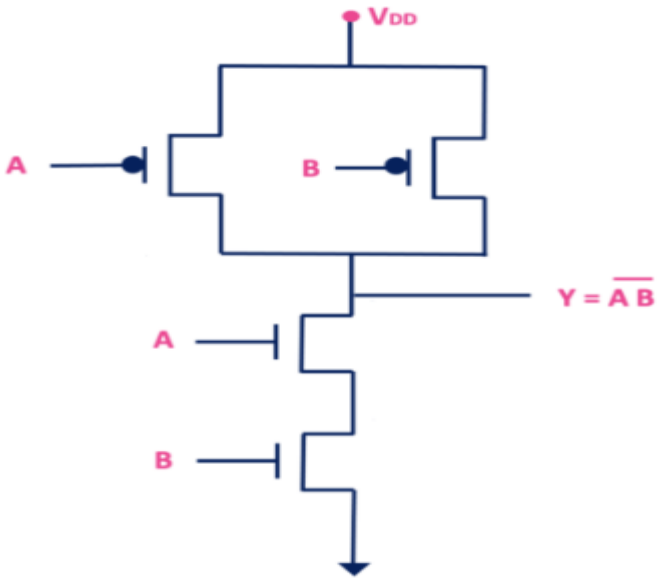
Try:

1. Use the lambda based design rules ,design the layout of nMOS inverter and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-layout and post-layout simulations,.
2. Use the lambda based design rules ,design the layout of nMOS inverter and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.

10. LAYOUT OF NAND/NOR GATES

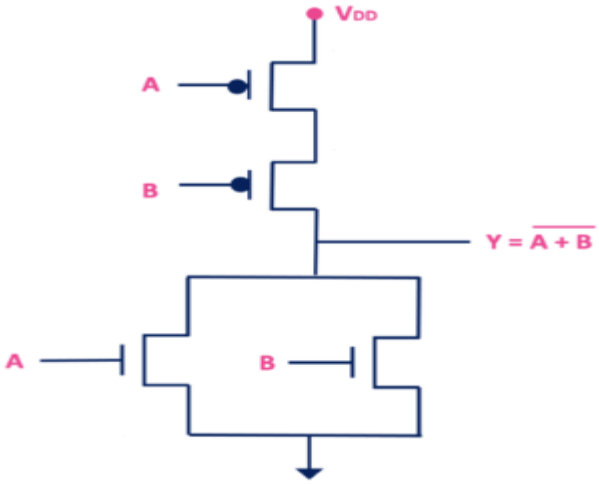
The NAND gate is a universal logic gate that outputs low only when both inputs are high; otherwise, the output is high. It is built using CMOS technology with PMOS transistors in parallel and NMOS transistors in series. The NOR gate also belongs to universal gates and outputs high only when both inputs are low; otherwise, it gives a low output. In CMOS layout, NOR has PMOS in series and NMOS in parallel. These gates are fundamental in digital design and can be used to construct any logic function. NAND is preferred for implementation due to its smaller transistor count and faster performance in most cases. In Cadence Virtuoso, both gates are designed using schematic capture, layout design, DRC, and LVS checks. They are essential building blocks in combinational logic circuits like adders, multiplexers, and memory.

10.1 Use the lambda based design rules ,design the layout of NAND gate and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-layout and post-layout simulations.



NAND gate

10.2 Use the lambda based design rules ,design the layout of NOR gate and do the DRC,LVS and RCX Extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.



NOR gate

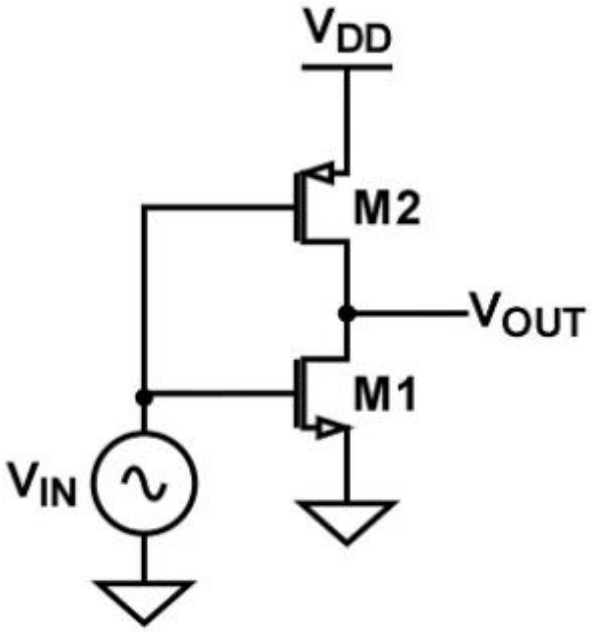
Try:

1. Use the lambda based design rules ,design the layout of EX-OR gate using CMOS and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.
2. Use the lambda based design rules ,design the layout of any AND-OR-INVERTER form expression and do the DRC,LVS and RCX extraction and find the parasitic values in the design ,do the pre-lay out and post-layout simulations,.

11. COMMON SOURCE AMPLIFIER

The common source amplifier is a mosfet configuration where the source is grounded, the input is applied to the gate**,** and the output is taken from the drain. It provides high voltage gain and is widely used for signal amplification in analog circuits. This amplifier exhibits 180° phase inversion between input and output. It typically has moderate input impedance and high output impedance. The mosfet operates in the saturation region for linear amplification. It may include a load resistor at the drain and a bypass capacitor at the source to improve gain. In cadence virtuoso, it is analyzed using dc, ac, and transient simulations to measure gain, bandwidth, and signal behavior.

11.1 Design common source amplifier using NMOSFETs with current source as load using cadence virtuoso using 180nm technology . Plot the transfer characteristics, dc characteristics and ac characteristics.



common source amplifier

11.2 Design common source amplifier using NMOSFETs with current source as load using cadence virtuoso using 180nm technology . Design layout and perform DRC, RCS, LVX checking and calculate parasitic values.

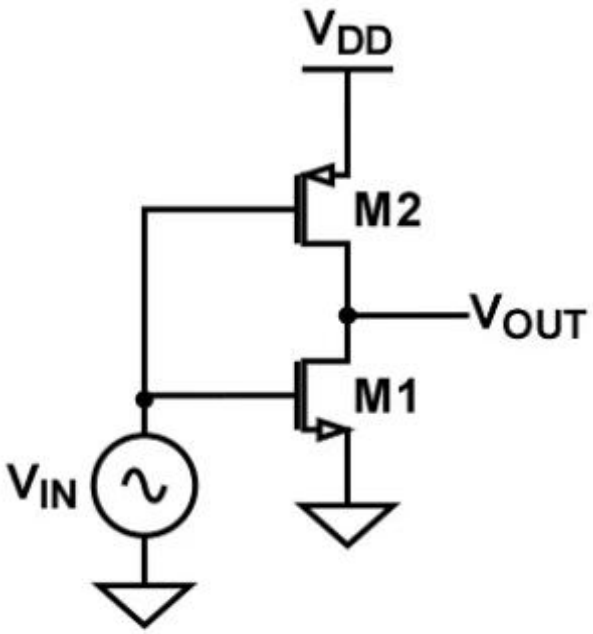
Try:

1. Design the Common Gate amplifier schematic (Current Gain of 30dB) and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
2. Design two stage operational amplifier using cadence virtuoso using 180nm technology Plot the transfer characteristics, dc characteristics and ac characteristics **,**calculate transconductance, voltage gain, bandwidth.

12. COMMON DRAIN AMPLIFIER

The common drain amplifier**,** also known as **a** source follower**,** is a MOSFET amplifier configuration where the drain is connected to a fixed voltage (usually Vdd) and the output is taken from the source. It provides no voltage gain **(**gain ≈ 1), but offers high input impedance and low output impedance**,** making it ideal for impedance matching**.** The amplifier operates in the saturation region for linear amplification. It produces an output signal in phase with the input (no phase inversion). It's widely used as a voltage buffer between high-impedance and low-impedance stages. In Cadence Virtuoso, it's analyzed using DC, AC, and transient simulations to confirm gain and impedance behavior**.**

12.1 Design common drain amplifier using NMOSFETs with current source as load using cadence virtuoso using 180nm technology. Plot the transfer characteristics, dc characteristics and ac characteristics**.**



common drain amplifier

12.2 For the above circuit do the parametric analysis or different width values of nMos transistor ,calculate transconductance, voltage gain, bandwidth of common drain amplifier using cadence analog design environment for 180nm technology.

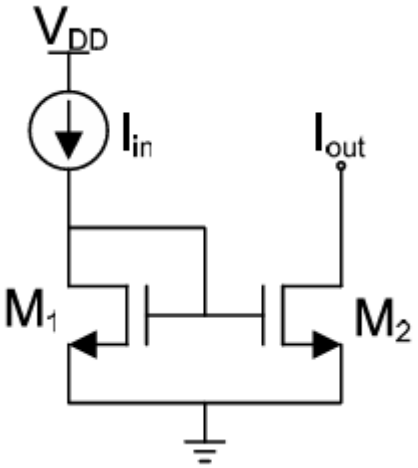
Try:

1. Design common drain amplifier using cadence virtuoso using 180nm technology Plot the transfer characteristics, dc characteristics and ac characteristics **,**calculate transconductance, voltage gain, bandwidth
2. Design two stage operational amplifier using cadence virtuoso using 180nm technology Plot the transfer characteristics, dc characteristics and ac characteristics **,**calculate transconductance, voltage gain, bandwidth.

13.CURRENT MIRROR

The current mirror is an analog circuit that senses the reference current and generates the copy or number of copies of the reference current, with the same characteristics. The replicated current is as stable as the reference current source. The replicated current could be the same as the reference current (Icopy = IREF), or it could be either multiple or fraction of the reference current. (Icopy = N*Iref or Icopy = (1/N)*IREF).

13.1 Design current mirror amplifier using MOSFETS, Find out output impedance, drain to source current, and output voltage using simulation. using cadence virtuoso using 180nm technology.



current mirror amplifier

13.2 Do the layout design for current mirror amplifier using MOSFETS, do the layout design DVS, RCX, LVS extraction fine the parasitic values using cadence virtuoso using 180nm technology.

Try:

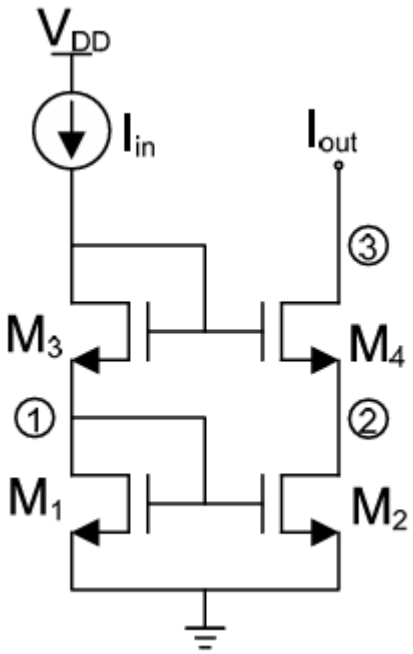
1. Design a simple 1:1 current mirror that has a compliance voltage of 100 mV to 150 mV. The output current should be 100 µA. Determine W/L for each transistor and what the expected output impedance should be.

2. Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 1 MΩ. Assume a 50 µA input current.

14 CASCODE CURRENT MIRROR

A cascoded current mirror is an improved version of the basic current mirror that offers higher output resistance and better current matching. It typically uses four transistors: two for the basic mirror and two additional cascode transistors. These cascode devices reduce the effect of output voltage variations on the current, improving accuracy. The higher output resistance also enhances gain in analog amplifiers. Cascoding helps maintain a constant drain-source voltage across the mirroring transistors, reducing channel-length modulation. This configuration is widely used in analog integrated circuits for biasing and signal processing.

14.1 Design cascaded current mirror amplifier using MOSFETS, Find out output impedance, drain to source current, and output voltage using simulation. using cadence virtuoso using 180nm technology.



cascaded current mirror amplifier

14.2 Do the layout design for cascoded current mirror amplifier using MOSFETS, do the layout design DVS, RCX, LVS extraction fine the parasitic values using cadence virtuoso using 180nm technology.

Try:

1. Design a simple low voltage cascoded current mirror in cadence virtuoso using 180nm technology and analyze the dc analysis and ac response of it.

2. Design a low-voltage cascode current mirror do the layout design DVS, RCX, LVS extraction fine the parasitic values using cadence virtuoso using 180nm technology.

I. TEXT BOOKS:

1. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill Publications, 2002
2. Allen Holberg, " CMOS Analog Circuit Design" , Oxford Publications, 2002.
3. R. Jacob Baker, " CMOS Mixed Circuit Design" , Wiley Publications, 2nd Edition 2008.

II. REFERENCE BOOKS:

1. Rabaey, "Digital Integrated Circuits ", Pearson, 2nd Edition 2016.
2. Kenneth Martin, David John Mohammad Rashid, "Analog Integrated Circuit Design", Wiley Publications, 2nd Edition 2013.

III. ELECTRONICS RESOURCES:

1. http://ee.usc.edu/~redekopp/ee209/virtuoso/setup/USCVLSI-VirtuosoTutorial.pdf
2. http://www.tedpavlic.com/teaching/osu/ece327

IV.. MATERIALS ONLINE

1. Course template
2. Lab Manual