

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

VLSI DESIGN LABORATORY								
VI Semester: ECE								
Course Code	Category	Hours /Week			Credits	Maximum Marks		
AECD44	Core	L	Т	Р	С	CIA	SEE	Total
		-	-	2	1	40	60	100
Contact Classes: Nil	Tutorial Classes: Nil	Practical Classes: 45				Total Classes: 45		
Prerequisite: Linear IC Applications								

I. COURSE OVERVIEW:

This course provides the hands-on experience on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design. VLSI designs are widely used in automobiles, mobiles and embedded processors.

II. COURSES OBJECTIVES:

The students will try to learn

- I. Modern tools for functional level to physical layout with verification at intermediate stages in the VLSI design flow in top-down approach.
- II. Design and simulations of analog, digital and mixed circuits for optimum values of area over head, power and time delay.
- III. The chip design through a practical approach using advanced modern tools such as vivado and cadence for front end and back end.

III. COURSE OUTCOMES:

At the end of the course students should be able to:

- CO 1 Make use of the static, dynamic and noise margin parameters of CMOS circuits for calculating figure of merit
- CO 2 Analyze complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays.
- CO 3 Utilize existing small building block and circuit symbols with necessary inter connections to realize complex design.
- CO 4 Examine the conditions for optimum performance of lathes and registers with the knowledge of digital system design.
- CO 5 Identify bandwidth, gain, and common mode rejection ratio parameters for cascode amplifiers to protect amplifier from miller effect.
- CO 6 Apply the design rule check and Layout versus schematic check on layout of MOS circuits to verify spacing rules between layers.

IV. COURSE CONTENT:

WEEK-1: NMOSFET

Verification of Transfer, dc characteristics and parametric analysis of NMOSFET in Cadence Virtuoso Schematic Editor using 180nm technology.

WEEK-2: CMOS INVERTER

Design of CMOS Inverter and calculating power dissipation and delay using Transfer, dc characteristics and parametric analysis.

WEEK-3: RING OSCILLATOR

Finding the frequency of oscillation for Ring oscillator using Cadence virtuoso environment

WEEK-4: LOGIC GATES

Design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS design style

WEEK-5: 4X1 MULTIPLEXER

Design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.

WEEK -6: LATCHES

Design and verify the latch operation using Static and dc analysis.

WEEK -7: REGISTERS

To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.

WEEK -8: DIFFERENTIAL AMPLIFIER

Design and simulate differential amplifier, Measure the values of output voltage and CMRR of Differential amplifier

WEEK -9: LAYOUT OF CMOS INVERTER

Design layout of CMOS INVERTER find the parasitic values using DRC, LVS, RCX extraction using cadence virtuoso environment.

WEEK -10: LAYOUT OF NAND / NOR GATES

Design layout of NAND / NOR GATES, find the parasitic values using DRC, LVS, RCX extraction using cadence virtuoso environment.

WEEK -11: COMMON SOURCE AMPLIFIER

Calculate voltage gain, bandwidth and body effect using Transient, DC characteristics and AC response of common source amplifier in Analog design environment.

WEEK -12: COMMON DRAIN AMPLIFIER

Calculate voltage gain, bandwidth and body effect using Transient, DC characteristics and AC response of common drain amplifier in Analog design environment.

WEEK -13: CURRENT MIRROR

Design basic current mirror in analog design environment and find out output impedance, drain to source current, and output voltage using simulation.

WEEK -14: CASCODE CURRENT MIRROR

Design cascode current mirror in analog design environment and find out output impedance, drain to source current, and output voltage using simulation.

V. TEXT BOOKS:

- 1. Razavi," Design of Analog CMOS Integrated Circuits", Tata McGraw Hill Publications, 2002
- 2. Allen Holberg, "CMOS Analog Circuit Design", Oxford Publications, 2002.
- 3. R. Jacob Baker, "CMOS Mixed Circuit Design", Wiley Publications, 2nd Edition 2008.

VI. REFERENCE BOOKS:

- 1. Rabaey, "Digital Integrated Circuits", Pearson, 2nd Edition 2016.
- 2. Kenneth Martin, David John Mohammad Rashid, "Analog Integrated Circuit Design", Wiley Publications, 2nd Edition 2013.

VII. ELECTRONICS RESOURCES:

- 1. http://ee.usc.edu/~redekopp/ee209/virtuoso/setup/USCVLSI-VirtuosoTutorial.pdf
- 2. http://www.tedpavlic.com/teaching/osu/ece327/

VIII. MATERIALS ONLINE

- 1. Course Content
- 2. Lab Manual