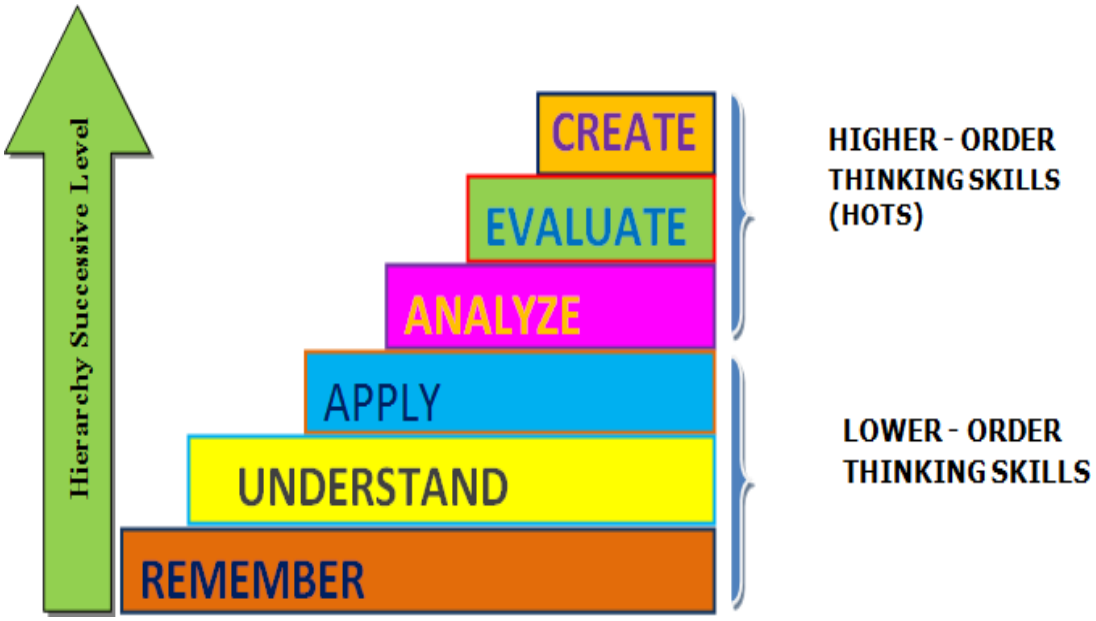
COURSE DESCRIPTOR BOOKLET

M.Tech

ELECTRONICS AND COMMUNICATION ENGINEERING

(Accredited by NBA)

R-16 REGULATIONS



BLOOM'S TAXONOMY OF LEARNING OUTCOMES

.....Moving Towards Perfection in Engineering

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Approved by AICTE; Affiliated to JNTUH and Accredited by NAAC with 'A' Grade
Dundigal, Hyderabad - 500 043

Vision

To produce professionally competent Electronics and Communication Engineers capable of effectively and efficiently addressing the technical challenges with social responsibility.

Mission

The mission of the Department is to provide an academic environment that will ensure high quality education, training and research by keeping the students abreast of latest developments in the field of Electronics and Communication Engineering aimed at promoting employability, leadership qualities with humanity, ethics, research aptitude and team spirit.

Contents

Program Education Objectives and Outcomes

As Per NBA Norms Post June, 2016

Semester: I-I, I-II, II-I, II-II

Part – I

PROGRAM EDUCATIONAL OBJECTIVES AND OUTCOMES

First version 22 July, 2014

Program Educational Objectives, Program Outcomes and Assessment Criteria (Approved by DAC ECE on 3/9/2014):

Electronics and Communication Engineering Department Advisory Council: The Electronics and Communication Engineering Department Advisory Council (ECEDAC) includes a diverse group of experts from academic and industry, as well as alumni representation. The Advisory Board meets annually, or as needed, for a comprehensive review of the Electronics and Communication Engineering Department strategic planning and programs. The Advisory Council meets with administration, faculty and students and prepares a report, which is presented to principal. In each visit, the Department of Electronics and Communication Engineering responds to the report indicating improvements and amendments to the program.

1. PROGRAM EDUCATIONAL OBJECTIVES, OUTCOMES AND ASSESSMENT CRITERIA

Learning Outcomes, Assessment Criteria

The educational aims of a module are statements of the broad intentions of the teaching team. They indicate the objectives that the teaching team intends to cover and the learning opportunities that are necessary to be available to the student. A learning outcome is a statement that indicates the content that a learner (student) is expected to know, understand and/or be able to do at the end of a period of learning. It is advisable to express learning outcomes with the common prefix:

'On completion of (the period of learning e.g. module), the student is expected to be able to…'

Generally, learning outcomes do not specify curriculum, but more general areas of learning. It is not possible to prescribe precisely how specific a learning outcome statement should be. There is a balance to be struck between the degree of specificity in a learning outcome statement and that achieved by the assessment criteria. If there are too many learning outcomes for a module, then either they are becoming assessment criteria or they are specifying too much curricular detail. The curriculum should be described in the range statement. Too few learning outcomes are unlikely to provide sufficient information on the course. As a guide, there should be between 4 and 8 learning outcomes for a course.

The Program Educational Objectives (PEOs) of the Electronics and Communication Engineering department are broad statements or road maps describing career and professional objectives that intend the graduates to achieve through this program.

2. M. TECH – EMBEDDED SYSTEMS PROGRAM

EDUCATIONAL OBJECTIVES

A graduate of Institute of Aeronautical Engineering in Embedded systems discipline should have a successful career in Electronics and Communication Engineering or a related field, and within three to five years, should attain the following:

PROGRAM EDUCATIONAL OBJECTIVES:

PEO1. Research and development

Be successful practicing professionals or pursue doctoral studies in allied areas, contributing significantly to **research and development** activities

PEO2. Demonstrate

Demonstrate technical competence, such as identifying, formulating, analyzing, and creating engineering solutions using appropriate current embedded engineering techniques, skills, and tools.

PEO3. Communicate

To work and **communicate** effectively in inter-disciplinary environment, either in a team or independently and establish leadership qualities.

PEO4. Apply

An ability to **apply** in-depth knowledge to evaluate, analyze and synthesize existing and novel designs.

These objectives are quite broad by intention, as Electronics and Communication Engineering graduates may seek further education or work in diverse areas. To make these objectives meaningful, they may be demonstrated by performance, actions, or achievements.

i. To prepare the students who will be able to attain a solid foundation in Embedded systems fundamentals with an attitude to pursue continuing education.

- Make the students to understand their aptitude to choose the correct path of study which leads to higher qualifications and heights in the chosen field.
- Should be prepared to undergo rigorous training in their fields of working.
- Be capable of utilizing the solid foundation obtained at institute to apply successfully in solving the real time engineering problems.
- Students need to have creative thinking processes that are acquired through good training to find solutions to engineering problems.

ii. To prepare the students to function professionally in an increasingly international and rapidly changing world due to the advances in technologies and concepts and to contribute to the needs of the society.

- Adoptability and accommodative mind set to suit modern world and changing economies.

- By working hard in the chosen field and sharing the professional experience at different forums within and outside the country.
- Desirable to be a member of various professional societies (IEEE, IETE, ISTE, IE, and etc.) to keep yourself abreast with the state-of-the-art technology.
- Should continue additional education in a broad range of subjects other than engineering may be needed in order to meet professional challenges efficiently and effectively.
- Continuous interaction with educational and research institutions or industrial research labs.
- Have a sound foundation of knowledge within a chosen field and achieve good depth and experience of practice in it.
- Able to relate knowledge within chosen field to larger problems in society and able to appreciate the interaction between science, technology, and society.
- Strong grasp of quantitative reasoning and an ability to manage complexity and ambiguity.
- To conduct research, and design, develop, test and oversee the development of electronic systems for global upliftment.
- Applying scientific knowledge to solve technical problems and develop products and services that benefit the society.
- An electronic engineer shall contribute to the society by research, design and development, testing and evaluation, application by manufacturing, maintenance by service, management and other functions like sales, customer service and etc.

iii. To prepare the students to acquire and exercise excellent leadership qualities, at various levels appropriate to their experience, to address issues in a responsive, ethical, and innovative manner.

- Gives ample opportunity to work in diverse fields to acquire leadership roles in professional circles outside the workplace.
- Should keep in mind that the opportunities may change with the times.
- Should be prepared for creative solo and collaborative brainstorming sessions.
- Be able to inspire the team with selfless motivation and attitude to achieve success.
- Ability to think laterally or at-least have a flexibility of thought and make choices based on the requirement for situation.

iv. To prepare the students who will be able to excel, in their careers by being a part of success and growth of an organization, with which they are associated.

- To achieve this, the focus should not be limited to an engineering curriculum and even to the class room.
- Continuing professional education by attending short term in courses design to update engineering skills.
- A lifelong commitment to learning new and specialized information.
- Should accept first person responsibility and should take the initiative in carrying out the work.
- Should be determined for the duty and dedicated to work and have passion for that.
- Be delight at work with a positive attitude.
- Should be a detailed worker so that one can be relied by the organization.

The department of Electronics and Communication Engineering periodically reviews these objectives and as part of this review process, encourages comments from all interested parties including current students, alumni, prospective students, faculty those who hire or admit our graduates to other programs members of related professional organizations, and colleagues from other educational institutions.

3. M. TECH –EMBEDDED SYSTEMS PROGRAM OUTCOMES:

Masters of the embedded systems Program Outcomes will demonstrate:

PROGRAM OUTCOMES:

PO1. Engineering Knowledge

Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.

PO2. Teamwork and Project Management

Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.

PO3. Develop and Novel Designs

Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.

PO4. Analyze Complex Systems

Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.

PO5. Technical Presentation Skills

Write and present a substantial technical report / document.

PO6. Development of Solutions

Independently carry out research / investigation and development work to solve practical problems.

PO7. Lifelong learning

Recognize the need to engage in lifelong learning through continuing education and research.

4. MAPPING OF PROGRAM EDUCATIONAL OBJECTIVES TO PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES

The following Figure shows the correlation between the PEOs and the POs and PSOs

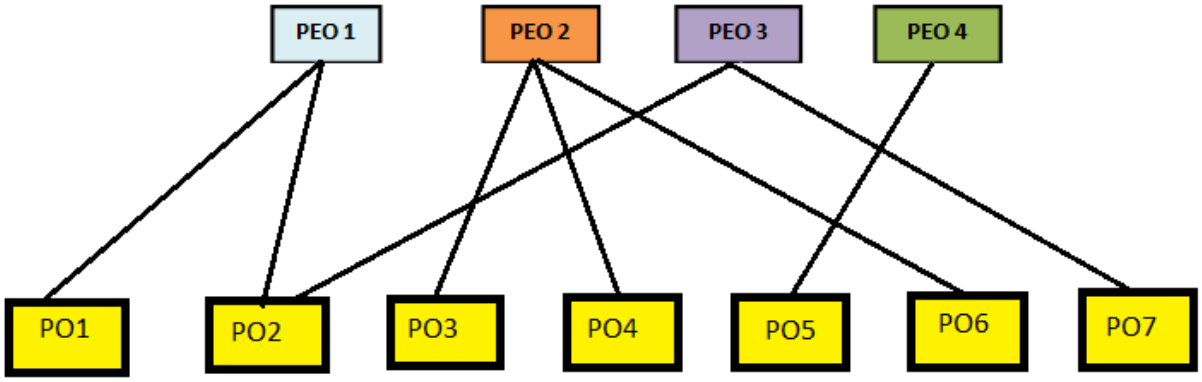


Figure: *Correlation between the PEOs and the POs*

The following Table shows the correlation between the Program Educational Objectives and the Program Outcomes & Program Specific Outcomes

	Program Educational Objectives		Program Outcomes
I	Be successful practicing professionals or pursue doctoral studies in allied areas, contributing significantly to **research and development** activities	**PO1**	**Engineering Knowledge** Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.
		PO2	**Teamwork and Project Management** Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
II	To be in a position to analyze real life problems and design socially accepted and economically feasible solutions in the respective fields.	**PO3**	**Develop and Novel Designs** Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.
		PO4	**Analyze Complex Systems** Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.
		PO6	**Development of Solutions** Independently carry out research / investigation and development work to solve practical problems.
III	To work and **communicate** effectively in inter-disciplinary environment, either	**PO2**	**Teamwork and Project Management** Function on multidisciplinary environments by

	independently or in a team, and establish leadership qualities.		working cooperatively, creatively and responsibly as a member of a team.
		PO7	**Lifelong learning** Recognize the need to engage in lifelong learning through continuing education and research.
IV	An ability to **apply** in-depth knowledge to evaluate, analyze and synthesize existing and novel designs.	**PO5**	**Technical Presentation Skills** Write and present a substantial technical report / document.

5. RELATION BETWEEN THE PROGRAM OUTCOMES AND PROGRAM EDUCATIONAL OBJECTIVES

A broad relation between the Program Educational Objectives and the Program Outcomes is given in the following table:

POs \ PEOs →		(1) Research and development	(2) Demonstrate	(3) Communicate	(4) Apply
PO1	Engineering Knowledge	3			
PO2	Teamwork and Project Management	3		1	
PO3	Develop and Novel Designs		3		
PO4	Analyze Complex Systems		3		
PO5	Technical Presentation Skills				3
PO6	Development of Solutions		3		
PO7	Lifelong learning			3	

Relationship between Program Outcomes and Program Educational Objectives
Key: 3 = Highly 2 Medium; 1 = Low

6. PROGRAM OUTCOMES OF (M.Tech) EMBEDDED SYSTEMS MASTERS

Masters from accredited programs must achieve the following learning outcomes, defined by broad areas of learning.

The outcomes are distributed within and among the courses within our curriculum, and our students are assessed for the achievement of these outcomes, as well as specific course learning objectives, through testing, surveys, and other faculty assessment instruments. Information obtained in these assessments is used in a short-term feedback and improvement loop.

Each Electronics and Communication Engineering student will demonstrate the following attributes by the time they masters:

PO1. Engineering Knowledge

Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems

Performance Criteria Definitions

- Identify the concepts and/or equations
- Execute the solution using a logic and structured approach
- Evaluate the solution of the problem

PO2. Teamwork and Project Management

Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments

Performance Criteria Definitions

- Awareness of global effects of the product / practice /event
- Understanding of economic factors
- Awareness of implications to society at large

PO3. Develop Novel designs

Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations

Performance Criteria Definitions

- Use modern engineering tools for the system design, simulation and analysis
- Use software applications effectively to write technical reports and oral presentations
- Use modern equipment and instrumentation in the design process, analysis and troubleshooting

PO4. Analyze Complex Systems

Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions

Performance Criteria Definitions

- Identify problem/purpose
- Prepare hypothesis
- Outline procedure
- List materials and equipment
- Conduct experiment
- Record observations, data and results
- Perform analysis
- Document conclusions

PO5. Technical Presentation skills

Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

Performance Criteria Definitions

- Use appropriate format and grammatical structure
- Create a well organized document
- Present the results appropriately
- Demonstrate effective oral communication

PO6. Development of Solutions

Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations

Performance Criteria Definitions

- Awareness of global effects of the product / practice / event
- Understanding of economic factors
- Awareness of implications to society at large

PO7. Life-long Learning

Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

Performance Criteria Definitions

- Find relevant sources of information
- Participate in school or professional seminars
- Participate in students or professional associations

I SEMESTER

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**Embedded C**				
Course Code	BES001				
Programme	M. Tech				
Semester	I	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	3	2
Course Faculty	Ms N.Anusha, Assistant Professor				

I. COURSE OVERVIEW:

This course provides the basic knowledge over the programming and functionality of the embedded systems. Embedded C is most popular programming language in software field for developing electronic gadgets. Each processor used in electronic system is associated with embedded software.This plays a key role in performing specific function by the processor and all the device working is based on microcontroller that are programmed by embedded C.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	-	-	Computer programming	-
UG	-	-	Embedded systems	-

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIAExamination	Total Marks
Embedded C	70 Marks	30 Marks	100 Marks

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IOT, Processor technology, storage technology.	3	Term paper, Seminar
PO 2	Function on multidisciplinary environment by working cooperatively, creatively and responsibly as a member of a team.	3	Term paper, Seminar
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronics product designing.	2	Term paper
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Term paper, Seminar

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	Term paper, Seminar

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Understand embedded C and use it for programming embedded system.
II	Apply techniques for data transfer between I/O ports and memory.
III	Apply object oriented programming for designing embedded system.
IV	Use timers to generate time delay.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the basic knowledge about embedded processor and hardware and software interrupts.	CLO 1	Understanding the basic concepts of Embedded C
		CLO 2	Understanding the basic concept of interfacing and interrupts
		CLO 3	Understanding the basic of 8051 architecture
CO 2	Understand the basic embedded programming concepts in C and assembly language	CLO 4	Analyze the programming on switches
		CLO 5	Analysis of processor scheduling real time.
		CLO 6	Understanding the programming language tools.
CO 3	Illustrate various tasks in real time operating systems including inter-task communication and software development tool	CLO 7	Understanding the basic concepts of coding on embedded C.
		CLO 8	Applications of software on real time constraints
CO 4	Explore on various testing concepts on real time applications.	CLO 9	Analyse the programming on real time constraints
		CLO 10	Understanding the testing concepts on real time applications
CO 5	Apply embedded programming concepts on case study.	CLO 11	Understanding the basic concepts on software architecture
		CLO 12	Understanding the real time concepts using case study.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES001.01	CLO 1	Understanding the basic concepts of Embedded C.	PO1	2
BES001.02	CLO 2	Understanding the basic concept of interfacing and interrupts	PO1, PO2	3
BES001.03	CLO 3	Understanding the basic of 8051 architecture	PO1, PO3	3
BES001.04	CLO 4	Analyse the programming on switches	PO4	3
BES001.05	CLO 5	Analysis of processor scheduling real time.	PO3, PO4	3
BES001.06	CLO 6	Understanding the programming language tools.	PO1, PO6	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES001.07	CLO 7	Understanding the basic concepts of coding on embedded C.	PO4	3
BES001.08	CLO 8	Applications of software on real time constraints	PO6	2
BES001.09	CLO 9	Analyse the programming on real time constraints	PO3, PO6	3
BES001.10	CLO 10	Understanding the testing concepts on real time applications	PO3, PO4	3
BES001.11	CLO 11	Understanding the basic concepts on software architecture	PO4	3
BES001.12	CLO 12	Understanding the real time concepts using case study	PO2, PO3	2

3= High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENTOF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 4	PO 6
CO 1	3	3	3		
CO 2	3		2	3	2
CO 3				3	3
CO 4			2	3	3
CO 5		3	3	2	

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes				
	PO1	PO2	PO3	PO4	PO6
CLO 1	2				
CLO 2	3	3			
CLO 3	3		3		
CLO 4				3	
CLO 5			3	3	
CLO 6	3				3
CLO 7				3	
CLO 8					2
CLO 9			3		3
CLO 10			3	3	
CLO 11				3	
CLO 12		2	2		

XII. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO1,PO2, PO3, PO4, PO6	SEE Exams	PO1, PO2, PO3, PO4, PO6	Seminarand Term Paper	PO1, PO2, PO3, PO4, PO6
Laboratory Practices	-	Viva	-	Mini Project	-

XIII. ASSESSMENT METHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✔	Assessment of Mini Projects by Experts		

XIV. SYLLABUS

UNIT-I	
PROGRAMMING EMBEDDED SYSTEMS IN C Introduction, what is an embedded system, which processor should you use, which programming language should you use, which operating system should you use, how do you develop embedded software, conclusions; Introduction, what's in a name, the external interface of the standard 8051, reset requirements, clock frequency and performance, memory issues, I/O pins, timers, interrupts, serial interface, power consumption ,conclusions.	
UNIT-II	
SWITCHES Introduction, basic techniques for reading from port pins; Example: Reading and writing bytes, example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), example: counting goats, conclusions.	
UNIT-III	
ADDING STRUCTURE TO THE CODE Introduction, object oriented programming with C, the project header (MAIN.H), the port header (PORT.H); Example: Restructuring the „Hello Embedded World" example, Example: Restructuring the goat-counting example, further examples and conclusions.	
UNIT-IV	
MEETING REAL-TIME CONSTRAINTS Introduction, creating hardware delays using Timer 0 and Timer 1, example: Generating a precise 50 ms delay, example: Creating a portable hardware delay, Why not use Timer 2? The need for timeout mechanisms, creating loop timeouts and example: Testing loop timeouts, example: A more reliable switch interface, Creating hardware timeouts, example: Testing a hardware timeout, conclusions.	
UNIT-V	
CASE STUDY: INTRUDER ALARM SYSTEM Introduction, The software architecture, key software components used in this example, running the program, the software, conclusions.	
Text Books:	
1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008.	
Reference:	
1.Nigel Gardner, "The Microchip PIC in CCS C", Ccs Inc, 2ndRevision Edition, 2002.	

Reference E-Text Books:
1. http://www.keil.com/forum/5973/ 2. http://nptel.ac.in/courses/Webcourse,contents/IIT%20Kharagpur/Embedded%20systems/New 3. http://nptel.iitg.ernet.in/courses/Elec_Engg/IIT%20Delhi/Embedded%20Systems%20(Video).htm 4. http://freevideolectures.com/Course/2999/Embedded-Systems-I/5

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand the concepts of embedded system.	Introduction, what is an embedded system	T1:1.1, 1.2
4-6	Understand the concepts of operating system.	which processor should you use, which programming language should you use	T1:2.1
7-9	Design the programming on embedded system	which operating system should you use how do you develop embedded software	T1:2.2, 2.3
10-13	Understand the standard the concepts of 8051	key software components used in this examplethe external interface of the standard 8051	T1:4.1, 4.2, 4.3
14-16	Analyze the clock functions and I/O	reset requirements, clock frequency and performancememory issues, I/O pins, timers, interrupts	T1:4.2, 4.4
17-20	Analyze the concepts of interface and port pins	serial interface, power consumption, conclusions Introduction, basic techniques for reading from port pins	T1: 5.1, 5.2
21-22	Design the example programming and basic concepts of pull-up resistor	Example programs on Reading and writing bytes, Reading and writing bits simple versionReading and writing bits, The need for pull-up resistors	T1:6.1, 6.2, 6.4
23-27	Understand the basic of switch and c programming	Dealing with switch bounce, Example: Reading switch inputs (basic code)Introduction, object oriented programming with Cthe project header (MAIN.H), the port header (PORT.H);	T1:7.2, 7.3, 7.4
28-36	Design the example programming on goat counting	Restructuring the Hello Embedded World Restructuring the goat-counting example, further examples and conclusions	T1:8.1, 8.3
37-40	Understand the basic concepts of timer and testing the hardware.	Introduction, creating hardware delays using Timer 0 and Timer 1, Generating a precise 50 ms delay, example: Creating a portable hardware delay, Why not use Timer 2 Creating hardware timeouts, example: Testing a hardware timeout, conclusions	T1:5.3
41-45	Understand the basic concepts of software architecture.	Introduction, The software architecture key software components used in this example	T1:5.5, 5.6, 5.7

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Real time programming software architecture	Seminars / Guest Lectures / NPTEL	PO 1, PO 4, PO 3
2	Design concepts of embedded c	Work Shops/ Guest Lectures / NPTEL	PO 6, PO 2

Prepared by:

Mrs. Anusha. N, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**WIRELESS LANS AND PANS**			
Course Code	**BES002**			
Programme	**M.Tech**			
Semester	**I**			
Course Type	**Elective**			
Regulation	**IARE - R16**			
Course Structure	**Theory**		**Practical**	
	Lectures	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**3**
Course Faculty	**Mrs. M Kalyani, Assistant Professor**			

I. COURSE OVERVIEW:

Embedded systems have become the next inevitable wave of technology, finding application in diverse fields of engineering. The goal of this course is to impart training to graduate engineers, in specialized area of Embedded Systems so that they can develop expertise in developing and deploying embedded systems over a wide range of applications. This course provides the basic knowledge over the hardware units and devices for design of embedded systems. It also provides the information about the Use architectures of embedded RISC processors and system on chip processor design of embedded systems. This course is intended to Analyze interrupt latency, context switching time, for development of device drives for timing devices.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	--	--	Wireless Communication and Networks	--

III. MARKSDISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Wireless LANs and PANs	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IoT, Processor technology, storage technology.	3	Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Term paper and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	NPTEL Videos and Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand different WLAN topologies and transmission techniques.
II	Interpret Bluetooth and Zigbee technologies.
III	Enhance the understanding of 3G systems and 4G networks.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describefirst and second generation cellular systems and analyze cellular communications from 1G to 3G.	CLO 1	Understand and analyze first and second generation cellular systems.
		CLO 2	Analyze cellular communications from 1G to 3G.
		CLO 3	Explain wireless 4G systems, and wireless spectrum.
CO 2	Understand and analyze WLAN topologies and analyze transmission techniques.	CLO 4	Describe carrier sense multiple access (CSMA), carrier sense multiple access with collision detection (CSMA/CD), carrier sense multiple access with collision avoidance(CSMA/CA).
		CLO 5	Explain WLAN topologies and analyze transmission techniques
		CLO 6	Distinguish random access methods.
CO 3	Demonstrate network architecture and analyze MAC layer issues and describe the importance of MAC layer applications.	CLO 7	Describe importance of MAC layer applications
		CLO 8	Explain network architecture and analyze MAC layer issues.
CO 4	Explore Bluetooth technology and Bluetooth specifications, describe the importance of wireless private area networks.	CLO 9	Describe the importance of wireless private area networks.
		CLO 10	Explain Bluetooth technology and Bluetooth specifications.
		CLO 11	Analyze Enhancements to Bluetooth technology and applications
CO 5	Develop practical skills in the use of ZigBee components and network topologies.	CLO 12	Describe IEEE 802.15.3, The IEEE 802.15.4
		CLO 13	Understand ZigBee components and network topologies.
		CLO 14	Analyze Device architecture and network topologies

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES002.01	CLO 1	Understand and Analyze First and Second Generation Cellular Systems.	PO 1	2
BES002.02	CLO 2	Analyze Cellular Communications from 1G to 3G.	PO 1, PO 2	2
BES002.03	CLO 3	Explain Wireless 4G systems, The Wireless Spectrum.	PO 1, PO 3	1
BES002.04	CLO 4	Describe Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple	PO 2, PO 3	3

		Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).		
BES002.05	CLO 5	Explain WLAN Topologies and Analyze Transmission Techniques	PO 1	3
BES002.06	CLO 6	Distinguish Random Access Methods.	PO 1	3
BES002.07	CLO 7	Describe importance of Wireless Local Area Networks.	PO 3	3
BES002.08	CLO 8	Explain Network Architecture and Analyze MAC Layer issues.	PO 1, PO 3	2
BES002.09	CLO 9	Describe importance of Wireless Private Area Networks.	PO 3, PO 6	2
BES002.10	CLO10	Explain Bluetooth technology and Bluetooth specifications.	PO 1, PO 6	3
BES002.11	CLO 11	Analyze Enhancements to Bluetooth technology and applications	PO 2	2
BES002.12	CLO 12	Describe IEEE 802.15.3, The IEEE 802.15.4	PO 2, PO 6	3
BES002.13	CLO 13	Understand ZigBee components and network topologies.	PO 2	2
BES002.14	CLO 14	Analyze Device architecture and network topologies	PO 3, PO 6	3

3 = High; 2 = Medium; 1 = Low2

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes(PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	3	2	2	
CO 2	3	3	3	
CO 3	2		3	
CO 4	3	2	3	2
CO 5		2	3	3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcome(PO)			
	PO 1	PO 2	PO 3	PO 6
CLO 1	3			
CLO 2	3	2		
CLO 3	3		3	
CLO 4		3	2	

CLO 5	2			
CLO 6	2			
CLO 7			3	
CLO 8	2		3	
CLO 9			3	3
CLO 10	3			3
CLO 11		2		
CLO 12		2		3
CLO 13		2		
CLO 14			2	3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO2, PO3, PO 6	SEE Exams	PO1, PO2, PO3, PO 6	Seminar and Term Paper	PO1, PO2, PO3, PO6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I
WIRELESS SYSTEM&RANDOM ACCESS PROTOCOLS Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA)..
UNIT II
WIRELESS LANS Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology.
UNIT III
THE IEEE 802.11 STANDARD FOR WIRELESS LANS Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol..
UNIT IV
WIRELESS PANS Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatter net formation.

UNIT V
THE IEEE 802.15 WORKING GROUP FOR WPANS The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband..
TEXT BOOKS:
1. Carlos de Morais Cordeiro, Dharma Prakash Agrawal, "AdHoc and Sensor Networks", World Scientific, 2011.
2. Vijay K.Garg, "Wireless Communications and Networking", Morgan Kaufmann Publishers, 2009.
REFERENCES:
1. KavehPahlaram, Prashant Krishnamurthy, "Wireless Networks", PHI, 2002.
2. Marks Ciampor, Jeorge Olenewa, "Wireless Communication", Cengage Learning, 2007.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand and analyze first and second generation cellular systems.	Introduction, first and second generation cellular systems, Cellular communications from 1G to3G Wireless 4G systems, The wireless Spectrum	T1: 5.1, T1: 5.2, R1: 1.7
4-6	Analyze Cellular Communications from 1G to 3G.	Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA)	T1:6.1-6.2, T1: 6.3, T1: 6.4-6.6
7-9	Explain Wireless 4G systems, The Wireless Spectrum.	Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Transmission Techniques: Wireless Networks	T1:6.4-6.6, T1:6.7-6.8, T1: 6.15 R2:7.1, 8.1
10-13	Describe Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).	comparison of wired and Wireless LANs, WLAN Technologies: Infrared technology, UHF narrowband technology	T1:7.1, 7.4 T1:7.7, T1: 7.8-7.10 R2:7.2
14-16	Explain WLAN Topologies and analyze transmission techniques	Spread Spectrum technology, Network Architecture, Physical layer,The Medium access control layer	T1: 6.12, T1: 9.4, R2: 4.2, T1: 9.6
17-20	Describe importance of Wireless Local Area Networks.	MAC Layer issues: Hidden terminal problem, Reliability, Collision avoidance, congestion avoidance, Congestion control	T1: 7.12, T1: 10.4, R2: 4.2, T1: 10.6
21-22	Explain Network architecture and analyze MAC layer issues.	Security, The IEEE 802.11e MAC protocol. The IEEE 802.11e MAC protocol. Introduction, importance of wireless PANs, the Bluetooth technology: history and applications	T1: 10.5, T1: 8.1 T1: 8.4, T1: 8.2, T1:8.5,T1

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
			:8.6 R2: 4.4
23-27	Describe importance of Wireless Private Area Networks.	Technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch, Bluetooth security	T1: 8.2 R2: 4.4, T1: 8.9
28-36	Explain Bluetooth technology and Bluetooth specifications.	Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering,	T1: 8.12-8.13, T1: 8.14
37-40	Analyze Enhancements to Bluetooth	QoS and Dynamics Slot Assignment, Scatter net formation., The IEEE 802.15.3, The IEEE 802.15.4, ZigBee components and network topologies	T1: 9.1, T1: 9.2, T1: 9.3
41-45	Describe IEEE 802.15.3, The IEEE 802.15.4	The IEEE 802.15.4 LR-WPAN device architecture, physical layer, data link layer, the network layer, applications, IEEE 802.15.3a ultra wideband.	R1:7.1-7.3, R1:7.4, R1:7.7

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Currently available Wireless Communication and Networks	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 6
2	Interfacing Modules	Work Shops/ Guest Lectures / NPTEL	PO 2, PO 6

Prepared By:
Ms. M Kalyani, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**COMPUTER ARCHITECTURE**				
Course Code	**BES003**				
Programme	**M.Tech**				
Semester	**I**	**ECE**			
Course Type	**Core**				
Regulation	**IARE - R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Mr. N Bhargav Kumar, Assistant Professor**				

I. COURSE OVERVIEW:

This course includes the organization and architecture of computer systems. It covers the advanced topics such as instruction level parallelism, addressing modes; register transfer notation; memory hierarchies design, hardware implementations of virtual memory, storage systems and design of interconnection networks and clusters.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	-	Digital System Design	4
UG	AEC010	-	Computer Organization	4
UG	AEC013	-	Microprocessors & Microcontrollers	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Computer Architecture	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	2	Seminar and Term Paper
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems..	2	Seminar and Term Paper
PO 5	Write and present a substantial technical report / document.	1	Guest Lectures
PO 6	Independently carry out research / investigation and development work to solve practical problems.	2	Seminars
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	1	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the Computer architecture
II	Design and implementation of an I/O system & cluster
III	Understand the algorithms of memory and storage management

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the cost measuring and reporting performance principles of computer design	CLO 1	Describe various trends in technology and performance principles of computer design.
		CLO 2	Demonstrate addressing modes , instruction set & encoding an instruction set.
		CLO 3	Discuss the role of a compiler
CO 2	Illustrate the concepts and hazards in instruction level parallelism.	CLO 4	Understand the process of high performance instruction delivery & hardware based speculation
		CLO 5	Understand the limitations of ILP ,VLIW approach .
CO 3	Explore the shared memory concepts in symmetric architecture and distributed systems.	CLO 6	Illustrate the cache performance & multi threading
		CLO 7	Describe virtual memory & examples
		CLO 8	Compare different shared memory architectures
CO 4	Understand the various storage devices used to design I/O system.	CLO 9	Describe buses & process of bench marking a storage device
		CLO 10	Design an I/O system
CO 5	Know the different practical issues invoked interconnected networks and clusters.	CLO 11	Demonstrate the Interconnection network media
		CLO 12	Examine the practical issues in interconnecting networks
		CLO 13	Illustrate the examples of Interconnection networks
		CLO 14	Design a cluster

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES003.01	CLO 1	Describe various trends in technology and performance principles of computer design.	PO 1, PO 5	2
BES003.02	CLO 2	Demonstrate addressing modes , instruction set & encoding an instruction set.	PO 4	2
BES003.03	CLO 3	Discuss the role of a compiler	PO 4	2
BES003.04	CLO 4	Understand the process of high performance instruction delivery & hardware based speculation	PO 1, PO 5	2
BES003.05	CLO 5	Understand the limitations of ILP ,VLIW approach .	PO 4, PO 5	2
BES003.06	CLO 6	Illustrate the cache performance & multi threading	PO 4	2
BES003.07	CLO 7	Describe virtual memory & examples	PO 1	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES003.08	CLO 8	Compare different shared memory architectures	PO 4	2
BES003.09	CLO 9	Describe buses & process of bench marking a storage device	PO 1, PO 5	2
BES003.10	CLO 10	Design an I/O system	PO 4, PO 6, PO 7	2
BES003.11	CLO 11	Demonstrate the Interconnection network media	PO 1, PO 5	2
BES003.12	CLO 12	Examine the practical issues in interconnecting networks	PO 1, PO 4	2
BES003.13	CLO 13	Illustrate the examples of Interconnection networks	PO 6	2
BES003.14	CLO 14	Design a cluster	PO 1, PO 6	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 4	PO 5	PO 6	PO 7
CO 1	2	1	1	-	-
CO 2	2	2	1	-	-
CO 3	2	2	-	-	-
CO 4	1	2	2	2	1
CO 5	1	2	1	2	-

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 4	PO 5	PO 6	PO 7
CLO 1	2		1		
CLO 2		2			
CLO 3		2		2	
CLO 4		2	1		
CLO 5		2	1		
CLO 6		2			
CLO 7	2				
CLO 8		2			
CLO 9	2		1		

CLO 10		2		2	1
CLO 11	2		1		
CLO 12	2	2			
CLO 13				2	
CLO 14	2			2	

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 4 PO 5,PO 6, PO 7	SEE Exams	PO 1, PO 4 PO 5,PO 6, PO 7	Seminar and Term Paper	PO 1, PO 4 PO 6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

Unit-I	**FUNDAMENTALS OF COMPUTER DESIGN:**
Technology trends, cost measuring and reporting performance quantitative principles of computer design, classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler	
Unit-II	**INSTRUCTION LEVEL PARALLELISM:**
overcoming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP; Compiler techniques, static branch protection, VLIW approach, hardware support for more ILP at compile time: hardware verses software solutions.	
Unit-III	**MEMORY HIERARCHY DESIGN:**
Cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM. Symmetric shared memory architectures, distributed shared memory, synchronization, multi threading.	
Unit-IV	**STORAGE SYSTEMS :**
Types, Buses, RAID, errors and failures, bench marking a storage device, designing an I/O system.	
Unit-V	**INTER CONNECTION NETWORKS AND CLUSTERS:**
Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster.	
Text Books:	
1. John. Hennessy, David A. Patterson Morgan Kufmann, “Computer Architecture a Quantitative Approach”, Elsevier, 4th Edition, 2007.	
Reference Books:	
1. Kai Hwang, A. Briggs, “Computer Architecture and Parallel Processing”, Mc Graw Hill, International Edition, 1986. 2. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architectures”, Pearson Education, 2nd Edition, 2009.	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1 - 3	Understand the merits and demerits in computer performance measurements	Introduction to fundamentals of computer design & technology, performance parameters of computer design.	T1: 5.1, T1: 5.2, R1: 1.7
4 - 6	Understand the impact of instruction set architecture on cost-performance of computer design	Classification of instruction set, memory addressing, type and size of operands & addressing modes for signal processing.	T1:6.1-6.2, T1: 6.3, T1: 6.4-6.6
7 - 9	Demonstrate addressing modes , instruction set & encoding an instruction set.	Operations in the instruction set, instructions for control flow, encoding an instruction set & the role of compiler	T1:6.4-6.6, T1:6.7-6.8, T1: 6.15 R2:7.1, 8.1
10 - 13	Interpret ways to take advantage of instruction level parallelism for high performance processor design	Introduction to ILP, limitations of ILP & Compiler techniques,	T1:7.1, 7.4 T1:7.7, T1: 7.8-7.10 R2:7.2
14 - 16	Illustrate the limitations of ILP &VLIW approach	Static branch protection, VLIW approach, hardware support for more ILP at compile time: hardware verses software solutions	T1: 6.12, T1: 9.4, R2: 4.2, T1: 9.6
17 - 20	Explain the concept of memory hierarchy design	Cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.	T1: 7.12, T1: 10.4, R2: 4.2, T1: 10.6
21 - 24	Compare different shared memory architectures .	Symmetric shared memory architectures, distributed shared memory, synchronization, multi threading	T1: 10.5, T1: 8.1 T1: 8.4, T1: 8.2, T1:8.5,T1:8.6 R2: 4.4
25 - 28	Describe buses & process of bench marking a storage device	Types, Buses, RAID, errors and failures,bench marking a storage device	T1: 8.2 R2: 4.4, T1: 8.9
29 - 32	Design an I/O system	designing an I/O system.	T1: 8.12-8.13, T1: 8.14
32 - 36	Know the different practical issues invoked interconnected networks	Interconnection network media, practical issues in interconnecting networks,	T1: 9.1, T1: 9.2, T1: 9.3
37 - 40	Design an interconnection networks	Examples of interconnecting networks	R1:7.1-7.3, R1:7.4, R1:7.7
41 - 45	Design a cluster	Cluster	T1: 9.5, T1: 9.6, T1: 9.7

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Encourage students to solve real time applications and prepare towards competitive security mechanisms.	NPTEL	PO 1, PO 4, PO 6
2	Practical approach should be given for designing a cluster	Laboratory Practices	PO 1, PO 6

Prepared By:

Mr. N Bhargav Kumar, Assistant Professor **HOD, ECE**

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**HARDWARE SOFTWARE CO - DESIGN**				
Course Code	**BES204**				
Programme	**M. Tech**				
Semester	**I**	**ECE**			
Course Type	**Elective**				
Regulation	**IARE - R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	**-**	**3**	**3**	**2**
Course Faculty	**Dr. S China Venkateswarlu, Professor**				

I. COURSE OVERVIEW:

The course presents state-of-the-art concepts and techniques for design of embedded systems consisting of analog, hardware and software components. Discussed topics include system modeling and specification, architectures for embedded mixed-signal systems, performance evaluation, and system optimization. The course follows the top-down design paradigm based on IP cores. Course requirements include three reports on system specification and various co-design tasks. Recent progress and diversification in microelectronics and the emergence of several conceptually new approaches to computability have provided foundations for a number of new and interesting computer architectures. At the same time, new approaches developed within Software Engineering support the development of Software Architectures. The mapping between these two abstractions can be formalized, leaving open the possibility that Hardware Design and Software Design can proceed in parallel, leading to systems-level specification and implementation.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3
UG	-	-	Embedded systems	-

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIAExamination	Total Marks
Hardware Software Co-Design	70 Marks	30 Marks	100 Marks

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IoT, Processor technology, storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environment by working cooperatively, creatively and responsibly as a member of a team.	3	Tutorials, Seminar
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronics product designing.	2	Guest Lectures

PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Tutorials, Seminar
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	Guest Lectures

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Differentiate the various prototyping and emulation techniques for co-design models.
II	Understand the compilation techniques for embedded processor architecture.
III	Use verification tools for verification of co-design.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the basic knowledge Co-design models-Languages and a generic co-design methodology. Hardware-software system	CLO 1	Understanding the basicconcept of Co-design models, architectures, languages and a generic co-design methodology
		CLO 2	Study of Co-synthesis algorithms: hardware software synthesis algorithms. Hardware, software partitioning distributed system co-synthesis
		CLO 3	Examine the various prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques
		CLO 4	Discuss the various principlesinvolved in the system communication infrastructure target architectures.
CO 2	Understand the basic Co-Synthesis algorithms and Hardware software synthesis algorithms.	CLO 5	Describe the Architecture specialization techniques,system communication infrastructure, target architecture and application system classes, architecture for control dominated systems 8051
		CLO 6	Study the Architectures for High performance control, architecture for datadominated systems ADSP21060, TMS320C60, mixed systems.
		CLO 7	Study the Modern embedded architectures, embedded software development needs.
CO 3	Illustrate various Prototyping and Emulation techniques, Emulation environments, development and prototyping architecture specification techniques Systems.	CLO 8	FundamentalsCompilation technologies, practical consideration in a compiler development environment.
		CLO 9	Study the Design , co-design, the co-design computational model, concurrency coordinating concurrent computations ,

CO 4	Explore on Compilation Techniques , Modern Embedded Architectures, Embedded Software development –Practical, Compile development environment	CLO 10	Understand the interfacing components, design verification, implementation verification, verification tools, interface verification.
		CLO 11	Study the Level specification and design-I system, level specification,
		CLO 12	Study the design representation for system level synthesis, system level specification languages;
CO 5	Explore Designing specification and verification and Language for System-Multi language co-simulation, Cosyma system and Lycos system.	CLO 13	Understand the Level specification and design-II
		CLO 14	Understanding the basic concepts on software architecture
		CLO 15	Understanding the real time concepts using case study.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES204.01	CLO 1	Understanding the basicconcept of Co-design models, architectures, languages and a generic co-design methodology	PO1	2
BES204.02	CLO 2	Study of Co-synthesis algorithms: hardware software synthesis algorithms. Hardware, software partitioning distributed system co-synthesis	PO1, PO2	3
BES204.03	CLO 3	Examine the various prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques	PO1, PO2	3
BES204.04	CLO 4	Discuss the various principlesinvolved in the system communication infrastructure target architectures.	PO2, PO3	3
BES204.05	CLO 5	Describe the Architecture specialization techniques,system communication infrastructure, target architecture and application system classes, architecture for control dominated systems 8051	PO3, PO4	3
BES204.06	CLO 6	Study the Architectures for High performance control, architecture for data dominated systems ADSP21060, TMS320C60, mixed systems.	PO4, PO5	3
BES204.07	CLO 7	Study the Modern embedded architectures, embedded software development needs.	PO5	3
BES204.08	CLO 8	FundamentalsCompilation technologies, practical consideration in a compiler development environment.	PO5	2
BES204.09	CLO 9	Study the Design , co-design, the co-design computational model, concurrency coordinating concurrent computations ,	PO3, PO6	3
BES204.10	CLO 10	Understand the interfacing components, design verification, implementation verification, verification tools, interface verification.	PO3, PO4	3
BES204.11	CLO 11	Study the Level specification and design-I system, level specification,	PO4	3
BES204.12	CLO 12	Study the design representation for system level synthesis, system level specification languages;	PO4, PO3	2
BES204.13	CLO 13	Understand the Level specification and design-II	PO3, PO6	3
BES204.14	CLO 14	Analyze Heterogeneous specifications and multi language co-simulation	PO5, PO6	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES204.15	CLO 15	Analyze the cosyma system and lycos system.	PO6	3

3= High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENTOF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 4	PO 6
CO 1	3	3	3		
CO 2	3		2	3	2
CO 3				3	3
CO 4			2	3	3
CO 5		3	3	2	

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes				
	PO1	PO2	PO3	PO4	PO6
CLO 1	2				
CLO 2		3			
CLO 3	3		3		
CLO 4				3	
CLO 5			3	3	
CLO 6	3				3
CLO 7				3	
CLO 8					2
CLO 9			3		3
CLO 10			3	3	
CLO 11				3	
CLO 12		2	2		2
CLO 13	3			2	
CLO 14			3		
CLO 15		2		3	3

XII. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO1,PO2,PO3, PO4, PO6	SEE Exams	PO1, PO2,PO3, PO4, PO6	Seminarand Term Paper	PO1,PO2,PO3, PO4, PO6
Laboratory Practices	-	Viva	-	Mini Project	-

XIII. ASSESSMENT METHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS

UNIT-I	CO-DESIGN ISSUES
Co-design models, architectures, languages and a generic co-design methodology; Co-synthesis algorithms: hardware software synthesis algorithms: Hardware, software partitioning distributed system co-synthesis.	
UNIT-II	**PROTOTYPING AND EMULATION**
prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure target architectures: Architecture specialization techniques, system communication infrastructure, target architecture and application system classes, architecture for control dominated systems8051,Architectures for High performance control, architecture for data dominated systems ADSP21060, TMS320C60, mixed systems.	
UNIT-III	**COMPILATION TECHNIQUES**
Modern embedded architectures, embedded software development needs. Compilation technologies, practical consideration in a compiler development environment.	
UNIT-IV	**DESIGN SPECIFICATION AND VERIFICATION**
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations , interfacing components, design verification , implementation verification, verification tools, interface verification.	
UNIT-V	**LANGUAGES FOR SYSTEM**
Level specification and design-I system, level specification, design representation for system level synthesis, system level specification languages; Level specification and design-II: Heterogeneous specifications and multi language co-simulation, cosyma system and lycos system.	
Text Books:	
1. Jorgen Staunstrup, Wayne Wolf, "Hardware / Software Co-Design Principles and Practice", Springer, 2nd Edition, 2009. 2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware/Software Co-Design", Kluwer Academic Publishers, 1st Edition, 2012.	
Reference Books:	
1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design," Springer Issues and Practices", Elsevier, 1st Edition, 2005.	
Web References:	
1. http://www.springer.com/in/book/9781461437369 2. http://www.springer.com/us/book/9781441960009 3. http://rijndael.ece.vt.edu/gezel2/book	

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the basic concept of Co-Design Issues and Co-design	Co-Design Issues and Co-design	T1:2.3 to 2.7 R1: 1.5 to 1.8
4-6	Introduction toCo-designmodels, architectures and languages	Co-design models, architectures and languages	T1:1.4 R1: 1.9 to 1.10
7-9	Examine a generic co-design methodology, Co-synthesis	co-design methodology, Co-synthesis algorithms	T1:1.3 R1: 2.2 to 2.6

Lecture No	Topic Outcomes	Topics to be covered	Reference
	algorithms and hardware software synthesis algorithms		
10-13	Understand Hardware,software partitioning distributed system co-synthesis. Prototyping and emulation techniques	Hardware,software partitioning distributed system emulation techniques	T1:4.1 to 4.8 R2: 2.7 to 2.8
14-16	Discuss prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques	prototyping and emulation environments, future developments in emulation	T1:5.5 to 5.9 R1: 2.9 to 2.10
17-20	Examine system communication infrastructure target architectures, Architecturespecialization techniques, system communication infrastructure and target architecture and application system classes	Systemcommunicationinfrastructure and target architecture and application system classes	T1:6.4 to 6.8 R1: 2.11 to 2.12
21-24	Discuss architecture for control dominated systems 8051, Architectures for High performance control, architecture for data dominated systems ADSP21060 and TMS320C60	8051, Architectures for High performance control, architecture for data dominated systems ADSP21060 and TMS320C60	T1:6.8 to 6.9 R1: 2.13 to 2.14
25-28	Understand mixed systems. Compilation Techniques,Modern embedded architectures and embedded software development needs	Compilation Techniques , Modern embedded architectures and embedded software development needs	T1:7.1 to 7.9 R1: 2.15 to 2.16
29-32	Study Compilation technologies, practical consideration in a compiler developmentenvironment, Design , co-design and the co-design computational model	Development environment, Design , co-design and the co-design computational model	T1:7.10 to 7.11 R1: 3.1 to 3.3
33-36	Understand concurrency coordinating concurrent computations, interfacing components, design verification and implementation verification	Interfacing components, design verification and implementation verification	T1:8.1 to 8.4 R1: 3.4 to 3.5
37-40	Examine verification tools, interface verification, Level specification and design-I system and level specification	Verification tools, interface verification, Level specification and design-I system and levelspecification	T1:8.5 to 8.7 R1: 3.6 to 3.7
41-45	Analyze design representation for system level synthesis, system level specification languages. Level specification and design-II. Heterogeneous specifications and multi language co-simulation and cosyma system and lycos system.	Design representation for system level synthesissystem level specification languages. Level specification and design-II. multi language co-simulation and cosyma system and lycos system	T1:8.8 to 8.9 R1: 3.8 to 3.9

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Design ofSoftware's and Hardware's	Seminars / Guest Lectures / NPTEL	PO 1, PO 4, PO 3

2	Compiler development environment	Work Shops / Guest Lectures / NPTEL	PO 6, PO 2
3	Cosyma system and lycos system.	Work Shops / Guest Lectures / Laboratory Practices	PO 2, PO 3

Prepared by:
Dr. S China Venkateswarlu, Professor **HOD, ECE**

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED NETWORKING**			
Course Code	**BES209**			
Programme	**M.Tech**			
Semester	**I**			
Course Type	**Core**			
Regulation	**R16**			
Course Structure	**Theory**		**Practical**	
	Lectures	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**3**
Course Faculty	**Mrs. G.Bhavana, Assistant Professor, ECE**			

I. COURSE OVERVIEW:

Embedded network systems are a key component that enables our modern society. The course focuses on the fundamentals of embedded system, networking protocols and wireless embedded network. The course includes communication protocols, USB, CAN bus and Ethernet cables. The knowledge derived from this course is useful in development of various projects and models in engineering and scientific professions.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	-	-	Computer Networking	-
UG	-	-	Microprocessor and Microcontroller	-

III. MARKSDISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Networking	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, and storage technology	3	Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	3	Term paper and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	2	Seminar and Guest Lectures
PO 4	Demonstrate the importance of embedded technologies	3	Term paper and Guest Lectures

	and design new innovative products for solving society relevant problems		
PO 6	Independently carry out research / investigation and development work to solve practical problems	3	NPTEL Videos and Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand embedded communication protocols to implement in embedded networking
II	Design of CAN network based systems
III	Use UDP, TCP and FTP in design of embedded networks.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe the Embedded networking, serial/parallel communication.	CLO 1	Outline the the concepts of Embedded Networking
		CLO 2	Examine the Serial/parallel Communication
		CLO 3	Understand the concept of RS232,RS485, I2C– pc parallel port programming
CO 2	Demonstrate the USB BUS, PIC microcontroller USB, CAN interface.	CLO 4	Demonstrate the USB BUS Communication, PIC 18 microcontroller USB interface, C programs
		CLO 5	Illustrate the CAN bus types of errors, PIC microcontroller CAN interface, simple application with CAN
CO 3	Develop the Ethernet cables	CLO 6	Examine the Ethernet cables and Communication
		CLO 7	Describe the internet in local and communications, inside the Internet protocol.
		CLO 8	Outline the Hardware options, cables.
CO 4	Develop the Ethernet using UDP,TCP	CLO 9	Illustrate Exchanging messages using UDP and TCP
		CLO 10	Demonstrate the serving web pages that respond to user Input, email for embedded systems
CO 5	Describe the Wireless Embedded Networking.	CLO 11	Compare the energy efficient MAC protocols, SMAC
		CLO 12	Demonstrate robust routing, data centric routing.
		CLO 13	Illustrate time synchronization network concepts

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BCS005.01	CLO 1	Outline the the concepts of Embedded Networking	PO 1	3

BCS005.02	CLO 2	Examine the Serial/parallel Communication	PO 1	3
BCS005.03	CLO 3	Understand the concept of RS232,RS485, I2C– pc parallel port programming	PO 3	2
BCS005.04	CLO 4	Demonstrate the USB BUS Communication, PIC 18 microcontroller USB interface, C programs	PO 3, PO 4	2
BCS005.05	CLO 5	Illustrate the CAN bus types of errors, PIC microcontroller CAN interface, simple application with CAN	PO 3, PO 4	3
BCS005.06	CLO 6	Examine the Ethernet cables and Communication	PO 2	3
BCS005.07	CLO 7	Describe the internet in local and communications, inside the Internet protocol	PO 2, PO 3	2
BCS005.08	CLO 8	Outline the Hardware options, cables.	PO 2, PO 3	3
BCS005.09	CLO 9	Illustrate Exchanging messages using UDP and TCP	PO 2, PO 4	3
BCS005.10	CLO 10	Demonstrate the serving web pages that respond to user Input, email for embedded systems	PO 2, PO 6	3
BCS005.11	CLO 11	Compare theenergy efficient MAC protocols, SMAC	PO 6	3
BCS005.12	CLO 12	Demonstrate robust routing, data centric routing.	PO 3	2
BCS005.13	CLO 13	Illustrate time synchronization network concepts	PO 1	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes(Po's)				
	PO 1	PO 2	PO 3	PO 4	PO 6
CO 1	3		3		
CO 2			3	3	
CO 3		2	3		
CO 4		2		3	2
CO 5	2		3		2

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes(PO'S)				
	PO 1	PO 2	PO 3	PO 4	PO 6
CLO 1	3				
CLO 2	3				

CLO 3			2		
CLO 4			3	2	
CLO 5			3	2	
CLO 6		3			
CLO 7		2	3		
CLO 8		3	3		
CLO 9		3		2	
CLO 10		2			3
CLO 11					3
CLO 12			2		
CLO 13	2				

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO2,PO3, PO4, PO6	SEE Exams	PO1, PO2 PO3, PO4,PO6	Seminar and Term Paper	PO1, PO2, PO3PO4, PO6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I
INTRODUCTION TO EMBEDDED SYSTEMS Embedded Networking: Introduction, serial/parallel communication, serial communication protocols, RS232 standard, RS485, synchronous serial protocols, serial peripheral interface, inter integrated circuits I2C– pc parallel port programming, ISA/PCI bus protocols, fire wire.
UNIT II
USB AND CAN BUS USB bus, introduction, speed identification on the bus, USB states, USB bus communication: Packets ,data flow types, enumeration, descriptors, PIC 18 microcontroller USB interface, C programs; CAN bus: Introduction, frames, bit stuffing, types of errors, nominal bit timing, PIC microcontroller CAN interface, simple application with CAN
UNIT III
ETHERNET BASICS Elements of a network, inside Ethernet, building a network: Hardware options, cables, connections and network speed. Design choices: Selecting components, Ethernet controllers, using the internet in local and communications, inside the Internet protocol.
UNIT IV
EMBEDDED ETHERNET Exchanging messages using UDP and TCP: Serving web pages with dynamic data, serving web pages that respond to user Input, email for embedded systems, using FTP, keeping devices and network secure.

UNIT V
WIRELESS EMBEDDED NETWORKING Wireless sensor networks: Introduction, applications, network topology, localization, time synchronization, energy efficient MAC protocols, SMAC, energy efficient and robust routing, data centric routing
TEXT BOOKS:
1. Frank Vahid, Tony Givargis, "Embedded Systems Design: AUnified Hardware/Software Introduction" John & Wiley Publications, 1st Edition, 2002.
2. Jan Axelson, "Parallel Port Complete: Programming, Interfacing and using the PCs Parallel Printer Port", Penram Publications, 1stEdition, 1996.
REFERENCES:
3. Dogan Ibrahim, "Advanced PIC Microcontroller Projects in C: from USB to RTOS with the PIC18F Series" Elsevier, 1st Edition, 2008.
1. Jan Axelson, "Embedded Ethernet and Internet Complete", Penram Publications, 2nd Edition,2003.
2. Bhaskar Krishnamachari, "Networking Wireless Sensors", Cambridge press, 1st Edition, 2000.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand the Embedded networking.	Introduction to Embedded networking, serial/parallel communication	T1:1.1, 1.2
4-6	DescribeRS232,RS485	RS232 standard, RS485, Inter integrated circuits I2C– pc parallel port programming, ISA/PCI bus protocols, fire wire	T1:2.1
7-9	Understand the USB bus.	Introduction to USB bus, speed identification on the bus	T2:2.2, 2.3
10-13	Understand the PIC microcontroller USB,CAN	PIC 18 microcontroller USB interface, C programs, Types of errors, nominal bit timing, PIC microcontroller CAN interface, simple application with CAN	T1:4.1, 4.2, 4.3
14-16	Implementing the web pages using UDO, TCP.	Exchanging messages using UDP and TCP, Serving web pages with dynamic data	T1:4.2, 4.4
17-20	Understand the concepts of FTP.	Email for embedded systems, using FTP, keeping devices and network secure	T2: 5.1, 5.2
21-22	Understand the concepts of Wireless sensor networks.	Introduction to wireless sensor networks	T2:6.1, 6.2, 6.4
23-27	Develop the sensor network, toplogy.	Sensor network Applications, network topology, localization, Time synchronization	T2:7.2, 7.3, 7.4
28-36	Evaluate MAC, SMAC protocols.	Energy efficient MAC protocols, SMAC	T2:8.1, 8.3
37-40	Understand the robust routing.	Energy efficient and robust routing	T1:5.3
41-45	Understanding the concept of Data centric routing.	Data centric routing.	T1:5.5, 5.6, 5.7

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Currently available processors and microcontrollers	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 4
2	Interfacing Modules	Seminars / Guest Lectures / NPTEL	PO 2,PO 3, PO 6

Prepared By:
Ms. G Bhavana, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTRODUCTION TO AEROSPACE ENGINEERING**				
Course Code	BAE701				
Programme	M.Tech				
Semester	I	ECE			
Course Type	Open elective				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Chief Coordinator	Mr. R Sabari Vihar, Assistant Professor				
Course Faculty	Mr. R Sabari Vihar, Assistant Professor				

I. COURSE OVERVIEW:

Introduction to Aerospace engineeringcovers the fundamental concepts, and approaches of aerospaceengineering, and are highlighted through lectures on aeronautics, astronautics, and design. Active learning aerospace modules make use of information technology. Student teams are immersed in a hands-on, lighter-than-air (LTA) vehicle design project, where they design, LTA vehicles. The connections between theory and practice are realized in the design exercises. The performance, weight, and principal characteristics of the LTA vehicles are estimated and illustrated using physics, mathematics, and chemistry known to freshmen, the emphasis being on the application of this knowledge to aerospace engineering and design rather than on exposure to new science and mathematics.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
-	AHS007	I	Applied Physics	-

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIAExamination	Total Marks
Introduction to aerospace engineering	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✘	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Independently carry out research / investigation and development work to solve practical problems	1	Term Papers
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Lectures

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	2	Lectures

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Get the knowledge of technical areas of aerospace engineering including mechanics and physics of fluids, structures and materials, instrumentation, control and estimation, humans and automation, propulsion and energy conversion, aeronautical and astronautical systems
II	Understand the methodology and experience of analysis, modeling, and synthesis
III	Understand the evolution of human space exploration with a brief introduction to the missions conducted by various countries
IV	Knowledge in satellite engineering and the systems involved in the operation of satellites.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the theory, science and history behind the working of aircraft along with the foundation of aerodynamics and flight mechanics.	CLO 1	Understand the evolution of an aircraft and gain knowledge about the detailed history of aircraft.
		CLO 3	Gain knowledge about the anatomy of aircraft, helicopters, satellites and other air vehicles, and about the working importance of each component in an air vehicle
		CLO 6	Getting knowledge about the theory to produce a safe, effective, economic production of aircraft.
		CLO 12	Understand about the performance parameters, performance in steady flight, cruise, climb, range, endurance, accelerated flight symmetric maneuvers, turns, sideslips, takeoff and landing.
		CLO 13	Gain knowledge about the basic Aerodynamics, Flight mechanics and aircraft structures which are the foundation stones for knowledge based exams.
CO 2	Gain knowledge about terms and terminologies along with the principles of air transport and the working of space propulsion systems.	CLO 2	Develop one- self to gain knowledge about current technical term which helps to extend the outputs of research.
		CLO 5	Getting knowledge about different factors that effect generation of lift and practices that are in use for effective lift generation.
		CLO 7	Identify, solve new problems and gain new knowledge.
		CLO 9	Discuss the principle constituents of the transportation system involved in civil and commercial aircrafts and understanding the working of space propulsion systems.
		CLO 10	Understand different terminologies and technologies in the field of aerodynamics.
CO 3	Understand various working principles which will be the basics to gain knowledge sufficient to design new products.	CLO 4	Understand the theoretical knowledge behind the design and development of aircrafts.
		CLO 8	Choose a concept or idea of technical real time problems to form solutions for the same.
		CLO 11	Memorize procedure and steps to keep the products working effectively.

		CLO 16	Extend the outputs of earlier research and discover good ideas for new products or improving current products.
CO 4	Knowledge in space radiation and effect of radiation on space crafts and gain knowledge of different space missions.	CLO 14	Understand the impact of radiations in the outer space on the spacecrafts and satellites and safety precautions to be followed.
		CLO 15	Ability to summarize the efficiency of the design in achieving the mission goal and safety of flight.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BAE701.01	CLO 1	Understand the evolution of an aircraft and gain knowledge about the detailed history of aircraft.	PO 1	1
BAE701.02	CLO 2	Develop one- self to gain knowledge about current technical term which helps to extend the outputs of research.	PO 1	1
BAE701.03	CLO 3	Gain knowledge about the anatomy of aircraft, helicopters, satellites and other air vehicles, and about the working importance of each component in an air vehicle	PO 1	1
BAE701.04	CLO 4	Understand the theoretical knowledge behind the design and development of aircrafts.	PO 1	1
BAE701.05	CLO 5	Getting knowledge about different factors that effect generation of lift and practices that are in use for effective lift generation.	PO 1	1
BAE701.06	CLO 6	Getting knowledge about the theory to produce a safe, effective, economic production of aircraft.	PO 1	1
BAE701.07	CLO 7	Identify, solve new problems and gain new knowledge.	PO 1	1
BAE701.08	CLO 8	Choose a concept or idea of technical real time problems to form solutions for the same.	PO 5	2
BAE701.09	CLO 9	Discuss the principle constituents of the transportation system involved in civil and commercial aircrafts and understanding the working of space propulsion systems.	PO 5	2
BAE701.10	CLO 10	Understand different terminologies and technologies in the field of aerodynamics.	PO 5	2
BAE701.11	CLO 11	Memorize procedure and steps to keep the products working effectively.	PO 5	2
BAE701.12	CLO 12	Understand about the performance parameters, performance in steady flight, cruise, climb, range, endurance, accelerated flight symmetric maneuvers, turns, sideslips, takeoff and landing.	PO 5	2
BAE701.13	CLO 13	Gain knowledge about the basic Aerodynamics, Flight mechanics and aircraft structures which are the foundation stones for knowledge based exams.	PO 5	2
BAE701.14	CLO 14	Understand the impact of radiations in the outer space on the spacecrafts and satellites and safety precautions to be followed.	PO 7	2
BAE701.15	CLO 15	Ability to summarize the efficiency of the design in achieving the mission goal and safety of flight.	PO 7	2
BAE701.16	CLO 16	Extend the outputs of earlier research and discover good ideas for new products or improving current products.	PO 7	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	PO1	PO5	PO7
CLO 1	1		
CLO 2	1		
CLO 3	1		
CLO 4	1		
CLO 5	1		
CLO 6	1		
CLO 7	1		
CLO 8		2	
CLO 9		2	
CLO 10		2	
CLO 11		2	
CLO 12		2	
CLO 13		2	
CLO 14			2
CLO 15			2
CLO 16			2

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO 1	SEE Exams	PO 1	Seminars and Term Paper	PO 1
Student Viva	-	Mini Project	-	Laboratory Practices	-

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

UNIT-I	INTRODUCTION TO AERONAUTICS AND ASTRONAUTICS
Historical perspective of aeronautics and astronautics, anatomy of the airplane, anatomy of a space vehicle, aerodynamic forces; Parameters affecting aerodynamic forces: Dimensional analysis; Theory	

and experiment, wind tunnels; Atmosphere: Properties of U.S. standard atmosphere, definitions of altitude.

UNIT- II	ONE DIMENSIONAL FLOW IN INCOMPRESSIBLE AND COMPRESSIBLE FLUIDS, TWO DIMENSIONAL FLOW AND FINITE WING

Continuity equation, Bernoulli's equation; Application of Bernoulli's equation: Airspeed indicators and wind tunnels, one dimensional compressible flow concepts, speed of sound, compressible flow equations in a variable-area stream tube, application to airspeed measurement, applications to channels and wind tunnels; Two dimensional flow and finite wing: Limitations of one dimensional flow equations; Theory of lift: circulation, Airfoil pressure distribution, Helmholtz vortex theorems, Simulating the wing with a vortex Line, downwash, elliptic lift distribution; Lift and drag: Momentum and energy, Slope of finite wing lift curve, verification of Prandtl wing theory, additional effects of wing vortices, search for reduced induced drag.

UNIT-III	VISCOUS EFFECTS, DRAG DETERMINATION, AIRFOILS, WINGS AND HIGH-LIFT SYSTEMS

Boundary layer, boundary layer on bluff bodies, creation of circulation, laminar and turbulent boundary layers: skin friction, nature of Reynolds number, effect of turbulent boundary layer on separation; Total Incompressible drag: Parasite drag, drag due to lift, importance of aspect ratio; Compressibility drag: Prediction of drag divergence Mach number, sweptback wings, total drag.

Supersonic flow: Shock waves and Mach waves, supersonic wing lift and drag, area rule, supersonic aircraft, airfoils; Wings: early airfoil development, modern airfoils, supersonic airfoils, airfoil pitching moments, effects of sweepback on lift, airfoil characteristics, airfoil selection and wing design; High-lift Devices: Airfoil maximum lift coefficient, leading and trailing edge devices, effect of sweepback, deep stall, effect of Reynolds number, propulsive lift.

UNIT-IV	AIRPLANE PERFORMANCE, STABILITY AND CONTROL, AEROSPACE PROPULSION

Level flight performance, climb performance, range, endurance, energy-state approach to airplane performance, takeoff performance, landing performance; Static longitudinal stability; Dynamic longitudinal stability; Dynamic lateral stability; Control and maneuverability: Turning performance, control systems, active controls; Aerospace propulsion: Piston engines, gas turbines; Speed limitations of gas turbines: Ramjets, propellers, overall propulsion efficiency, rocket engines, rocket motor performance, propulsion-airframe integration.

UNIT-V	AIRCRAFT STRUCTURES, HYPERSONIC FLOWS, ROCKET TRAJECTORIES AND ORBITS

Aircraft structures: Importance of structural weight and integrity, development of aircraft structures, importance of fatigue, materials, loads, weight estimation; Hypersonic flows: temperature effects, Newtonian theory; rocket trajectories, multistage rockets, escape velocity, circular orbital or satellite velocity, elliptical orbits, orbital maneuvers.

Text Books:

1. Richard S. Shevell, "Fundamentals of Flight", Pearson Education Publication, 2nd Edition,1988.
2. Anderson J. D, "Introduction to Flight", McGraw-Hill, 5th Edition,1989.
3. Newman D, "Interactive Aerospace Engineering and Design", McGraw-Hill, 1st Edition,2002.
4. Barnard R.H and Philpot. D.R, "Aircraft Flight", Pearson Education, 3rd Edition,2004.

Reference Books:

1. John D. Anderson, Jr., "Introduction to Flight", Tata McGraw-Hill Publishing Company, 5thEdition,2007.
2. Kermode, A. C, "Flight without Formulae", McGraw Hill, 4th Edition,1997.
3. Swatton P.J, "Flight Planning", Blackwell Publisher, 6th Edition,2002.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Historical perspective of aeronautics and astronautics, anatomy of the airplane, anatomy of a space vehicle, aerodynamic forces	CLO 1	T1:1.7 T2:1-3
2	Parameters affecting aerodynamic forces	CLO 2	T1:1.13 T2:1-4
3	Dimensional analysis; Theory and experiment, wind tunnels	CLO 1	T1:1.11 T2:1-3
4	Atmosphere: Properties of U.S. standard atmosphere	CLO 1	T1:5.6 T2:2-5
5	Definitions of altitude.	CLO 2	T1:3.2 T2:2-4
6	Continuity equation, Bernoulli's equation	CLO 3	T1:2.1 T2:1-8
7	Application of Bernoulli's equation	CLO 1	T1:2.5 T2:1-8
8	Airspeed indicators and wind tunnels, one dimensional compressible flow concepts	CLO 4	T1:3.6 T2:2-6
9-10	Speed of sound, compressible flow equations in a variable-area stream tube,	CLO 5	T1:5.3 T2:2-6
11	Application to airspeed measurement, applications to channels and wind tunnels	CLO 6	T1:6.3 T2:6-1
12	Two dimensional flow and finite wing	CLO 6	T1:6.4 T2:6-4
13-14	Limitations of one dimensional flow equations	CLO 7	T1:6.5 T2:6-5
15-16	Theory of lift: circulation, Airfoil pressure distribution	CLO 7	T1:6.11 T2:6-6
17-19	Helmholtz vortex theorems, Simulating the wing with a vortex Line	CLO 9	T1:6.9 T2:7-2
20-22	Downwash, elliptic lift distribution	CLO 12	T1:11.2 T2:12-2
23-24	Momentum and energy, Slope of finite wing lift curve	CLO 11	T1:9.2 T2:3-4
24-25	Verification of Prandtl wing theory	CLO 11	T1:9.4 T2:3-4
26	Additional effects of wing vortices search for reduced induceddrag. Boundary layer, boundary layer on bluff bodies	CLO 10	T1:9.5 T2:1-3
27-28	Creation of circulation, laminar and turbulent boundary layers, Specific and Universal Gas Constants	CLO 10	T1:9.5 T2:1-3
29-30	Effect of turbulent boundary layer on separation, Total Incompressible drag: Parasite drag, drag due to lift, importance of aspect ratio	CLO 02	T1:9.6
31-32	Compressibility drag, Prediction of drag divergence Mach number sweptback wings, totaldrag.	CLO 10	T1:10.2 T2:13-1
33	Supersonic flow: Shock waves and Mach waves, supersonic wing lift and drag, area rule, supersonic aircraft, airfoils;	CLO 10	T1:10.3 T2:13-1
34-35	Wings: early airfoil development, modern airfoils, supersonic airfoils, airfoil pitching moments, effects of sweepback on lift, airfoil characteristics	CLO 10	T1:10.5 T2:13-2
36	Airfoil selection and wing design; High-lift Devices: Airfoil maximum lift coefficient, leading and trailing edge devices	CLO 11	T1:10.6 T2:13-3

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
37-39	effect of sweepback, deep stall, effect of Reynolds number, propulsivelift.	CLO 11	T1:10.4
40-41	Level flight performance, climb performance, range, endurance, energy-state approach to airplane performance, takeoff performance, landing performance	CLO 10	T1:10.8 T2:13-3
42	Static longitudinal stability; Dynamic longitudinal stability; Dynamic lateral stabilityControl and maneuverability: Turning performance, control systems, active controls; Aerospace propulsion	CLO 10	T1:10.8 T2:13-2
43-44	Piston engines, gas turbines; Speed limitations of gas turbines: Ramjets, propellers, overall propulsion efficiency, rocket engines, rocket motor performance, propulsion-airframeintegration.	CLO 10	T1:10.8 T2:13-2
45-46	Aircraft structures: Importance of structural weight and integrity	CLO 11	T1:10.7 T2:13-3
47	development of aircraft structures	CLO 10	T1:10.9 T2:13-1
48-49	importance of fatigue, materials, loads	CLO 08	T1:10.9 T2:13-2
50-51	weight estimation	CLO 13	T1:15.1 T2:14-1
52	Hypersonic flows: temperature effects,	CLO 12	T1:15.2 T2:14-2
53	Newtonian theory	CLO 12	T1:15.2 T2:14-4
54	rocket trajectories, multistage rockets	CLO 13	T1:15.3
55-56	escape velocity	CLO 14	T1:13.6 T2:9-5
57	circular orbital or satellite velocity	CLO 14	T1:13.6 T2:9-6
58	elliptical orbits	CLO 14	T1:13.8 T2:9-5
59-60	orbital maneuvers	CLO 14	T1:13.8 T2:9-6

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S NO	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POs	RELEVANCE WITH PSOs
1	Gain information about lift augmentation devices and control surfaces	Seminars / Guest Lectures / NPTEL	PO 1, PO 3	PSO 4

Prepared By:
Mr. R Sabari Vihar, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED PRORAMMING LABORATORY**			
Course Code	BES101			
Programme	M.Tech (ES)			
Semester	I	ECE		
Course Type	Core			
Regulation	IARE - R16			
	Lectures	**Tutorials**	**Practical**	**Credits**
	-	-	3	2
Course Faculty	Mr. S Lakshmanachari, Assistant Professor			

I. COURSE OVERVIEW:

This course provides knowledge of embedded C programming language. This covers the concepts for reading data from port pins of microcontroller, understanding the interfacing of data I/O devices, serial communication, and port on P89V51RD2 microcontroller. Through laboratory experiments and out-of-class assignments, students are provided learning experiences that enable them to provide in-depth knowledge about embedded processor, its hardware and software, explain programming concepts and embedded programming in C and assembly language and explain real time operating systems, inter-task communication and an embedded software development tool.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	--	I	Microprocessors and Microcontrollers Laboratory	--

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIAExamination	Total Marks
Embedded Programming Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	CHALK & TALK	✔	VIVA	✘	ASSIGNMENTS	✘	MOOCs
✔	LCD / PPT	✘	SEMINARS	✔	MINI PROJECT	✘	VIDEOS
✘	OPEN ENDED EXPERIMENTS						

V. EVALUATION METHODOLOGY:

Ccontinuous internal assessment (CIA):

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, with 20 marks for day to day evaluation and 10 marks for Internal Examination (CIE).

Semester End Examination (SEE):

The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the this courses is contains 12 experiments. The question paper pattern is as follows: Two full questions with 'either' 'or' choice will be drawn from each set. Each set contains 4 questions.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 10 marks for Continuous Internal Examination (CIE), 20 marks for Day to Day Evaluation.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Day to Day Evaluation	
CIA Marks	10	20	30

Continuous Internal Examination (CIE):

Two CIE exam shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration consisting of two sets.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, and storage technology	3	Lab related Exercises
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Lab related Exercises / Mini projects
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	1	Lab related Exercises
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	2	Lab related Exercises
PO 6	Independently carry out research / investigation and development work to solve practical problems	2	Lab related Exercises

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Use embedded C for reading data from port pins
II	Understand the interfacing of data I/O devices with microcontroller.
III	Understand serial communication and port RTOS on microcontroller.

VIII. COURSEOUTCOMES (COs):

CO Code	CO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES101.01	CO 1	Ability to write the programs for LED blinking and to interface the devices like switch, buzzer and LCD with P89V51RD2.	PO 1, PO 3	2
BES101.02	CO 2	Ability to write the programs for interfacing of data I/O devices like seven segment display, keypad and RS232 with P89V51RD2.	PO 1, PO 2	3
BES101.03	CO 3	Ability to write the programs for interfacing stepper motor and temperature sensor.	PO 4	2
BES101.04	CO 4	Ability to understand real time operating systems, inter- task communication and analog to digital conversions.	PO 1, PO 3	2
BES101.05	CO 5	Ability to write the programs for interfacing digital to analog conversion and elevator.	PO 6	2

3= High; 2 = Medium; 1 = Low

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO 1	3		1				
CO 2	3	2					1
CO 3				2			
CO4	3		1				
CO5						2	

3= High; 2 = Medium; 1 = Low

X. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, PO 3, PO 4	SEE Exams	PO 1, PO 3, PO 4	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2, PO 3, PO 4, PO 6	Student Viva	PO 3, PO 6,	Mini Project	PO 2	Certification	-
Term Paper	-						

XI. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XII. SYLLABUS:

S No.	Experiment
1	Program to toggle all the bits of port P1 continuously with 250 ms delay.
2	Program to interface a switch and a buzzer to two different pins of a port such that the buzzer should sound as long as the switch is pressed.
3	Program to interface LCD data pins to port P1 and display a message on it.
4	Program to interface seven segment display.
5	Program to interface keypad. Whenever a key is pressed, it should be displayed on lcd.
6	Program to transmit message from microcontroller to PC serially using RS232. Program to receive a message from PC to microcontroller serially using RS232.
7	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
8	Program to read data from temperature sensor and display the temperature value.
9	Program Port RTOS on to 89V51 Microcontroller and verify. Run 2 to 3 tasks simultaneously on 89V51 SDK. Use LCD interface, LED interface, Serial communication.
10	Program to convert analog signal into digital (ADC).
11	Program to convert digital into analog (DAC).
12	Program to interface Elevator.

XIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Learning Objectives	Topics to be covered
1-3	Over view of Micro controller architecture.	Open the micro controller P89V51RD2 kit box and study the architecture.
4-6	Understand the LED toggling.	Program to toggle all the bits of port P1 continuously with 250 ms delay.
7-9	Understand the concepts of buzzer.	Program to interface a switch and a buzzer to two different pins of a port such that the buzzer should sound as long as the switch is pressed.
10-12	Understand the concept of LCD interfacing.	Program to interface LCD data pins to port P1 and display a message on it.
13-15	Understand seven segment display interface.	Program to interface seven segment display.
16-18	Understand the concept of keypad.	Program to interface keypad. Whenever a key is pressed, it should be displayed on lcd.
19-21	Understand the concept of serial communication.	Program to transmit message from microcontroller to PC serially using RS232. Program to receive a message from PC to microcontroller serially using RS232.
22-24	Understand the working principle of temperature sensor.	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
25-27	Understand the working principle of temperature sensor.	Program to read data from temperature sensor and display the temperature value.

28-30	Understand the concepts of RTOS.	Program Port RTOS on to 89V51ucontroller and verify. Run 2 to 3 tasks simultaneously on 89V51 SDK. Use LCD interface, LED interface, Serial communication.
31-33	Understand ADC and DAC.	Program to convert analog signal into digital (ADC) and digital into analog (DAC).
34-36	Understand interface of elevator.	Program to interface Elevator.

Prepared by:
Mr. S Lakshmanachari, Assistant Professor **HOD, ECE**

II SEMESTER

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED SYSTEM ARCHITECTURE**				
Course Code	**BES004**				
Programme	**M.Tech**				
Semester	**II**				
Course Type	**Core**				
Regulation	**IARE - R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Dr. M Ramesh Babu, Assistant Professor**				

I. COURSE OVERVIEW:

Embedded System Architecture(ESA) attempts to give a pragmatic process for creating an embedded systems architecture based upon some of the mechanisms that exist in the more complex industry approaches. ESA provides understanding and applying the requirements to derive feasible hardware and/or software solutions for a particular design can be accomplished. ESA provides outline tactics for each of the scenarios that can be used to bring about the desired system response.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES003	I	Computer Architecture	3

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded System Architecture	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminar and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 6	Independently carry out research / investigation and development work to solve practical problems.	2	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understanding the fundamentals of embedded systems design paradigms, architectures.
II	Interpret possibilities and challenges, both with respect to software and hardware.
III	Analyze a system both as whole and in the included parts, and how these parts interact in the functionality and properties of the system.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe differentEmbedded system models, ISA architecture models.	CLO 1	Describe different Embedded system models, embedded standards, block diagrams Embedded board using von Neuman model.
		CLO 2	Demonstrate EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models.
CO 2	Demonstrate Internal processor design: ALU, memory.	CLO 3	Understand Internal processor design: ALU, registers, control unit, clock management
		CLO 4	Identify different processor i/o, interrupts, processor buses, processor performance
CO 3	Distinguish different memory managements.	CLO 5	DistinguishROM, RAM, cache, auxiliary memory, memory management.
		CLO 6	Identify performance of Board buses: Arbitration and timing, PCI bus example, integrating bus with components.
CO 4	DescribeMiddleware and applications and layers.	CLO 7	UnderstandMiddleware and applications: PPP, IP middleware UDP, Java. Application layer: FTP client, SMTP, HTTP server and client.
		CLO 8	DescribeApplication layer: FTP client, SMTP, HTTP server and client.
CO 5	Design and development architectural patterns and reference models.	CLO 9	Design and development of architectural patterns and reference models.
		CLO 10	Creating the architectural structures and evaluating the architecture, debugging testing, and maintaining.

IX. COURSE LEARNING OUTCOMES(CLOs)

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES004.01	CLO 1	Understand the different Embedded system models, embedded standards, block diagrams Embedded board using von Neuman model.	PO 1	3
BES004.02	CLO 2	Identify different ISA architecture models, application specific ISA models and general purpose ISA models.	PO 1	2
BES004.03	CLO 3	Understand Internal processor design: ALU, registers, control unit, clock management.	PO 2	2
BES004.04	CLO 4	Distinguish different processor i/o, interrupts, processor buses, processor performance.	PO 2	2
BES004.05	CLO 5	UnderstandROM, RAM, cache, auxiliary memory, memory management.	PO 3	3

BES004.06	CLO 6	Identify performance of Board buses: Arbitration and timing, PCI bus example, integrating bus with components	PO 3	3
BES004.07	CLO 7	UnderstandMiddleware and applications: PPP, IP middleware UDP, Java	PO 6	1
BES004.08	CLO 8	DescribeApplication layer FTP client, SMTP, HTTP server and client	PO 6	1
BES004.09	CLO 9	Describe Design and development of architectural patterns and reference models	PO 1, PO 6	2
BES004.10	CLO 10	Creating the architectural structures and evaluating the architecture, debugging testing, and maintaining	PO 1, PO 6	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	2	1	1	1
CO 2		1	1	
CO 3	1			
CO 4	2		1	1
CO 5			3	1

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THEACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 6
CLO 1	3			
CLO 2	2			
CLO 3		2		
CLO 4		2		
CLO 5			2	
CLO 6			2	
CLO 7				1
CLO 8				1
CLO 9	3			2
CLO 10	3			2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO2, PO3,PO6	SEE Exams	PO1, PO2, PO3, PO6	Seminar and Term Paper	PO1, PO2, PO3, PO6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES –INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I
INTRODUCTION TO EMBEDDED SYSTEMS Embedded system model, embedded standards, block diagrams, powering the hardware: Embedded board using von Neuman model; EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models: Instruction level parallelism.
UNIT II
PROCESSOR HARDWARE Internal processor design: ALU, registers, control unit, clock, on chip memory, processor i/o, interrupts, processor buses, processor performance.
UNIT III
SUPPORT HARDWARE Board memory: ROM, RAM, cache , auxiliary memory, memory management, memory performance. Board buses: Arbitration and timing, PCI bus example, integrating bus with components, bus performance.
UNIT IV
SOFTWARE Middleware and applications: PPP, IP middleware UDP, Java. Application layer: FTP client, SMTP, HTTP server and client.
UNIT V
ENGINEERING ISSUES OF SOFTWARE Design and development: architectural patterns and reference models: Creating the architectural structures, documenting the architecture, analyzing and evaluating the architecture, debugging testing, and maintaining.
TEXT BOOKS:
3. Charles H. Roth Jr, Lizy Kurian ,Tammy Noergaard, "Embedded system architecture", Elsevier, 2006.
REFERENCES:
2. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", the publisher Paul Temme, 2011.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand the basic concepts of Embedded system model, embedded standards	Introduction: Embedded system model, embedded standards, block diagrams powering the hardware: Embedded board using von Neuman model	T1:1.1, 1.2
4-6	Describeoverall Embedded board using von Neuman model.	Powering the hardware: Embedded board using von Neuman model.	T1:2.1
7-9	Understand the differentISA architecture models	EMBEDDED processors: ISA architecture models, application specific ISA models	T1:2.2, 2.3

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
		and general purpose ISA models: Instruction level parallelism.	
10-13	Describe Internal processor design	Internal processor design: ALU, registers, control unit, clock	T1:4.1, 4.2, 4.3
14-16	Implementing the concepts of processor.	On chip memory, processor i/o, interrupts, processor buses, processor performance.	T1:4.2, 4.4
17-20	Understand the concepts of different memories.	Board memory: ROM, RAM, cache , auxiliary memory, memory management, memory performance.	T1: 5.1, 5.2
21-22	Describe the concepts of board buses.	Board buses: Arbitration and timing, PCI bus example, integrating bus with components, bus performance.	T1:6.1, 6.2, 6.4
23-27	Understand Middleware and applications.	Middleware and applications: PPP, IP middleware UDP, Java.	T1:7.2, 7.3, 7.4
28-36	DescribeApplication layer and different clients.	Application layer: FTP client, SMTP, HTTP server and client.	T1:8.1, 8.3
37-40	Understand design and development of architectural patterns	Design and development: architectural patterns and reference models: Creating the architectural structures	T1:5.3
41-45	Understanding the concept of architecture.	Documenting the architecture, analyzing and evaluating the architecture, debugging testing, and maintaining.	T1:5.5, 5.6, 5.7

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Embedded standards, block diagrams	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 6
2	Application layer: FTP client, SMTP	Work Shops/ Guest Lectures / NPTEL	PO 3, PO 6

Prepared By:
Dr. M Ramesh Babu, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**FPGA ARCHITECTURE AND APPLICATION**				
Course Code	**BES005**				
Programme	**M.Tech**				
Semester	**II**	**ECE**			
Course Type	**Core**				
Regulation	**IARE - R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Dr. K.Nehru, Associate Professor**				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of FPGA architectures and its requirements. Subsequently the course covers architectural design of CPLD architectures. As we progress with the course, students will be familiarized with the programming models as well as protocols which govern the sensor network and its applications in real world.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
FPGA Architecture And Application	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminar and Term Paper
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Guest Lectures
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	Seminars
PO 6	Independently carry out research/investigation and development work to solve practical problems.	2	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the architecture of various FPGA and CPLD
II	Design and implementation ASIC targeting to FPGA/CPLD
III	Understand different types of programming technologies and logic devices

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define the complex programmable logic device and its features using CPLD architectures.	CLO 1	Understanding the basic concept of logic devices, Familiarization to architecture of read only memories and logic arrays, design the programmable logic devices
		CLO 2	Study of complex programmable logic device and its features, design the parallel adder using CPLD architectures
		CLO 3	Examine the various function blocks in FPGA, List the programming technology and its features
CO 2	Describe programming of SRAM FPGA, Define the programming technology.	CLO 4	Discuss the various principles involved in the design of programmable logic blockArchitectures, Understand the needs of programmable interconnects
		CLO 5	Describe the functions of programmable I/O blocks in FPGA, Describe the programming of SRAM FPGA, Define the programming technology and Analyze device architecture
CO 3	Demonstrate knowledge and understanding of Xilinx XC4000 architecture; Describe the programming of antifuse FPGA.	CLO 6	Study the features of Xilinx XC2000 architecture Understand the concepts of Xilinx XC3000 architecture
		CLO 7	Study the features of Xilinx XC4000 architecture, Describe the programming of antifuse FPGA
		CLO 8	Define the programming technology and Analyze device architecture
CO 4	Collect data for ACTEL ACT2 architecture.	CLO 9	Study the features of ACTEL act1 architecture
		CLO 10	Understand the concepts of ACTEL ACT2 architecture
CO 5	Discuss about position tracking and analyze the features of DMA controller.	CLO 11	Study the features of ACTEL act3 architecture
		CLO 12	Study the design issues and design of counter
		CLO 13	Implement robot for position tracking and analyze the features of DMA controller
		CLO 14	Analyze the performance of counters using ACT devices, Design of data path units using ACT architecture

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BES005.01	CLO 1	Understanding the basicconcept of logic devices, Familiarization to architectureof read only memories andlogic arrays, design the programmable logicdevices	PO1, PO 3	3, 3
BES005.02	CLO 2	Study of complex programmablelogic device and its features, design the parallel adder usingCPLD architectures	PO 2, PO 4	2, 3
BES005.03	CLO 3	Examine the various functionblocks in FPGA, List the programmingtechnology and its features	PO 2, PO 4	2, 3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BES005.04	CLO 4	Discuss the various principlesinvolved in the design ofprogrammable logic block Architectures, Understand the needs ofprogrammable interconnects	PO 1, PO 4	3, 3
BES005.05	CLO 5	Describe the functions ofprogrammable I/O blocks inFPGA, Describe the programming ofSRAM FPGA, Define the programmingtechnology and Analyzedevice architecture	PO 2, PO 4	2, 3
BES005.06	CLO 6	Study the features of XilinxXC2000 architecture Understand the concepts ofXilinx XC3000 architecture	PO 2, PO 3	2, 3
BES005.07	CLO 7	Study the features of XilinxXC4000 architecture, Describe the programming ofantifuse FPGA	PO1	3
BES005.08	CLO 8	Define the programmingtechnology and Analyze devicearchitecture	PO 3	3
BES005.09	CLO 9	Study the features of ACTEL act1architecture	PO 3, PO 4	3, 3
BES005.10	CLO 10	Understand the concepts ofACTEL ACT2 architecture	PO 3, PO 4	3, 3
BES005.11	CLO 11	Study the features of ACTEL act3architecture	PO 1, PO 3	3, 3
BES005.12	CLO 12	Study the design issues anddesign of counter	PO 3	3
BES005.13	CLO 13	Implement robot for positiontracking and analyze the featuresof DMA controller	PO 6	2
BES005.14	CLO 14	Analyze the performance ofcounters using ACT devices, Design of data path units usingACT architecture	PO 1, PO 6	3, 2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 4	PO 6
CO 1	3	2	3	3	
CO 2	3	2		3	
CO 3	3	2	3		
CO 4			3	3	
CO 5	3		3		2

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO1	PO 2	PO 3	PO 4	PO 6
CLO 1	3		3		

CLO 2		2		3	
CLO 3		2		3	
CLO 4	3			3	
CLO 5		2		3	
CLO 6		2	3		
CLO 7	3				
CLO 8			3		
CLO 9			3	3	
CLO 10			3	3	
CLO 11	3		3		
CLO 12			3		
CLO 13					2
CLO 14	3				2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1,PO3 PO 4	SEE Exams	PO1,PO3 PO 6	Seminar and Term Paper	PO1, PO 2 PO 3, PO 4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

Unit-I	**INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES:**
Introduction, simple programmable logic devices: Read only memories; Programmable logic arrays, Programmable array logic, Programmable logic devices/Generic array logic; Complex programmable logic devices: Architecture of Xilinx cool runner XCR3064XL CPLD, CPLD implementation of a parallel adder with accumulation.	
Unit-II	**FIELD PROGRAMMABLE GATE ARRAYS:**
Organization of FPGAs, FPGA programming technologies and Programmable logic block architectures, programmable interconnects, programmable I/O blocks in FPGAs, dedicated specialized components of FPGAs and applications of FPGAs.	
Unit-III	**SRAM PROGRAMMABLE FPGAS:**
Introduction, programming technology, device architecture, the Xilinx XC2000, XC3000 and XC4000 architectures.	

Unit-IV	ANTIFUSE PROGRAMMED FPGAS:
Introduction, programming technology, device architecture, the Actel ACT1, ACT2 and ACT3 architectures.	
Unit-V	**DESIGN APPLICATIONS**
General design issues, counter examples, fast video controller and position tracker for a robot manipulator, fast DMA controller, designing counters with ACT devices, designing adders and accumulators with the ACT architecture.	
Text Books:	
3. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition, 1st Editon, 1994. 4. Charles H. Roth Jr, Lizy Kurian John, "Digital Systems Design", Cengage Learning, 2nd Edition, 2012.	
Reference Books:	
3. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India, 1st Edition, 2008. 4. Pak K. Chan/Samiha Mourad, "Digital Design Using Field Programmable Gate Arrays", Pearson LowPrice Edition, 1999. 5. Ian Grout, "Digital Systems Design with FPGAs and CPLDs, Elsevier, Newnes, 1st Edition, 2008. 6. Wayne Wolf, "FPGA based System Design", Prentice Hall, Modern Semiconductor Design Series, 2004.	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the basic concept of logic devices, Familiarization to architecture of read only memories and logic arrays, design the programmable logic devices	Introduction,simpleprogrammable logicdevices, Read only memories	T1:1.1 to 1.5 R1:3.1 to 3.5
4-6	Study of complex programmable logic device and its features, design the parallel adder using CPLD architectures	Programmable logic arrays, programmable logicdevices/Generic array logic	T1:2.1 to 2.6 R2:2.8 to 3.5
7-9	Examine the various function blocks in FPGA, List the programming technology and its features	Complex programmablelogic devices, architecture of Xilinx coolrunner XCR3064XL CPLD, CPLD implementation of aparallel adder withaccumulation	T1:4.1 to 4.9 R4:2.1 to 2.4
10-13	Discuss the various principles involved in the design of programmable logic block Architectures, Understand the needs of programmable interconnects	Organization of FPGAs, FPGA programmingtechnologies	T1:6.1 to 6.5 R4:7.1 to 7.7
14-16	Describe the functions of programmable I/O blocks in FPGA, Describe the programming of SRAM FPGA, Define the programming technology and Analyze device architecture	Programmable logic blockarchitectures	T2:5.1to 5.4 R5:4.1 to 4.8
17-20	Study the features of Xilinx XC2000 architecture Understand the concepts of Xilinx XC3000 architecture	Counters, timers, Programmableinterconnects	T1:2.8 R2:3.3 to 3.7
21-24	Study the features of Xilinx XC4000 architecture, Describe the programming of antifuse FPGA	Programmable I/O blocks, programmable I/O blocks in FPGAs	T1:3.7 to 3.8 R3: 2.7 to 2.9
25-28	Define the programming technology and Analyze device architecture	Introduction, programming technology, and device architecture	T1:4.1 to 4.9

Lecture No	Topic Outcomes	Topics to be covered	Reference
29-32	Study the features of ACTEL act1 architecture	Xilinx XC2000 architecture, Xilinx XC3000 architecture, Xilinx XC4000 architecture	T1:5.1 to 5.2 R1:3.1 to 3.5
32-36	Understand the concepts of ACTEL ACT2 architecture	General design issues, counter examples, fast video controller and position tracker for a robot manipulator	T1:5.3 to 5.5 R4:5.1 to 5.8
37-40	Implement robot for position tracking and analyze the features of DMA controller	Fast DMA controller, designing counters with ACT devices	T1:4.9 to 4.12 R3:8.1 to 8.5
41-45	Analyze the performance of counters using ACT devices, Design of data path units using ACT architecture	Designing adders and accumulators with the ACT architecture	T1:1.1 to 1.5 R1:3.1 to 3.5

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONAL REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Logic block architectures	Seminars / NPTEL	PO 1, PO 3, PO 4
2	Programming technology	Seminars / Guest Lectures / NPTEL	PO 3, PO 4
3	Needs of programmable interconnects	Laboratory Practices	PO 3, PO 6

Prepared By:
Dr. K Nehru, Associate Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTERNET OF THINGS (IoT)**			
Course Code	**BES006**			
Programme	**M.Tech (ES)**			
Semester	**II**			
Course Type	**Core**			
Regulation	**IARE - R16**			
Course Structure	**Theory**		**Practical**	
	Lectures	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**-**
Course Faculty	**Mr. B.Subbharayudu, Assistant Professor**			

I. COURSE OVERVIEW:

The Internet of Things is transforming our physical world into a complex and dynamic system of connected devices on an unprecedented scale. Advances in technology are making possible a more widespread adoption of IoT, from micro cameras to smart sensors that can asses crop conditions on a farm, to the smart home devices that are becoming increasingly popular.

The course covers the concepts of communication technologies, computer networks, cloud computing, and terms including the basic components of hardware and software. This course helps the students in gaining the knowledge about the sensor devices, different communication technologies like RFID, Bluetooth, and programming microcontroller for sending data to cloud. This course helps to undertake future courses that assume as a background in setting up cloud for different applications using IoT.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES201	I	Embedded System Architecture	3

III. MARKSDISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Internet of Things	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, storage technology.	3	Seminars, Lab session
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminar & Term paper

PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars , Lab session
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	Term paper
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	3	Term paper

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Learn the basic issues, policy and challenges in theInternet of Things.
II	Understand the components and the protocols inInternet of Things.
III	Understand the various modes of communications and build a small low cost embedded system with Internet of Things.
IV	Learn to manage the resources and deploy the resources into business.
V	Understand the cloud and internetenvironment.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define IOT and understand building blocks of Internet of things and characteristics.	CLO 1	Understand principles of Internet of Things(IoT).
		CLO 2	Understand the components of internet of things.
		CLO 3	Explain different communication technologies like RFID, Bluetooth, Zigbee, Wifi, Mobile internet etc.
CO 2	Understand the programming of microcontroller for IOT	CLO 4	Explain embedded communication software and software partitioning.
CO 3	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.	CLO 5	Discuss device and router management.
		CLO 6	Explain clustering and software agents.
		CLO 7	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.
CO 4	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.	CLO 8	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.
		CLO 9	Explain the internet of things in context of EURIDICE.
		CLO 10	Understand ontology and apply ontology engineering in the internet of things
CO 5	Able to realize the set upof Cloud environment and understand web enabling constrained devices.	CLO 11	Explain set up of cloud environment and sending data from microcontroller to cloud.
		CLO 12	Discuss case studies related to internet of things.
		CLO 13	Identify common approaches used for future developments of IoT.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES006.01	CLO 1	Understand principles of Internet of Things(IoT) .	PO 1	3
BES006.02	CLO 2	Understand the components of internet of things.	PO 1	3
BES006.03	CLO 3	Explain different communication technologies like RFID, Bluetooth, Zigbee, Wifi, Mobile internet etc.	PO 1, PO 3	3
BES006.04	CLO 4	Explain embedded communication software and software partitioning .	PO 1	3
BES006.05	CLO 5	Discuss device and router management.	PO 1, PO 2	2
BES006.06	CLO 6	Explain clustering and software agents.	PO 1, PO 2	2
BES006.07	CLO 7	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.	PO 1, PO 2	3
BES006.08	CLO 8	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.	PO 2, PO 3	3
BES006.09	CLO 9	Explain the internet of things in context of EURIDICE.	PO 2, PO 3	3
BES006.10	CLO 10	Understand ontology and apply ontology engineering in the internet of things	PO 3, PO 6	3
BES006.11	CLO 11	Explain set up of cloud environment and sending data from microcontroller to cloud.	PO 3, PO 6	2
BES006.12	CLO 12	Discuss case studies related to internet of things.	PO 6, PO 7	2
BES006.13	CLO 13	Identify common approaches used for future developments of IoT.	PO 6, PO 7	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CO 1	3		3		
CO 2	3				
CO 3	2	3			
CO 4		1	3	2	
CO 5			2	3	3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CLO 1	3				
CLO 2	3				
CLO 3	3		3		
CLO 4	3				
CLO 5	2	3			
CLO 6	2	3			
CLO 7	2	3			
CLO 8		2	3		
CLO 9		2	3		
CLO 10			3	3	
CLO 11			3	2	
CLO 12				2	3
CLO 13				2	3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1,PO3, PO5	SEE Exams	PO1,PO3, PO5, PO 6	Seminar and Term Paper	PO1, PO2, PO3, PO7
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I
INTRODUCTION Definition – phases – Foundations – Policy– Challenges and Issues - identification - security – privacy. Components in internet of things: Control Units – Sensors – Communication modules – Power Sources – Communication Technologies – RFID – Bluetooth – Zigbee – Wifi – Rflinks – Mobile Internet – Wired Communication.
UNIT II
PROGRAMMING THE MICROCONTROLLER FOR IOT Ecosystem, embedded communications software, software partitioning, module and task decomposition: Partitioning case study , protocol software, debugging protocols, tables and other data structures, table access routines, buffer and timer management, management software, device and router management: CLI based management and HTTP based management, agent to protocol

interface, device to manager communication, system setup, boot and post-boot configuration, saving and restoring the configuration
UNIT III
RESOURCE MANAGEMENT IN THE INTERNET OF THINGS Clustering - Software Agents - Data Synchronization - Clustering Principles in an Internet of Things Architecture - The Role of Context - Design Guidelines -Software Agents for Object. Data Synchronization- Types of Network Architectures - Fundamental Concepts of Agility and AutonomyEnabling Autonomy and Agility by the Internet of Things-Technical Requirements for Satisfying the New Demands in Production - The Evolution from the RFID-based EPCNetwork to an Agent basedInternet of Things- Agents for the Behaviour of Objects.
UNIT IV
BUSINESS MODELS FOR THE INTERNET OF THINGS The Meaning of DiY in the Network Society- Sensor-actuator Technologies and Middleware as a Basis for a DiY Service Creation Framework - Device Integration - MiddlewareTechnologies Needed for a DiY 36 | P a g e Internet of Things Semantic Interoperability as a Requirement for DiY Creation -Ontology- Value Creation in the Internet of Things-Application of Ontology Engineering in the Internet of Things-Semantic Web-Ontology - The Internet of Things in Context of EURIDICE - Business Impact.
UNIT V
FROM THE INTERNET OF THINGS TO THE WEB OF THINGS Resource-oriented Architecture and Best Practices- Designing REST ful Smart Things - Web-enabling Constrained Devices - The Future Web of Things - Set up cloud environment – send data from microcontroller to cloud – Case studies – Open Source e-Health sensor platform – Be Close Elderly monitoring – Other recent projects..
TEXT BOOKS:
4. Charalampos Doukas, "Building Internet of Things with the Arduino", Create space, April2002.
5. Dieter Uckelmann et.al, "Architecting the Internet of Things", Springer, 1st Edition, 2011.
REFERENCES:
1. Luigi Atzor et.al, "The Internet of Things: A survey, ", Journal on Networks,Elsevier Publications, October 2010.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Define IOT and understand the components of internet of things	Definition, phases, Foundations Policy, Challenges and issues, identification, security, privacy. Components in internet of things	T1:1.1, 1.5
4-6	DescribeCommunication modulesCommunication Technologies	Control units, sensors, communication modules, power sources, communication technologies	T1:2.7
7-9	Understand RFID, Bluetooth, Zigbee	RFID, Bluetooth, Zigbee, Wifi, Rflinks, mobile internet, wired communication.	T2:2.2, 2.3
10-13	Understand ecosystem and embedded communication software	Ecosystem, embedded communications software, software partitioning, module and task decomposition: Partitioning case study	T1:3.1, 3.2, 3.3
14-16	Define protocol software, debugging protocols, tables	Protocol software, debugging protocols, tables and other data structures, table access routines, buffer and timer management, management software	T1:4.2, 4.4
17-20	Understand the concepts of device and router management	Device and router management: CLI based management and HTTP based management, agent to protocol interface, device to manager communication, system setup, boot and post-boot configuration, saving and restoring the configuration	T2: 5.1, 5.2
21-22	Understand clustering software Agents and data synchronization	Clustering, software agents, data synchronization, clustering principles in an Internet of Things architecture, the role of context design guidelines, software agents for object	T2:6.1, 6.2, 6.4

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
23-27	Define Types of Network Architectures - Fundamental Concepts of Agility.	Data synchronization, types of network Architectures, fundamental concepts of agility and autonomy enabling by the Internet of Things, technical requirements for satisfying the new demands in production, the evolution from the RFID-based EPC Network to an agent basedInternet of Things, agents for the behaviour of objects.	T2:7.2, 7.3, 7.4
28-32	Understand the Meaning of DiY in the Network Society-Sensor-actuator Technologies	The meaning of DiY in the network society, Sensoractuator technologies and Middleware as a basis for a DiY service creation framework, Device Integration, MiddlewareTechnologies needed for a DiY	T1:8.1, 8.3
32-36	Understand application of Ontology Engineering in the Internet of Things	Interoperability as a requirement for DiY creation, Ontology, value creation in the Internet of Things, application of Ontology engineering in the Internet of Things, semantic web, Ontology, the Internet of Things in context of EURIDICE business impact.	T1:8.1, 8.3
37-40	Demonstrate resource-oriented Architecture	Resource oriented architecture and best practices designing REST full smart things, web enabling constrained devices	T1:8.6
41-45	Demonstrate Set up cloud environment – send data from microcontroller to cloud	The future web of things, set up cloud environment, send data from microcontroller to cloud, case studies, open source e-Health sensor platform, be close elderly monitoring, other recent projects..	T1:8.8, 8.9

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Real time implementation of simple modules using IoT.	Project	PO 2, PO 3, PO 6
2	Program modelling	Seminars / Guest Lectures / NPTEL	PO 1, PO 6, PO 7

Prepared By:
Mr. B Subbharayudu, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED WIRELESS SENSOR NETWORKS**				
Course Code	**BES210**				
Programme	**M.Tech**				
Semester	**II**	**ECE**			
Course Type	**Elective**				
Regulation	**IARE - R16**				
Course Structure	**Theory**		**Practical**		
	Lectures	**Tutorials**	**Practicals**	**Credits**	
	3	**-**	**-**	**3**	
Course Faculty	**S.Sherya Varma, Associate Professor**				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of wireless, embedded, internetworked sensor/actuator systems, an emerging technology that can provide visibility into and control over complex physical processes. Sensor net systems have applications to many societal-scale problems including health, safety, energy, and the environment. However, their design raises challenges across all areas of computer systems research, including platform architecture, power systems, operating systems, embedded databases, networking, data management, and machine learning. Many of these challenges stem from severe energy-constraints, deep physical embedding, volatile network connectivity, and small physical form factor, all of which present different design issues than traditional computing systems, and require a different design approach.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Wireless Sensor Networks	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	Guest Lectures
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	2	Guest Lectures

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the concepts of sensor networks to use in embedded wireless sensor networks.
II	Use sensor programming in wireless sensor networks.
III	Analyze wireless sensor networks for different applications.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define the hardware and other components, energy level of consumption of sensor nodes.	CLO 1	Understanding the basic concept of WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture
		CLO 2	Study of hardware components, energy consumption of sensor nodes
		CLO 3	Examine the various operating systems and execution environments, some examples of sensor nodes
CO 2	Describe various principles involved in the design of Sensor network scenarios.	CLO 4	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit
		CLO 5	Describe the functions of design principles for WSNs
CO 3	Demonstrate features of Sensor programming, introduction to tiny OS programming.	CLO 6	Study the features of service interfaces of WSNs, gateway concepts
		CLO 7	Study the features of Sensor programming, introduction to tiny OS programming
		CLO 8	Understand the fundamentals of programming sensors using nes C
CO 4	Collect functions of design principles for WSNs.	CLO 9	Study the features of Algorithms for WSN Techniques for protocol programming
		CLO 10	Understand the concepts of cooperating objects and sensor networks
CO 5	Discuss performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring.	CLO 11	Study the features of system architectures, Study the design issues and design of programming models
		CLO 12	Implement Wireless sensor networks for environmental monitoring
		CLO 13	Analyze the performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring
		CLO 14	Analyze the performance of Inter-vehicle communication networks

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BES210.01	CLO 1	Understanding the basic concept of WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture	PO 1, PO 2	3, 2
BES210.02	CLO 2	Study of hardware components, energy consumption of sensor nodes	PO 2	2
BES210.03	CLO 3	Examine the various operating systems and execution environments, some examples of sensor nodes	PO 3	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BES210.04	CLO 4	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit	PO 3, PO 4, PO 7	3, 3, 2
BES210.05	CLO 5	Describe the functions of design principles for WSNs	PO 2, PO 3, PO 7	2, 3, 2
BES210.06	CLO 6	Study the features of service interfaces of WSNs, gateway concepts	PO 4	3
BES210.07	CLO 7	Study the features of Sensor programming, introduction to tiny OS programming	PO 3	3
BES210.08	CLO 8	Understand the fundamentals of programming sensors using nes C	PO 1	3
BES210.09	CLO 9	Study the features of Algorithms for WSN Techniques for protocol programming	PO 1, PO 2, PO 7	3, 2, 2
BES210.10	CLO 10	Understand the concepts of cooperating objects and sensor networks	PO 1, PO 3 PO 7	3, 3, 2
BES210.11	CLO 11	Study the features of system architectures, Study the design issues and design of programming models	PO 1, PO 2, PO 7	3, 2, 2
BES210.12	CLO 12	Implement Wireless sensor networks for environmental monitoring	PO 2, PO 7	2, 2
BES210.13	CLO 13	Analyze the performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring	PO 4, PO 7	3, 2
BES210.14	CLO 14	Analyze the performance of Inter-vehicle communication networks	PO 2, PO 4, PO 7	2, 3, 2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 4	PO 7
CO 1	3	2	3		
CO 2		2	3	3	
CO 3	3		3	3	2
CO 4	3	2	3		2
CO 5	3	2		3	2

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 4	PO 7
CLO 1	3	2			
CLO 2		2			

CLO 3			3		
CLO 4			3	3	2
CLO 5		2	3		2
CLO 6				3	
CLO 7			3		
CLO 8	3				
CLO 9	3	2			2
CLO 10	3		3		2
CLO 11	3	2			2
CLO 12		2			2
CLO 13				3	2
CLO 14		2		3	2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 3 PO 4, PO 7	Seminar and Term Paper	PO 1, PO 2 PO 3, PO 4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

Unit-I	**INTRODUCTION TO WSN:**
Introduction to WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture, hardware components, energy consumption of sensor nodes, operating systems and execution environments, some examples of sensor nodes.	
Unit-II	**NETWORK ARCHITECTURE:**
Sensor network scenarios, optimization goals and figures of merit, design principles for WSNs, service interfaces of WSNs, gateway concepts.	
Unit-III	**SENSOR NETWORK IMPLEMENTATION:**
Sensor programming, introduction to tiny OS programming and fundamentals of programming sensors using nes C. Algorithms for WSN: Techniques for protocol programming.	
Unit-IV	**PROGRAMMING MODELS:**
An introduction to the concept of cooperating objects and sensor networks, system architectures and programming models.	

Unit-V	CASE STUDIES
Wireless sensor networks for environmental monitoring, wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.	
Text Books:	
1. Holger karl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley, 1st Edition, 2005. 2. Liljana Gavrilovska, Srdjan Krco, Veljko Milutinovic, Ivan Stojmenovic, Roman Trobec, "Application and Multidisciplinary Aspects of Wireless Sensor Networks", Springer, London Limited, 1st Edition, 2011.	
Reference Books:	
1. Michel Banatre, Pedro Jose Marron, Anibal Ollero, A. Dam Wolisz, "Cooperating Embedded Systems and Wireless Sensor Networks", John Wiley & Sons, 1st Edition, 2008. 2. Seetharaman Iyengar, Nandhan, "Fundamentals of Sensor Network Programming Applications and Technology", John Wiley & Sons, 1st Edition, 2008.	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the basic concept of WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture	Introduction to WSN, challenges for WSNs, characteristic requirements, required mechanisms	T1:2.3 to 2.7 R1: 1.5 to 1.8
4-6	Study of hardware components, energy consumption of sensor nodes	Single node architecture, hardware components	T1:4.1 to 4.8 R2: 2.7 to 2.8
7-9	Examine the various operating systems and execution environments, some examples of sensor nodes	energy consumption of sensor nodes, operating systems and execution environments, some examples of sensor nodes	T1:7.1 to 7.9 R1: 2.15 to 2.16
10-13	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit	Sensor network scenarios, optimization goals and figures of merit	T1:8.1 to 8.4 R1: 3.4 to 3.5
14-16	Describe the functions of design principles for WSNs	design principles for WSNs, service interfaces of WSNs, gateway concepts	T1:8.8 to 8.9 R1: 3.8 to 3.9
17-20	Study the features of service interfaces of WSNs, gateway concepts	Sensor programming, introduction to tiny OS programming and fundamentals of programming sensors using nes C	T2: 8.13 to 8.14 R1: 3.12 to 3.13
21-24	Study the features of Sensor programming, introduction to tiny OS programming	Algorithms for WSN: Techniques for protocol programming	T2: 9.4 to 9.6 R1: 4.5 to 4.7
25-28	Study the features of Algorithms for WSN Techniques for protocol programming	An introduction to the concept of cooperating objects and sensor networks	T2: 9.10 to 9.11 R1: 5.1 to 5.5
29-32	Understand the concepts of cooperating objects and sensor networks	system architectures and programming models	T2: 1.6 R1: 5.10 to 5.12
32-36	Study the features of system architectures, Study the design issues and design of programming models	Wireless sensor networks for environmental monitoring	T2: 1.9 R2: 2.1 to 2.3
37-40	Implement Wireless sensor networks for environmental monitoring	wireless sensor networks with mobile nodes	T2: 2.7 to 2.8 R2: 3.1 to 3.5
41-45	Analyze the performance of wireless sensor networks with	autonomous robotic teams for surveillance and monitoring, Inter-	T2: 4.5 to 4.6 R2: 5.8 to 5.9

Lecture No	Topic Outcomes	Topics to be covered	Reference
	mobile nodes, autonomous robotic teams for surveillance and monitoring	vehicle communication networks	

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Design of Sensor network scenarios	Seminars / NPTEL	PO 1, PO 3, PO 4
2	OS programming technology	Seminars / Guest Lectures / NPTEL	PO 2, PO 4, PO 7
3	Low-Power Networking Systems	Laboratory Practices	PO 3, PO 4

Prepared By:
Ms. S Sherya Varma, Associate Professor **HOD, ECE**

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED REAL TIME OPERATING SYSTEMS**				
Course Code	**BES214**				
Programme	**M. Tech**				
Semester	**II**				
Course Type	**Core**				
Regulation	**R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Mrs. N Anusha , Assistant Professor**				

I. COURSE OVERVIEW:

This course introduces some basic ideas of real time system design paradigms. Subsequently the course covers important concepts like scheduling in real time and challenges, both with respect to software and hardware. It also covers analysis of a system and programming tools and languages, to understand how the real time system design and fault tolerance techniques.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	-	-	Embedded systems	-

III. MARKS DISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Real time operating system	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	3	Seminar and Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	3	Seminar and Term paper
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	3	Seminar
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Seminar and Term paper
PO 6	Independently carry out research / investigation and development work to solve practical problems.	2	Seminar and Term paper

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the process of real-time system design
II	Use different scheduling algorithms for design of real time systems
III	Identify the tools and programming language for development of real time systems.
IV	Understanding the real time programming using case study.
V	Understand the process of real-time system design

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the concepts of various operating systems for embedded systems and describe the basic commands to perform operations on files.	CLO 1	Understand the basic UNIX/LINUX programming.
		CLO 2	Understand the overview of commands, file I/O process control.
		CLO 3	Understand the history of OS, RTOS, characteristics of RTOS
CO 2	Explore the structures, task services, states and other basic operations of the real time operating systems.	CLO 4	Understand the defining a task, task states, scheduling and synchronization.
		CLO 5	Understand the various components of the RTOS.
CO 3	Demonstrate the objects, services, I/Os and other building blocks of the real time operating systems.	CLO 6	Analyze the objects and services of the RTOS.
		CLO 7	Evaluate the Pipes, event registers, other building blocks, and component configuration.
		CLO 8	Understandthe device I/O management, Exceptions, interrupts and event handling.
CO 4	Explore exceptions, timers interrupts, service routines and other operations of the RTOS	CLO 9	Analyze the real time clocks, Programmable timers, timer interrupt service routines.
		CLO 10	Understand the basic concepts of RT Linux, Micro C/OS-II
CO 5	Develop knowledge and practical skills through case studies of various RTOS.	CLO 11	Understand the basic concepts of Vx works, embedded Linux, tiny OS
		CLO 12	Understand the basic concepts of android OS.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES214.01	CLO 1	Understanding the basic UNIX/LINUX programming.	PO 1	3
BES214.02	CLO 2	Understand the overview of commands, file I/Oprocess control.	PO 1	2
BES214.03	CLO 3	Understanding the basic f history of OS, defining RTOS, Scheduler, objects, services, characteristics of RTOS	PO 1, PO 2	2
BES214.04	CLO 4	Analyze the defining a task, task states and scheduling, task operations, structure, synchronization	PO 2	3
BES214.05	CLO 5	Analyze the communication and concurrency,defining semaphores, operations and use, defining message queue	PO 2	2

BES214.06	CLO 6	Understand the states, content, storage, operations and use.	PO 2, PO 3	3
BES214.07	CLO 7	Evaluate the Pipes, event registers, signals, other building blocks, component configuration.	PO 3	3
BES214.08	CLO 8	Evaluate the Basic I/O concepts, I/O subsystem. Exceptions, interrupts, applications, processing of exceptions and spurious interrupts	PO 3, PO 2	3
BES214.09	CLO 9	Analyze the real time clocks, programmable timers, timer interrupt service routines, soft timers, operations	PO 4	2
BES214.10	CLO 10	Understand the basic concepts of RT Linux, Micro C/OS-II	PO 4, PO 6	3
BES214.11	CLO 11	Understand the basic concepts of Vx works, embedded Linux, tiny OS	PO 6	3
BES214.12	CLO 12	Understand the basic concepts of basic concepts of android OS.PO	PO 6	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)				
	PO1	PO2	PO3	PO4	PO6
CO 1	3	3			
CO 2		3			
CO 3		2	3		
CO 4				3	2
CO 5					3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO1	PO2	PO3	PO4	PO6
CLO 1	3				
CLO 2	2				
CLO 3	2	2			
CLO 4		3			
CLO 5		2			
CLO 6		2	3		
CLO 7			3		
CLO 8		2	3		
CLO 9				2	

CLO 10				3	2
CLO 11					3
CLO 12					2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 2 PO 3, PO 4	Seminar and Term Paper	PO 2, PO 3
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT-I	**INTRODUCTION:**
Introduction to UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write), process control (fork, vfork, exit, wait, waitpid, exec).	
UNIT-II	**REAL TIME OPERATING SYSTEM:**
Brief history of OS, defining RTOS, Scheduler, objects, services, characteristics of RTOS, defining a task, task states and scheduling, task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue, states, content, storage, operations and use.	
UNIT-III	**OBJECTS,SERVICES AND INPUT OUTPUTS:**
Pipes, event registers, signals, other building blocks, component configuration. Basic I/O concepts, I/O subsystem.	
UNIT-IV	**EXCEPTIONS , INTERUPTS AND TIMERS:**
Exceptions, interrupts, applications, processing of exceptions and spurious interrupts, real time clocks, programmable timers, timer interrupt service routines, soft timers, operations.	
UNIT-V	**CASE STUDIES OF RTOS:**
RT Linux, Micro C/OS-II, Vx works, embedded linux, tiny OS and basic concepts of android OS.	
TEXT BOOKS:	
6. Quing Li, "Real Time Concepts for Embedded Systems",Elsevier,1st Edition,2011.	
REFERENCES:	
3. Rajkamal,"Embedded systems, Architecture, programming and Design" 'Tata McGraw Hill,2nd Edition, 2003.	
4. Richard steven, "Advanced UNIX Programming", Addision Wesley professional,3rd Edition 2013.	
5. Dr. Craig Hollabaugh , "Embedded Linux :Hardware, Software and Interfacing",Addision Wesely,1st Edition,2002.	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understand the basic concepts of operating system.	Introduction to real time system, issues task class performances	T1:1
4-5	Implementbasic scheduling algorithms of operating systems.	Real time application examples basics in algorithms	T1:1,5

Lecture No	Topic Outcomes	Topics to be covered	Reference
6-7	Describe the task scheduling of the specific application.	Application specific scheduling of independent task Internal process design Applications of each tasks	T1:1,5
8-9	Understand the history of the operating system.	Introduction to real time operating system history of OS,	T2:4
10-12	Implementing the concepts of task schedulers, services.	Defining RTOS, Scheduler, objects, services, characteristics of RTOS	T2:7,8
11-14	Understand the concepts of concurrency, various states of the task.	RTO defining a task states and scheduling, communication and concurrency,	T2:2,3
15-16	Understand the concepts of structure, synchronization of the task and communication.	task operationsstructure, synchronization	T2:5
17-18	Describe the managing of shared resources and task synchronization using semaphores.	Defining semaphores, operations and use	T1: 5, T2:3
19-21	Defining message queues, States, Content and typical message queue operations.	Defining message queue, states, content, storage, operations and use.	T2:10
22-24	Understand the unstructured data exchange and facilitate synchronization amongtasks using objects, event registers, pipes and other blocks of the real time embedded system.	Understanding the objects, service and I/O Pipes, event registers, signals, other building blocks	T2:11
25-26	Describing the I/O concepts tointeract with the outside world by moving data into and out of the system.	Component configuration. Basic I/O concepts, I/O subsystem.	T2:11
27-28	Defining exception handling and interrupts information for managing software and hardware events that occur,to avoid the failures, and improves the robustness of the software.	Exceptions, interrupts and timersapplications, processing of exceptions	T1,T2:96-97
29-30	Describing the RTC and timers to generate a periodic interrupt like timer tick, provide a baud rate clock to a UART. Implement real-time clock (RTC) functions in embedded systems with minimal design time, component count, and power	Spurious interrupts, real time clocks, timers	T2:170-86
31-32	Understand the portions of the ISR program thathandletheinterruptrequests, whenan Interrupt is triggered (either a hardware /software interrupt),	Timer interrupts service routines, soft timers, operations.	T2:1
33-34	Analysis the characteristics of various embedded real time operating systems	Case studies of ERTOS, RT linux, Micro C/OS-II.	T3:2
35-37	Understand the customizable real-time operating system (RTOS).,VxWorks designed for distributed computing on most central processing units.	Vx works, embedded linux	T3:5,6
38-40	Defining a component-based operating system and platform for low-power wireless devices, such as	Tiny OS and basic concepts of android OS	T3:164

Lecture No	Topic Outcomes	Topics to be covered	Reference
	those used in wireless sensor networks		

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Real Time Databases	Seminars / Guest Lectures / NPTEL	PO 4, PO 6
2	Fault Tolerance Techniques	Work Shops/ Guest Lectures / NPTEL	PO 4, PO 6

Prepared By:
Ms. N Anusha, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	Research Methodology				
Course Code	BCS703				
Programme	M.Tech (ES)				
Semester	II	ECE			
Course Type	ELECTIVE				
Regulation	IARE - R16				
Course Structure	Theory			Practical	
	Lectures	Tutorials	Credits	Laboratory	Credits
	3	-	3	-	-
Course Faculty	Dr. G Manisha, Assistant Professor				

I. COURSE OVERVIEW:

The course covers the identification of research problem and scientific approaches of research. This course helps the students to gain the knowledge on research design and overall research process is requirements for different types of researches and the data collection approaches and experimental setup for research. This course helps the students in identifying their research problem, plan of research, methodology, data collection, measuring errors and scalability of research. Topics include data visualizations, report writing standards and basics in intellectual property rights for their work. This course in reached to student by power point presentations, lecture notes, and lab involve the problem solving in mathematical and engineering areas.

II PRE-REQUISITE(S):

Level	Course Code	Semester	Prerequisites	Credits
-	-	-	-	-

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Research Methodology	70 Marks	30 Marks	100 Marks

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	3	CIE,SEE, Seminar
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminars

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars
PO 6	Independently carry out research / investigation and development work to solve practical problems.	2	Guest Lectures

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Identify an appropriate research problem in their interesting domain.
II	Organize and conduct research project.
III	Prepare a research project thesis report.
IV	Understand the law of patent and copyrights.
V	Adequate knowledge on process for filing Patent.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define the terms research and methodology.	CLO 1	Identify and understand the Research process and strength of research.
		CLO 2	Develop good research design with experimental work.
CO 2	Describe research approaches, techniques and strategies in the appropriate manner for decision making.	CLO 3	Design Error measurement and scaling parameters.
		CLO 4	Use various data forecasting techniques.
CO 3	Demonstrate knowledge and understanding of data analysis and interpretation in relation to the research process.	CLO 5	Understand the concept of regression analysis to find the hidden relations in data.
		CLO 6	Understand the professional attitude, ethics and excellence in engineering and science.
CO 4	Collect data for designs and methodologies to apply to a specific research project.	CLO 7	Understand the techniques of data interpretation and making effective research presentation.
		CLO 8	Analyze the Public debates on Scientific Issues.
CO 5	Discuss about patent laws and ownership rights.	CLO 9	Understand the fundamentals of copy rights laws.
		CLO 10	Understand the importance and process of patents and ownership rights.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BCS703.01	CLO 1	Identify and understand the Research process and strength of research.	PO 1	3
BCS703.02	CLO 2	Develop good research design with experimental work.	PO 1	2
BCS703.03	CLO 3	Design Error measurement and scaling parameters.	PO 2	2
BCS703.04	CLO 4	Use various data forecasting techniques.	PO 2	2

BCS703.05	CLO 5	Understand the concept of regression analysis to find the hidden relations in data.	PO 3	3
BCS703.06	CLO 6	Understand the professional attitude, ethics and excellence in engineering and science	PO 3	3
BCS703.07	CLO 7	Understand the techniques of data interpretation and making effective research presentation.	PO 6	1
BCS703.08	CLO 8	Analyze the Public debates on Scientific Issues.	PO 6	1
BCS703.09	CLO 9	Understand the fundamentals of copy rights laws.	PO1, PO 6	2
BCS703.10	CLO 10	Understand the importance and process of patents and ownership rights.	PO1, PO6	2

3= High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	2	1	1	1
CO 2		1	1	
CO 3	1			
CO 4	2		1	1
CO 5			3	1

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)			
	PO1	PO2	PO3	PO6
CLO 1	3			
CLO 2	2			
CLO 3		2		
CLO 4		2		
CLO 5			3	
CLO 6			3	
CLO 7				1
CLO 8				1

CLO 9	3			2
CLO 10	3			2

3= High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, P02, PO 3, PO 6	SEE Exams	PO 1, PO 2, PO 3, PO6	Seminar and Term Paper	PO 1, P02, PO 3, PO 6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT -I	**INTRODUCTION**
Definition, types of research, research approaches, research process, validity and reliability in research, features of good design, types of research design, and basic principles of experimental design.	
UNIT - II	**MEASUREMENT AND SCALING TECHNIQUES**
Errors in measurement, tests of sound measurement, scaling and scale construction techniques, forecasting techniques, time series analysis, interpolation and extrapolation.	
UNIT - III	**METHODS OF DATA COLLECTION**
Primary data, questionnaire and interviews, collection of secondary data, cases and schedules. Professional attitude and goals, concept of excellence, ethics in science and engineering, some famous frauds in science, case studies.	
UNIT - IV	**INTERPRETATION OF DATA AND REPORT WRITING**
Layout of a research paper, techniques of interpretation, making scientific presentation at conferences and popular lectures to semi technical audience, participating in public debates on scientific issues.	
UNIT - V	**INTRODUCTION TO INTELLECTUAL PROPERTY**
Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights; Law of copy rights: Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law; Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer.	
Text Books:	
1. C. R. Kothari, "Research Methodology: Methods and Techniques", New Age International Publishers, 2. P. Gupta, "Statistical Methods", Sultan Chand and Sons, New Delhi, 1st Edition, 2005. 3. Richard W. Stim, "Intellectual Property: Patents, Trademarks, and Copyrights", Cengage Learning, 2nd Edition, 2001.	
Reference Books:	
1. P. Narayana Reddy, G. V. R. K. Acharyulu, "Research Methodology and Statistical Tools", Excel Books, New Delhi, 1st Edition, 2008. 2. Prabuddha Ganguli, "Intellectual Property Right, Unleashing the Knowledge Economy", Tata Mc Graw Hill Publishing Company Ltd, 1st Edition, 2001.	

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Describe research approaches, techniques and strategies in the appropriate manner for decision making process.	Definition, types of research, research approaches, research process, validity and reliability.	T1:1
4-6	Describe the features of design, experimental design.	Features of good design, types of research design, and basic principles of experimental design.	T1:1.5
7-9	Understand the errors in measurement, scale construction techniques.	Errors in measurement, tests of sound measurement, scaling and scale construction techniques	T1:1.5
10-13	Evaluate the forecasting techniques and describe the interpolation and extrapolation.	Forecasting techniques, time series analysis, interpolation and extrapolation.	T2:4.1
14-16	Understand the requirement of primary data and secondary data.	Primary data, questionnaire and interviews, collection of secondary data, cases and schedules.	T2:7.8
17-20	Understand the professional attitude and goals, excellence.	Professional attitude and goals, concept of excellence, ethics in science and engineering, some famous frauds in science, case studies, models, validating models.	T2:2.3
21-24	Describe the research paper, public debates on scientific issues.	Layout of a research paper, techniques of interpretation, making scientific presentation at conferences and popular lectures to semi technical audience, participating in public debates on scientific issues.	T2:5.1
25-28	Identify the types of intellectual property.	Introduction, types of intellectual property, international organizations, agencies and treaties	T1: 5.3, T2:3.2
29-32	Understand the Importance of intellectual property rights.	Importance of intellectual property rights.	T2:10.2
32-36	Describe the Law of copy rights.	Law of copy rights: Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly.	T2:11
37-40	Describe the Copy right ownership issues.	Copy right ownership issues, copy right registration, notice of copy right, international copy right law.	T2:11
41-45	Understand the law of patents.	Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer.	T1:96-97

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs
1	Product development	Project/ Term Paper	PO 2, PO 3, PO 6
2	Research programs	Seminars / Guest Lectures / NPTEL	PO 2,PO 3

Prepared by:

Dr. G Manisha, Assistant Professor

HOD, ECE

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	EMBEDDED SYSTEM LABORATORY			
Course Code	BES102			
Programme	M.Tech (ES)			
Semester	II	ECE		
Course Type	Core			
Regulation	IARE - R16			
	Lectures	Tutorials	Practical	Credits
	-	-	3	2
Course Faculty	Mrs. S.Ranjatha, Assistant Professor			

I. COURSE OVERVIEW:

This course provides knowledge of Embedded System Lab. This covers the concepts for reading data from port pins of microcontroller, the interfacing of LED, KEYPAD and various motors to ARM7 (LPC2148). Along with this interfacing amplifiers, filters, converters, ALU operations and PSOC (CY8C29466, 24X1).

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES101	I	Embedded Programming Laboratory	2

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded System Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	CHALK & TALK	✔	VIVA	✘	ASSIGNMENTS	✘	MOOCs
✔	LCD / PPT	✘	SEMINARS	✔	MINI PROJECT	✘	VIDEOS
✘	OPEN ENDED EXPERIMENTS						

V. EVALUATION METHODOLOGY:

Continuous Internal Assessment (CIA):

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, with 20 marks for day to day evaluation and 10 marks for Internal Examination (CIE).

Semester End Examination (SEE):

The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the this courses is contains 12 experiments. The question paper pattern is as follows: Two full questions with 'either' 'or' choice will be drawn from each set. Each set contains 4 questions.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 10 marks for Continuous Internal Examination (CIE), 20 marks for Day to Day Evaluation.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Day to Day Evaluation	
CIA Marks	10	20	30

Continuous Internal Examination (CIE):

Two CIE exam shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration consisting of two sets.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded systems and sub areas IOT, processor technology, and storage technology	3	Lab related Exercises
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Lab related Exercises
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	3	Lab related Exercises
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Lab related Exercises
PO 6	Independently carry out research / investigation and development work to solve practical problems	3	Lab related Exercises
PO 7	Recognize the need to engage in lifelong learning through continuing education and research	2	Lab related Exercises

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Use embedded C for reading data from port pins.
II	Understand the interfacing of data I/O devices with microcontroller.
III	Understand serial communication

VIII. COURSE OUTCOMES (COs):

CO Code	CO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BES102.01	CO 1	Ability to write the programs for LED blinking and to interface the devices like LCD and KEYPAD with ARM7 (LPC2148).	PO1, PO3 PO6, PO7	2
BES102.02	CO 2	Ability to write the programs for interfacing of I/O devices like MOTORS,LED with ARM7 (LPC2148).	PO1, PO 3 PO4, PO6 PO7	3
BES102.03	CO 3	Ability to write the programs for interfacing programmable gain amplifier,study of various characteristics of Filters with PSOC (CY8C29466,24X1).	PO 1, PO2 PO 3, PO4 PO6, PO7	2
BES102.04	CO 4	Ability to write the programs for interfacingconverters, digital functions with PSOC (CY8C29466,24X1).	PO 1, PO 2 PO 3, PO 4 PO 6, PO7	3
BES102.05	CO 5	Ability to write the programs to do ALU operations and timing operations by interfacing PSOC (CY8C29466,24X1).	PO 1, PO 2 PO 3, PO 4 PO 6, PO7	3

3= High; 2 = Medium; 1 = Low

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO6	PO7
CO 1	3		2		2	2
CO 2	2		3	3	2	3
CO 3	3	2	2	3	2	2
CO 4	3	3	2	2	3	2
CO 5	3	2	3	2	3	2

3= High; 2 = Medium; 1 = Low

X. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, PO 3, PO 4	SEE Exams	PO 1, PO 3, PO 4	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2, PO 3,PO 6	Student Viva	PO 1, PO 2, PO 3, PO 4 , PO6	Mini Project	PO 6,PO 7	Certification	-
Term Paper	-						

XI. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XII. SYLLABUS:

S No.	Experiment
1	Program to toggle all the led to port and with some time delay.
2	Program to Interface LCD to ARM7 and display message on screen.
3	Program to Interface keypad with ARM7.
4	Program to Interface LED with ARM7.
5	Program to Stepper motor interfacing with ARM7.
6	Program to Interface DC motor with ARM7.
7	Program to implement Study and characterization of the Programmable Gain Amplifier (PGA): Gain bandwidth Product through PSOC.
8	Program to implement Low pass, High pass and Band pass filters and their characterization using PSOC.
9	Program to do Experiments with on-chip ADC's and DAC's using PSOC.
10	Program to implement Digital Function Implementation using Digital Blocks. a. Timer experiment b. Counter for blinking LED c. PWM experiment d. Digital buffer and digital inverter USING PSOC.
11	Program to implement Logical/Arithmetic functions using PSOC Microcontroller.
12	Program to implement Timer operation in different Modes using PSOC

XIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Learning Objectives	Topics to be covered
1-3	Over view of Micro controller architecture.	Open the micro controller kit box and study the architecture.
4-6	Understand the LED blinking.	Program to toggle all the led to port and with some time delay.
7-9	Understand the concepts of LCD.	Program to Interface LCD to ARM7 and display message on screen.
10-12	Understand the keypad structure.	Program to Interface keypad with ARM7.
13-15	Understand the design LED.	Program to Interface LED with ARM7.
16-18	Understand the design of stepper motor.	Program to Stepper motor interfacing with ARM7.
19-21	Understand the design of DC motor.	Program to Interface DC motor with ARM7.

22-24	Understand the characteristics of programmable gain amplifier.	Program to implement Study and characterization of the Programmable Gain Amplifier (PGA): Gain bandwidth Product through PSOC.
25-27	Understand the concepts of filters.	Program to implement Low pass, High pass and Band pass filters and their characterization using PSOC.
28-30	Understand the functionality ADC and DAC.	Program to do Experiments with on-chip ADC's and DAC's using PSOC.
31-33	Understand digital function implementation.	Program to implement Digital Function Implementation using Digital Blocks. a. Timer experiment b. Counter for blinking LED c. PWM experiment d. Digital buffer and digital inverter USING PSOC.
34-36	Understand ALU operation and timers.	Program to implement Logical/Arithmetic functions using PSOC Microcontroller.
37-39	Understand timer operation.	Program to implement Timer operation in different Modes using PSOC
40-42	Internal Lab Exam	CIE-I

Prepared by:
Ms. S.Ranjatha, Assistant Professor **HOD, ECE**