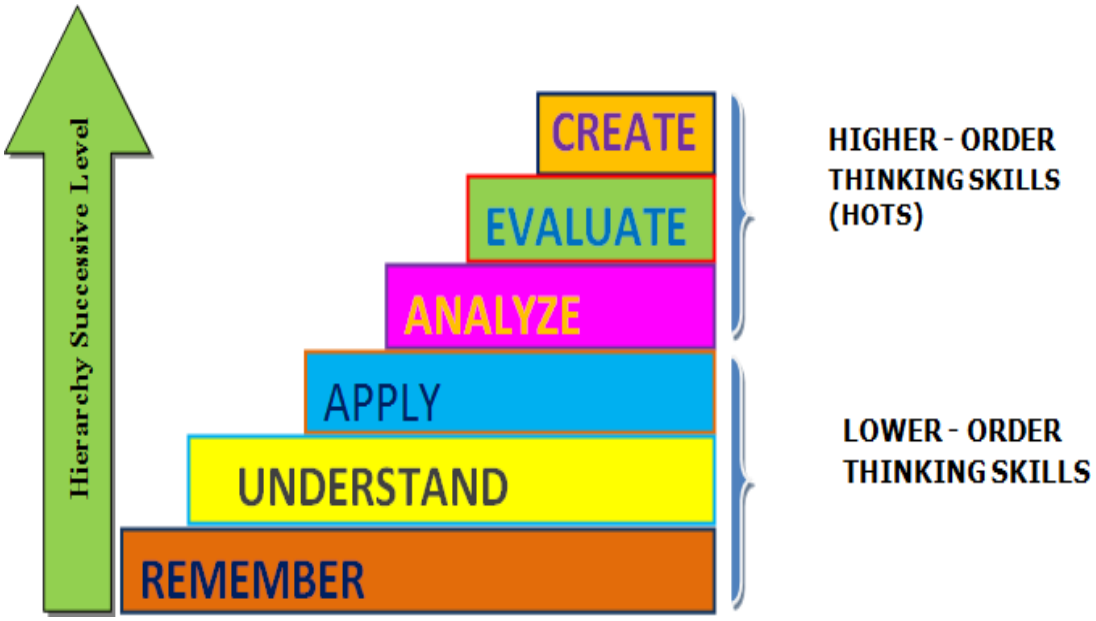
COURSE DESCRIPTOR BOOKLET

M.Tech(Embedded Systems)

ELECTRONICS AND COMMUNICATION ENGINEERING

(Accredited by NBA)

R-18 REGULATIONS



BLOOM'S TAXONOMY OF LEARNING OUTCOMES

.....Moving Towards Perfection in Engineering

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Approved by AICTE; Affiliated to JNTUH and Accredited by NAAC with 'A' Grade
Dundigal, Hyderabad - 500 043

Vision

To produce professionally competent Electronics and Communication Engineers capable of effectively and efficiently addressing the technical challenges with social responsibility.

Mission

The mission of the Department is to provide an academic environment that will ensure high quality education, training and research by keeping the students abreast of latest developments in the field of Electronics and Communication Engineering aimed at promoting employability, leadership qualities with humanity, ethics, research aptitude and team spirit.

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Program Education Objectives and Outcomes

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As Per NBA Norms Post June, 2016

Semester: I-I, I-II, II-I, II-II

Part – I

PROGRAM EDUCATIONAL OBJECTIVES AND OUTCOMES

First version 22 July, 2014

Program Educational Objectives, Program Outcomes and Assessment Criteria (Approved by DAC ECE on 3/9/2014):

Electronics and Communication Engineering Department Advisory Council: The Electronics and Communication Engineering Department Advisory Council (ECEDAC) includes a diverse group of experts from academic and industry, as well as alumni representation. The Advisory Board meets annually, or as needed, for a comprehensive review of the Electronics and Communication Engineering Department strategic planning and programs. The Advisory Council meets with administration, faculty and students and prepares a report, which is presented to principal. In each visit, the Department of Electronics and Communication Engineering responds to the report indicating improvements and amendments to the program.

1. PROGRAM EDUCATIONAL OBJECTIVES, OUTCOMES AND ASSESSMENT CRITERIA

Learning Outcomes, Assessment Criteria

The educational aims of a module are statements of the broad intentions of the teaching team. They indicate the objectives that the teaching team intends to cover and the learning opportunities that are necessary to be available to the student. A learning outcome is a statement that indicates the content that a learner (student) is expected to know, understand and/or be able to do at the end of a period of learning. It is advisable to express learning outcomes with the common prefix:

'On completion of (the period of learning e.g. module), the student is expected to be able to…'

Generally, learning outcomes do not specify curriculum, but more general areas of learning. It is not possible to prescribe precisely how specific a learning outcome statement should be. There is a balance to be struck between the degree of specificity in a learning outcome statement and that achieved by the assessment criteria. If there are too many learning outcomes for a module, then either they are becoming assessment criteria or they are specifying too much curricular detail. The curriculum should be described in the range statement. Too few learning outcomes are unlikely to provide sufficient information on the course. As a guide, there should be between 4 and 8 learning outcomes for a course.

The Program Educational Objectives (PEOs) of the Electronics and Communication Engineering department are broad statements or road maps describing career and professional objectives that intend the graduates to achieve through this program.

2. M. TECH – EMBEDDED SYSTEMS PROGRAM

EDUCATIONAL OBJECTIVES

A graduate of Institute of Aeronautical Engineering in Embedded systems discipline should have a successful career in Electronics and Communication Engineering or a related field, and within three to five years, should attain the following:

PROGRAM EDUCATIONAL OBJECTIVES:

PEO1. Research and development

Be successful practicing professionals or pursue doctoral studies in allied areas, contributing significantly to **research and development** activities

PEO2. Demonstrate

Demonstrate technical competence, such as identifying, formulating, analyzing, and creating engineering solutions using appropriate current embedded engineering techniques, skills, and tools.

PEO3. Communicate

To work and **communicate** effectively in inter-disciplinary environment, either in a team or independently and establish leadership qualities.

PEO4. Apply

An ability to **apply** in-depth knowledge to evaluate, analyze and synthesize existing and novel designs.

These objectives are quite broad by intention, as Electronics and Communication Engineering graduates may seek further education or work in diverse areas. To make these objectives meaningful, they may be demonstrated by performance, actions, or achievements.

i. To prepare the students who will be able to attain a solid foundation in Embedded systems fundamentals with an attitude to pursue continuing education.

- Make the students to understand their aptitude to choose the correct path of study which leads to higher qualifications and heights in the chosen field.
- Should be prepared to undergo rigorous training in their fields of working.
- Be capable of utilizing the solid foundation obtained at institute to apply successfully in solving the real time engineering problems.
- Students need to have creative thinking processes that are acquired through good training to find solutions to engineering problems.

ii. To prepare the students to function professionally in an increasingly international and rapidly changing world due to the advances in technologies and concepts and to contribute to the needs of the society.

- Adoptability and accommodative mind set to suit modern world and changing economies.
- By working hard in the chosen field and sharing the professional experience at different forums within and outside the country.
- Desirable to be a member of various professional societies (IEEE, IETE, ISTE, IE, and etc.) to keep yourself abreast with the state-of-the-art technology.
- Should continue additional education in a broad range of subjects other than engineering may be needed in order to meet professional challenges efficiently and effectively.
- Continuous interaction with educational and research institutions or industrial research labs.
- Have a sound foundation of knowledge within a chosen field and achieve good depth and experience of practice in it.
- Able to relate knowledge within chosen field to larger problems in society and able to appreciate the interaction between science, technology, and society.
- Strong grasp of quantitative reasoning and an ability to manage complexity and ambiguity.
- To conduct research, and design, develop, test and oversee the development of electronic systems for global upliftment.
- Applying scientific knowledge to solve technical problems and develop products and services that benefit the society.
- An electronic engineer shall contribute to the society by research, design and development, testing and evaluation, application by manufacturing, maintenance by service, management and other functions like sales, customer service and etc.

iii. To prepare the students to acquire and exercise excellent leadership qualities, at various levels appropriate to their experience, to address issues in a responsive, ethical, and innovative manner.

- Gives ample opportunity to work in diverse fields to acquire leadership roles in professional circles outside the workplace.
- Should keep in mind that the opportunities may change with the times.
- Should be prepared for creative solo and collaborative brainstorming sessions.
- Be able to inspire the team with selfless motivation and attitude to achieve success.
- Ability to think laterally or at-least have a flexibility of thought and make choices based on the requirement for situation.

iv. To prepare the students who will be able to excel, in their careers by being a part of success and growth of an organization, with which they are associated.

- To achieve this, the focus should not be limited to an engineering curriculum and even to the class room.
- Continuing professional education by attending short term in courses design to update engineering skills.
- A lifelong commitment to learning new and specialized information.
- Should accept first person responsibility and should take the initiative in carrying out the work.
- Should be determined for the duty and dedicated to work and have passion for that.

- Be delight at work with a positive attitude.
- Should be a detailed worker so that one can be relied by the organization.

The department of Electronics and Communication Engineering periodically reviews these objectives and as part of this review process, encourages comments from all interested parties including current students, alumni, prospective students, faculty those who hire or admit our graduates to other programs members of related professional organizations, and colleagues from other educational institutions.

3. M. TECH –EMBEDDED SYSTEMS PROGRAM OUTCOMES:

Masters of the embedded systems Program Outcomes will demonstrate:

PROGRAM OUTCOMES:

PO1. Engineering Knowledge

Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.

PO2. Teamwork and Project Management

Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.

PO3. Develop and Novel Designs

Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.

PO4. Analyze Complex Systems

Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.

PO5. Technical Presentation Skills

Write and present a substantial technical report / document.

PO6. Development of Solutions

Independently carry out research / investigation and development work to solve practical problems.

PO7. Lifelong learning

Recognize the need to engage in lifelong learning through continuing education and research.

4. MAPPING OF PROGRAM EDUCATIONAL OBJECTIVES TO PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES

The following Figure shows the correlation between the PEOs and the POs and PSOs

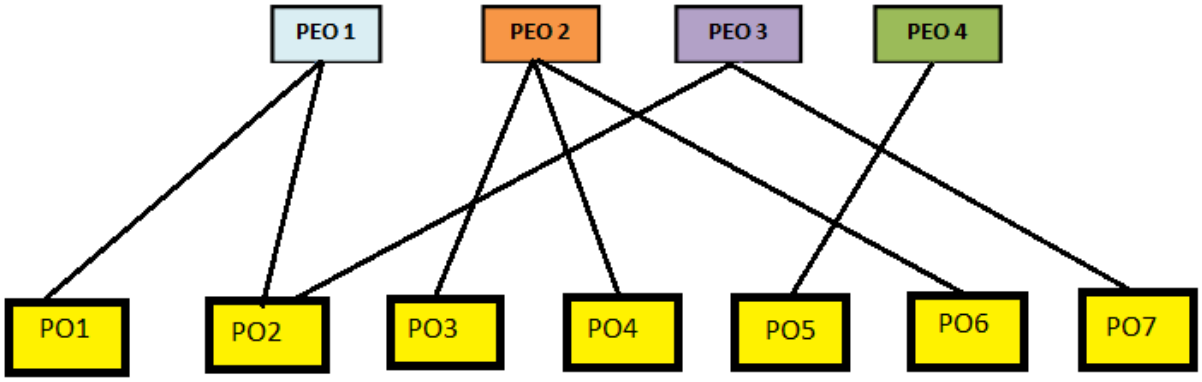

Figure: *Correlation between the PEOs and the POs*

The following Table shows the correlation between the Program Educational Objectives and the Program Outcomes & Program Specific Outcomes

	Program Educational Objectives		Program Outcomes
I	Be successful practicing professionals or pursue doctoral studies in allied areas, contributing significantly to **research and development** activities	**PO1**	**Engineering Knowledge** Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.
		PO2	**Teamwork and Project Management** Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
II	To be in a position to analyze real life problems and design socially accepted and economically feasible solutions in the respective fields.	**PO3**	**Develop and Novel Designs** Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.
		PO4	**Analyze Complex Systems** Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.
		PO6	**Development of Solutions** Independently carry out research / investigation and development work to solve practical problems.
III	To work and **communicate** effectively in inter-disciplinary environment, either independently or in a team, and establish	**PO2**	**Teamwork and Project Management** Function on multidisciplinary environments by working cooperatively, creatively and responsibly as

	leadership qualities.		a member of a team.
		PO7	**Lifelong learning** Recognize the need to engage in lifelong learning through continuing education and research.
IV	An ability to **apply** in-depth knowledge to evaluate, analyze and synthesize existing and novel designs.	**PO5**	**Technical Presentation Skills** Write and present a substantial technical report / document.

5. RELATION BETWEEN THE PROGRAM OUTCOMES AND PROGRAM EDUCATIONAL OBJECTIVES

A broad relation between the Program Educational Objectives and the Program Outcomes is given in the following table:

POs ↓ / PEOs →		(1) Research and development	(2) Demonstrate	(3) Communicate	(4) Apply
PO1	Engineering Knowledge	3			
PO2	Teamwork and Project Management	3		1	
PO3	Develop and Novel Designs		3		
PO4	Analyze Complex Systems		3		
PO5	Technical Presentation Skills				3
PO6	Development of Solutions		3		
PO7	Lifelong learning			3	

Relationship between Program Outcomes and Program Educational Objectives
Key: 3 = Highly Related; 1 = Low

6. PROGRAM OUTCOMES OF (M.Tech) EMBEDDED SYSTEMS MASTERS

Masters from accredited programs must achieve the following learning outcomes, defined by broad areas of learning.

The outcomes are distributed within and among the courses within our curriculum, and our students are assessed for the achievement of these outcomes, as well as specific course learning objectives, through testing, surveys, and other faculty assessment instruments. Information obtained in these assessments is used in a short-term feedback and improvement loop.

Each Electronics and Communication Engineering student will demonstrate the following attributes by the time they masters:

PO1. Engineering Knowledge

Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems

Performance Criteria Definitions

- Identify the concepts and/or equations
- Execute the solution using a logic and structured approach
- Evaluate the solution of the problem

PO2. Teamwork and Project Management

Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments

Performance Criteria Definitions

- Awareness of global effects of the product / practice /event
- Understanding of economic factors
- Awareness of implications to society at large

PO3. Develop Novel designs

Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations

Performance Criteria Definitions

- Use modern engineering tools for the system design, simulation and analysis
- Use software applications effectively to write technical reports and oral presentations
- Use modern equipment and instrumentation in the design process, analysis and troubleshooting

PO4. Analyze Complex Systems

Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions

Performance Criteria Definitions

- Identify problem/purpose
- Prepare hypothesis
- Outline procedure
- List materials and equipment
- Conduct experiment
- Record observations, data and results
- Perform analysis
- Document conclusions

PO5. Technical Presentation skills

Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

Performance Criteria Definitions

- Use appropriate format and grammatical structure
- Create a well organized document
- Present the results appropriately
- Demonstrate effective oral communication

PO6. Development of Solutions

Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations

Performance Criteria Definitions

- Awareness of global effects of the product / practice /event
- Understanding of economic factors
- Awareness of implications to society at large

PO7. Life-long Learning

Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

Performance Criteria Definitions

- Find relevant sources of information
- Participate in school or professional seminars
- Participate in students or professional associations

I SEMESTER

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED SYSTEM DESIGN**				
Course Code	**BESB01**				
Programme	**M.Tech**				
Semester	**I**				
Course Type	**Core**				
Regulation	**IARE - R18**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Mr. K.Ravi, Assistant Professor**				

I. COURSE OVERVIEW:

Embedded systems have become the next inevitable wave of technology, finding application in diverse fields of engineering. The goal of this course is to impart training to graduate engineers, in specialized area of Embedded Systems so that they can develop expertise in developing and deploying embedded systems over a wide range of applications. This course provides the basic knowledge over the hardware units and devices for design of embedded systems. It also provides the information about the Use architectures of embedded RISC processors and system on chip processor design of embedded systems. This course is intended to Analyze interrupt latency, context switching time, for development of device drives for timing devices.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC533	VI	Embedded C	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded System Design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IoT, Processor technology, storage technology.	3	Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Term paper and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	NPTEL Videos and Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	To introduce the difference between embedded systems and general purpose systems.
II	To optimize hardware designs of custom single-purpose processors.
III	To compare different approaches in optimizing general-purpose processors.
IV	To introduce different peripheral interfaces to embedded systems.
V	To understand the design tradeoffs made by different models of embedded systems.
VI	To apply knowledge gained in software-hardware integration in team-based projects

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the basic concepts of Embedded systems and its applications.	CLO 1	Understand the definition of Embedded system and classification.
		CLO 2	Analyze the history of Embedded Systems and its applications.
		CLO 3	Understand the characteristics and Quality Attributes of Embedded Systems.

COs	Course Outcome	CLOs	Course Learning Outcome
CO 2	Understand and analyze different processors in Embedded Systems	CLO 4	Describe general purpose and domain specific processors.
		CLO 5	Explain the concept of memory shadowing and memory selection for embedded systems.
		CLO 6	Distinguish between onboard and external communication interfaces.
CO 3	Describe about Embedded Firmware design approaches and development languages.	CLO 7	Describe importance of Real Time Clock and Watchdog Timer.
		CLO 8	Explain about Embedded firmware design approaches.
		CLO 9	Describe the importance of Embedded Firmware development Languages.
CO 4	Explain about Operating System basics, Multiprocessing and Multitasking.	CLO 10	Understand the importance of operating system basics and types of operating systems.
		CLO 11	Distinguish between Multiprocessing and Multitasking.
		CLO 12	Explain about the concept of task scheduling.
CO 5	Describe about synchronization issues and task synchronization techniques.	CLO 13	Describe about different Synchronization Issues.
		CLO 14	Analyze different task synchronization techniques.
		CLO 15	Understand the concept of how to choose an RTOS.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BESB01.01	CLO 1	Understand the definition of Embedded system and classification.	PO 1	2
BESB01.02	CLO 2	Analyze the history of Embedded Systems and its applications.	PO 1	2
BESB01.03	CLO 3	Understand the characteristics and Quality Attributes of Embedded Systems.	PO 1, PO 3	1
BESB01.04	CLO 4	Describe general purpose and domain specific processors.	PO 2, PO 3	3
BESB01.05	CLO 5	Explain the concept of memory shadowing and memory selection for embedded systems.	PO 1	3
BESB01.06	CLO 6	Distinguish between onboard and external communication interfaces.	PO 2	3
BESB01.07	CLO 7	Describe importance of Real Time Clock and Watchdog Timer.	PO 3	3
BESB01.08	CLO 8	Explain about Embedded firmware design approaches.	PO 1, PO 3	2
BESB01.09	CLO 9	Describe the importance of Embedded Firmware development Languages.	PO 3, PO 4	2
BESB01.10	CLO10	Understand the importance of operating system basics and types of operating systems.	PO 1, PO 4	3
BESB01.11	CLO 11	Distinguish between Multiprocessing and Multitasking.	PO 3	2

BESB01.12	CLO 12	Explain about the concept of task scheduling.	PO3, PO 4	3
BESB01.13	CLO 13	Describe about different Synchronization Issues.	PO 2	2
BESB01.14	CLO 14	Analyze different task synchronization techniques.	PO 3, PO 4	3
BESB01.15	CLO 15	Understand the concept of how to choose an RTOS.	PO 3, PO 4	2

3 = High; 2 = Medium; 1 = Low2

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes(PO)			
	PO 1	PO 2	PO 3	PO 4
CO 1	3		2	
CO 2	3	2	2	
CO 3	2		3	2
CO 4	2	2	2	2
CO 5		2	2	2

3 = High; 2 = Medium; 1 = Low2

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcome(PO)			
	PO 1	PO 2	PO 3	PO 4
CLO 1	3			
CLO 2	3			
CLO 3	3		3	
CLO 4		3	2	
CLO 5	2			
CLO 6		2		
CLO 7			3	
CLO 8	2		3	
CLO 9			3	3
CLO 10	3			3

CLO 11			2	
CLO 12			2	3
CLO 13		2		
CLO 14			2	3
CLO 15			2	2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT:

CIE Exams	PO1, PO2, PO3, PO 4	SEE Exams	PO1, PO2, PO3, PO 4	Seminar and Term Paper	PO1, PO2, PO3, PO4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES –INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

I Semester: ESD | PCC : CSE / SE / AE /(CAD /CAM) / PE/ST

Course code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
BES001	Core/Elective	3	-	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: Nil	Practical Classes: Nil			Total Classes: 45			

OBJECTIVES:

The course should enable the students to:

I. To introduce the difference between embedded systems and general purpose systems.
II. To optimize hardware designs of custom single-purpose processors.
III. To compare different approaches in optimizing general-purpose processors.
IV. To introduce different peripheral interfaces to embedded systems.
V. To understand the design tradeoffs made by different models of embedded systems.
VI. To apply knowledge gained in software-hardware integration in team-based projects.

UNIT-I	**INTRODUCTION TO EMBEDDED SYSTEMS:**	**Classes: 09**
Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.		
UNIT-II	**TYPICAL EMBEDDED SYSTEM:**	**Classes: 09**
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.		
UNIT-III	**EMBEDDED FIRMWARE**:	**Classes: 09**
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.		
UNIT-IV	**RTOS BASED EMBEDDED SYSTEM DESIGN:**	**Classes: 09**
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.		
UNIT-V	**TASK COMMUNICATION:**	**Classes: 09**
Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.		
Text Books:		
1. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.		
Reference Books:		
1. Embedded Systems - Raj Kamal, TMH. 2. Introduction to Embedded Systems - Shibu K.V, McGraw Hill. 3. Embedded Systems – Lyla, Pearson, 2013 4. An Embedded Software Primer - David E. Simon, Pearson Education.		

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand the definition of Embedded system and classification.	Definition of embedded system, embedded systems vs general computing systems.	T1: 5.1, 5.2, R1: 1.7
4-6	Analyze the history of Embedded Systems and its applications.	History of embedded systems, classification, major application areas.	T1:6.1,6.2, 6.3, T1: 6.4-6.6
7-9	Understand the characteristics	Purpose of embedded systems, characteristics and quality attributes of	T1:6.4-6.6, T1:6.7-6.8, 6.15 R2:7.1, 8.1

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
	and Quality Attributes of Embedded Systems.	embedded systems.	
10-12	Describe general purpose and domain specific processors.	Core of the embedded system: general purpose and domain specific processors.	T1:7.1, 7.4 T1:7.7, 7.8-7.10 R2:7.2
13-16	Explain the concept of memory shadowing and memory selection for embedded systems.	Basics, PLDs, commercial off-the-shelf components (cots), memory: ROM, RAM, memory according to the type of interface, memory shadowing, memory selection for embedded systems.	T1: 6.12, 9.4,9.6, R2: 4.2,
17-19	Distinguish between onboard and external communication interfaces.	Sensors and actuators, communication interface: onboard and external communication interfaces.	T1: 7.12,10.4, R2: 4.2, T1: 10.6
20-21	Describe importance of Real Time Clock and Watchdog Timer.	Reset circuit, brown-out protection circuit, oscillator unit, real time clock, watchdog timer,	T1: 10.5, T1: 8.1,8.2, 8.4,8.5,8.6 R2: 4.4
22-25	Explain about Embedded firmware design approaches.	Embedded firmware design approaches.	T1: 8.2,8.9 R2: 4.4,
26-30	Describe the importance of Embedded Firmware development Languages.	Embedded firmware development languages.	T1: 8.12, 8.13, 8.14
31-33	Understand the importance of operating system basics and types of operating systems.	Operating system basics, types of operating systems.	T1: 9.1, 9.2,9.3
34-36	Distinguish between Multiprocessing and Multitasking.	Tasks, process and threads, multiprocessing and multitasking.	R1:7.1,7.3 R1:7.4,7.7
37-39	Explain about the concept of task scheduling.	Task scheduling.	T1: 8.12, 8.13, 8.14
40-41	Describe about different Synchronization Issues.	Shared memory, message passing, remote procedure call and sockets, task synchronization: task communication/synchronization issues.	T1: 9.1, 9.2,9.3
42-44	Analyze different task synchronization techniques.	Task synchronization techniques	R1:7.1,7.3 R1:7.4,7.7
45	Understand the concept of how to choose an RTOS.	Device drivers, how to choose an RTOS.	T1: 9.1, 9.2,9.3

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY /PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Concepts of ERTOS	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 4

Prepared By:

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INSTITUTE OF AERONAUTICAL ENGINEERING

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Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING				
Course Code	BESB02				
Programme	M.Tech (ES)				
Semester	I	ECE			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Chief Coordinator	Dr. P Munaswami, Professor, ECE				
Course Faculty	Mr. V. Naresh Kumar, Assistant Professor, ECE				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of ARM Cortex-M3 Processor and LPC 17XX Microcontroller architectures and their features. Subsequently the course covers Programmable DSP Processor architecture. As we progress with the course students will be familiarized with the programming models of Microcontrollers and P-DSPs and their applications in real world.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microcontrollers And Programmable Digital Signal Processing	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✔	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make- examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weight age in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Technical Seminar and Term Paper	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Independently carry out research/investigation and development work to solve practical problems	2	Quiz
PO 3	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems.	2	Assignments
PO 6	Understand the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Seminars
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	2	Term paper

3= High; 2 = Medium; 1 = Low

VII COURSE OBJECTIVES:

The course should enable the students to:

I	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
II	Identify and characterize architecture of Programmable DSP Processors
III	Develop small applications by utilizing the ARM processor core and DSP processor based platform

VIII COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe different ARM processors, programming models, operations and interrupts.	CLO 1	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.
		CLO 2	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.
		CLO 3	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.
CO 2	Demonstrate various exceptions, interrupts, configurations, interrupt latency.	CLO 4	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions
		CLO 5	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.
		CLO 6	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.
CO 3	Describe the operation, feature of the LPC 17xx microcontroller.	CLO 7	Describe the LPC 17xx microcontroller- Internal memory, GPIOs, Timers.
		CLO 8	Study the features of ADC, UART and other serial interfaces.
		CLO 9	Understand the concepts of PWM, RTC, WDT.
CO 4	Describe the programmable DSP	CLO 10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.

COs	Course Outcome	CLOs	Course Learning Outcome
	processor and TI DSP processor.	CLO 11	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.
		CLO 12	Understand the Introduction to TI DSP processor family.
CO 5	Design and development architectural patterns and reference models.	CLO 13	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.
		CLO 14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.
		CLO 15	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB02.01	CLO 1	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.	PO1	3
BESB02.02	CLO 2	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.	PO1	2
BESB02.03	CLO 3	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.	PO3	2
BESB02.04	CLO 4	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions	PO1 PO6	2
BESB02.05	CLO 5	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.	PO1 PO7	2
BESB02.06	CLO 6	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	PO3	3
BESB02.07	CLO 7	Describe the LPC 17xx microcontroller-Internal memory, GPIOs, Timers.	PO7	3
BESB02.08	CLO 8	Study the features of ADC, UART and other serial interfaces.	PO1	2
BESB02.09	CLO 9	Understand the concepts of PWM, RTC, WDT.	PO3 PO6	2
BESB02.10	CLO 10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	PO1 PO7	2
BESB02.11	CLO 11	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.	PO1	2
BESB02.12	CLO 12	Understand the Introduction to TI DSP processor family.	PO6	2
BESB02.13	CLO 13	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.	PO1	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB02.14	CLO 14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.	PO3	3
BESB02.15	CLO 15	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.	PO1	2

3= High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 3	PO 6	PO 7
CO 1	3	2		
CO 2	2	3	2	2
CO 3	2	2	2	3
CO 4	2		2	2
CO 5	2	3		

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CLOs	POs			
	PO1	PO3	PO6	PO7
CLO 1	3			
CLO 2	2			
CLO 3		2		
CLO 4	2		2	
CLO 5	2			2
CLO 6		3		
CLO 7				3
CLO 8	2			
CLO 9		2	2	
CLO 10	2			2
CLO 11	2			
CLO 12			2	
CLO 13	2			
CLO 14		3		
CLO 15	2			

3= High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES–DIRECT:

CIE Exams	PO 1, PO 3 PO 6, PO 7	SEE Exams	PO 1, PO 3 PO 6, PO 7	Assignments	PO 3	Seminars	PO 6
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 6						

XIII. ASSESSMENT METHODOLOGIES–INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

MODULE -I	**SYSTEMS ARM CORTEX-M3 PROCESSOR**	**Classes: 09**
ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.		
MODULE - II	**EXCEPTIONS AND INTERRUPT**	**Classes: 09**
Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.		
MODULE - III	**LPC 17XX MICROCONTROLLER**	**Classes: 09**
LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.		
MODULE - IV	**PROGRAMMABLE DSP (P-DSP) PROCESSORS**	**Classes: 09**
Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.		
MODULE - V	**VLIW ARCHITECTURE**	**Classes: 09**
VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking.		
Text Books:		
1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition. 2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition.		
Reference Books:		
1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication 2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education 3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley 4. Technical references and user manuals on www.arm.com, NXP Semiconductor		

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.	ARM Cortex-M3 processor: Applications Programming model – Registers Operation modes, Exceptions and Interrupt, Reset Sequence	T1: 1.1, 1.5,2.2 2.3, 3.7
4-7	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.	Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes Permissions, Bit-Band Operations	T1: 4.1 5.2,5.5
8- 11	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.	Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces	T1: 6.1
12-17	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions	Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions	T1: 7.1, 7.2 7.4,7.5
18-20	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.	Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller	T2: 7.6,8.1
21-22	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	Basic Configuration, SYSTICK Timer, Interrupt Sequences Exits, Tail Chaining, Interrupt Latency	T1: 8.2, 8.5 9.1,9.2, 9.7
23-27	Describe the LPC 17xx microcontroller-Internal memory, GPIOs, Timers.	LPC17xx microcontroller-Internal memory, GPIOs, Timers.	R4: 8.4,8.10,8.21
28-32	Study the features of ADC, UART and other serial interfaces	ADC, UART, Other serial interfaces	R4: 8.14, 8.16,8.17
33-35	Understand the concepts of PWM, RTC, WDT.	PWM,RTC, WDT	R4: 8.228.28,8.27
36-39	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	Programmable DSP Processors ,Harvard architecture Multi-port memory Multi-port memory	T2: 2.1 2.2,2.4
40-42	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.	Architectural structure of P-DSP,Architectural structure of P-DSP,MAC unit, Barrel shifters	T2: 3.1,2.1,10.7
43-46	Understand the Introduction to TI DSP processor family.	Introduction to TI DSP processor family	T2: 2.5
47-49	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.	VLIW architecture and TMS320C6000 series Architecture study, data paths, cross paths	T2: 2.5,13.4
50-52	Understand the Introduction to Instruction level architecture of C6000 family, Assembly	Introduction to Instruction level architecture of C6000	T2: 13.3 13.6,13.5

Lecture No.	Topic Outcomes	Topics to be covered	Reference
	Instructions memory addressing, for arithmetic, logical operations.	family Assembly Instructions memory addressing, Arithmetic, logical operations	
53-55	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.	Code Composer Studio Code Composer Studio for application development for digital signal processing on chip peripherals Processor benchmarking	T2:13.11, 2.8,14.12

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs
1	Design examples of ARM Cortex-M3 processor.	Project	PO 1, PO 3, PO 7
2	Program modelling	Seminars / Guest Lectures / NPTEL	PO 1,PO 3, PO 6
3	Case studies of different DSP applications.	Seminars / Guest Lectures / NPTEL	PO 1, PO 3,PO 6

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**PRINCIPLES OF DISTRIBUTED EMBEDDED SYSTEMS**			
Course Code	**BES205**			
Programme	**M.Tech**			
Semester	**I**	**ECE**		
Course Type	**Elective**			
Regulation	**R16**			
Course Structure	**Theory**		**Practical**	
	Lectures	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**3**
Course Faculty	**Dr. S China Venkateswarlu, Professor, ECE**			

I. COURSE OVERVIEW:

Principles of Distributed Embedded Systems course is the environment of real-time computer systems. In a hard real-time application, analysis of the real-time system market is carried out with emphasis on the field of embedded real-time systems.

An embedded real-time system is a part of a self-contained product, a television set or an automobile. Embedded real-time systems will form the most important market segment for real-time technology. It focuses on the real-time aspects of operating systems.

A real-time operating system must provide a predictable service to the application tasks such that the temporal properties of the complete software in a node can be statically analyzed. Many dynamic mechanisms, such as dynamic task creation or virtual memory management, which are standard in workstation operating systems, interfere with this predictability requirement of real-time systems. These absolute timestamps are used to reason about the precision and accuracy of a global time base, and to expose the fundamental limits of time measurement in a distributed real-time system the idea of a sparse time base is introduced to establish a consistent view of the order of computer-generated events in a distributed real-time system. Some fundamental conflicts in the design of real-time protocols are highlighted.

The requirement for flexibility is in conflict with many other desirable protocol properties, such as comparability, error detection, and replica determinism. These conflicts have lead to the design of many different real-time protocols that try to bridge the gap between these conflicting requirements. Some of these protocols, such as the CAN (Control Area Network) system aspects of distributed real-time applications, treating the issues of real-time, distribution, This cross fertilization between the academic world and the industrial world has led to the inclusion of many insightful examples from the industrial world to explain the fundamental scientific concepts in a real-world setting. The emerging field of embedded automotive electronics that is acting as a catalyst for technology in the current real-time systems market.

This Course can be used by professionals in the industry, the relevance of the latest scientific insights to the solution of everyday problems in the design and implementation of distributed and embedded real-time systems. The recent appearance of cost-effective powerful system chips has a momentous influence on the architecture and economics of future distributed system solutions.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Principles of Distributed Embedded Systems	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each module carries equal weight age in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Technical Seminar and Term Paper	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the design principles of distributed embedded systems.
II	Design CAN network based systems.
III	Understand RTOS to design embedded system

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understanding the basic concept of Real time systems, Internal and external clock synchronization, real time model, Real time communication, rate constrains and time triggered.	CLO 1	Understanding the basic concept of Real time computer system requirements, global time, external clock synchronization.
		CLO 2	Study of real time model, real time communication, temporal relations and dependability.
		CLO 3	Examine the power and energy awareness, real time systems, event trigger, time trigger and rate constrained.
CO 2	Examine the real time operating systems, inter component communication, task management and dual role of time , inter task interactions, agreement protocols and error detection	CLO 4	Discuss the real time operating systems; inter component communication, task management and dual role of time.
		CLO 5	Describe the Inter task interactions, process input/output agreement protocol and error detection.
CO 3	Describe the System design, static and dynamic scheduling and system design, validation and time-triggered architecture.	CLO 6	Study the system design, scheduling problem and static and dynamic scheduling.
		CLO 7	Study the system design, validation.
		CLO 8	Describe the time-triggered architecture.
CO 4	Study the CAN, CAN open, CAN open standards, object directory, electronic data sheet and devices.	CLO 9	Understand CAN, CAN open Standards and object directory.
		CLO 10	Understand the electronic data sheet and devices.

CO 5	Analyze CAN standards, configuration files, service data objectives; network management CAN open messages and device profile encoder.	CLO 11	Study the configuration files, service data objectives.
		CLO 12	Understand network management CAN open messages.
		CLO 13	Analyze the device profile encoder.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BES205.01	CLO 1	Understanding the basic concept of Real time computer system requirements, global time, external clock synchronization.	PO 1 PO 2	2
BES205.02	CLO 2	Study of real time model, real time communication, temporal relations and dependability.	PO 2	2
BES205.03	CLO 3	Examine the power and energy awareness, real time systems, event trigger, time trigger and rate constrained.	PO 3	3
BES205.04	CLO 4	Discuss the real time operating systems; inter component communication, task management and dual role of time.	PO 3 PO 4	3
BES205.05	CLO 5	Describe the Inter task interactions, process input/output agreement protocol and error detection.	PO 2 PO 3	2
BES205.06	CLO 6	Study the system design, scheduling problem and static and dynamic scheduling.	PO 4	3
BES205.07	CLO 7	Study the system design, validation.	PO 3	3
BES205.08	CLO 8	Describe the time-triggered architecture.	PO 1	3
BES205.09	CLO 9	Understand CAN, CAN open Standards and object directory.	PO 1 PO 2	2
BES205.10	CLO 10	Understand the electronic data sheet and devices.	PO 1 PO 3	3
BES205.11	CLO 11	Study the configuration files, service data objectives.	PO 1 PO 2	2
BES205.12	CLO 12	Understand network management CAN open messages.	PO 2	2
BES205.13	CLO 13	Analyze the device profile encoder.	PO 4	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 4
CO 1	3	2	3	
CO 2	3	2	3	3
CO 3	3		3	3

CO 4	3	2	3	
CO 5	3	2		3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 4
CLO 1	3	2		
CLO 2		2		
CLO 3			3	
CLO 4			3	
CLO 5		2	3	
CLO 6		2	3	
CLO 7			3	
CLO 8	3			
CLO 9	3	2		
CLO 10	3		3	
CLO 11	3	2		
CLO 12		2		
CLO 13				3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 3 PO 4	Seminar and Term Paper	PO 1, PO 2 PO 3, PO 4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

Unit-I	REAL-TIME ENVIRONMENT :
Real-time computer system requirements, classification of real time systems, simplicity, global time, internal and external clock synchronization, real time model. Real time communication, temporal relations, dependability, power and energy awareness, real time communication, event triggered, rate constrained, time triggered.	

Unit-II	REAL-TIME OPERATING SYSTEMS :
Inter component communication, task management and dual role of time; Inter task interactions, process input/output, agreement protocols, error detection.	
Unit-III	**SYSTEM DESIGN :**
Scheduling problem, static and dynamic scheduling, system design. Validation, time-triggered architecture.	
Unit-IV	**INTRODUCTION TO CAN:**
Introduction to CAN open CAN open standard, object directory, electronic data sheets and devices.	
Unit-V	**CAN STANDARDS:**
Configuration files, service data objectives, network management CAN open messages, device profile encoder	

Text Books:

1. Hermann Kopetz, "Real–Time systems-Design Principles for distributed Embedded Applications", Springer, 2nd Edition, 2011.
2. Glaf P. Feiffer, Andrew Ayre and Christian Keyold, "Embedded networking with CAN and CAN open", Copperhill Media Corporation, 1st Edition, 2008.

Reference Books:

1. Rajkamal, 'Embedded system-Architecture-Programming-Design", Tata Mc Graw Hill, 3rd Edition, 2011.
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley and sons, 2nd Edition, 2002.
3. Lyla B Das, "Embedded Systems-An Integrated Approach", Pearson,1st Edition, 2013.
4. David E. Simon, "An Embedded Software Primer", Pearson Education, 1st Edition, 1999.

Web References:

1. https://www.youtube.com/watch?v=Uk9zFrEGguM
2. https://freevideolectures.com/blog/2010/11/130-nptel-iit-online-courses/

E-Text Books:

1. http://esd.cs.ucr.edu/
2. http://dsp-book.narod.ru/ESDUA.pdf
3. www.intel.com/education/highered/Embedded/Syllabus/Embedded_syllabus.pdf
4. www. dmi.uib.es/~jproenza/SistEncTR/Introduction.pdf

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the Real-time computer system requirements, classification of real time systems	Real-time computer system requirements, classification of real time systems	T1:1.1 to 1.7
4-6	Introduction to global time, internal and external clock synchronization, real time model.	Introduction to global time, internal and external clock synchronization, real time model.	T1:3.1 to 3.5
7-9	Examine the Real time communication, temporal relations, dependability	Real time communication, temporal relations, dependability	T1:7.1 to 7.7
10-13	Discuss the real time communication, event triggered, rate constrained, time triggered.	Real time communication, event triggered, rate constrained, time triggered.	T1:7.1 to 7.7 T1:8.1 to 8.5
14-16	Describe the Real-Time Operating Systems , Inter component communication, task management and dual role of time	Real-Time Operating Systems , Inter component communication, task management and dual role of time	T1:10.1 to 10.5

Lecture No	Topic Outcomes	Topics to be covered	Reference
17-20	Study the Inter task interactions, process input/output, agreement protocols, error detection.	Inter task interactions, process input/output, agreement protocols, and error detection.	T1:9.1 to 9.6 T1:10.1 to 10.5
21-24	Study the System Design, Scheduling problem, static and dynamic scheduling	System Design, Scheduling problem, static and dynamic scheduling	T1:13.1 to 13.6
25-28	Understand system design. Validation, time-triggered architecture.	System design. Validation, time-triggered architecture.	T1:13.1 to 13.6
29-32	Understand the CAN, Introduction to CAN open CAN open standard	CAN, Introduction to CAN open CAN open standard	R1: 245-309
33-36	Study the object directory, electronic data sheets and devices.	Object directory, electronic data sheets and devices.	R1: 40-93
37-40	Analyze CAN Standards Configuration files, service data objectives.	CAN Standards Configuration files, service data objectives.	R1: 40-93
41-45	Analyze the network management CAN open messages, device profile encoder	network management CAN open messages, device profile encoder	R1: 40-93

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Design of Sensor network scenarios	Seminars / NPTEL	PO 1, PO 3, PO 4
2	OS programming technology	Seminars / Guest Lectures / NPTEL	PO 3, PO 4
3	Low-Power Networking Systems	Laboratory Practices	PO 3, PO 4

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**WIRELESS LANS AND PANS**				
Course Code	**BESB03**				
Programme	M.Tech				
Semester	I				
Course Type	Elective				
Regulation	IARE - R18				
Course Structure	Theory			Practical	
	Lectures	Tutorials	Credits	Laboratory	Credits
	3	-	3	-	-
Course Faculty	Mr. M.Lakshmi Raviteja, Assistant Professor				

I. COURSE OVERVIEW:

Embedded systems have become the next inevitable wave of technology, finding application in diverse fields of engineering. The goal of this course is to impart training to graduate engineers, in specialized area of Embedded Systems so that they can develop expertise in developing and deploying embedded systems over a wide range of applications. This course provides the basic knowledge over the hardware units and devices for design of embedded systems. It also provides the information about the Use architectures of embedded RISC processors and system on chip processor design of embedded systems. This course is intended to Analyze interrupt latency, context switching time, for development of device drives for timing devices.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC524	VI	Wireless Communication and Networks	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Wireless LANs and PANs	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	)pen Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IoT, Processor technology, storage technology.	3	Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Term paper and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	NPTEL Videos and Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand different WLAN topologies and transmission techniques.
II	Interpret Bluetooth and Zigbee technologies.
III	Enhance the understanding of 3G systems and 4G networks.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe first and second generation cellular systems and analyze cellular communications from 1G to 3G.	CLO 1	Understand and analyze first and second generation cellular systems.
		CLO 2	Analyze cellular communications from 1G to 3G.
		CLO 3	Explain wireless 4G systems, and wireless spectrum.
CO 2	Understand and analyze WLAN topologies and analyze transmission techniques.	CLO 4	Describe carrier sense multiple access (CSMA), carrier sense multiple access with collision detection (CSMA/CD), carrier sense multiple access with collision avoidance (CSMA/CA).
		CLO 5	Explain WLAN topologies and analyze transmission techniques
		CLO 6	Distinguish random access methods.

COs	Course Outcome	CLOs	Course Learning Outcome
CO 3	Demonstrate network architecture and analyze MAC layer issues and describe the importance of MAC layer applications.	CLO 7	Describe importance of MAC layer applications
		CLO 8	Explain network architecture and analyze MAC layer issues.
CO 4	Explore Bluetooth technology and Bluetooth specifications, describe the importance of wireless private area networks.	CLO 9	Describe the importance of wireless private area networks.
		CLO 10	Explain Bluetooth technology and Bluetooth specifications.
		CLO 11	Analyze Enhancements to Bluetooth technology and applications
CO 5	Develop practical skills in the use of ZigBee components and network topologies.	CLO 12	Describe IEEE 802.15.3, The IEEE 802.15.4
		CLO 13	Understand ZigBee components and network topologies.
		CLO 14	Analyze Device architecture and network topologies

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES002.01	CLO 1	Understand and Analyze First and Second Generation Cellular Systems.	PO 1	2
BES002.02	CLO 2	Analyze Cellular Communications from 1G to 3G.	PO 1, PO 2	2
BES002.03	CLO 3	Explain Wireless 4G systems, The Wireless Spectrum.	PO 1, PO 3	1
BES002.04	CLO 4	Describe Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).	PO 2, PO 3	3
BES002.05	CLO 5	Explain WLAN Topologies and Analyze Transmission Techniques	PO 1	3
BES002.06	CLO 6	Distinguish Random Access Methods.	PO 1	3
BES002.07	CLO 7	Describe importance of Wireless Local Area Networks.	PO 3	3
BES002.08	CLO 8	Explain Network Architecture and Analyze MAC Layer issues.	PO 1, PO 3	2
BES002.09	CLO 9	Describe importance of Wireless Private Area Networks.	PO 3, PO 6	2
BES002.10	CLO10	Explain Bluetooth technology and Bluetooth specifications.	PO 1, PO 6	3
BES002.11	CLO 11	Analyze Enhancements to Bluetooth technology and applications	PO 2	2
BES002.12	CLO 12	Describe IEEE 802.15.3, The IEEE 802.15.4	PO 2, PO 6	3
BES002.13	CLO 13	Understand ZigBee components and network topologies.	PO 2	2
BES002.14	CLO 14	Analyze Device architecture and network topologies	PO 3, PO 6	3

3 = High; 2 = Medium; 1 = Low2

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes(PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	3	2	2	
CO 2	3	3	3	
CO 3	2		3	
CO 4	3	2	3	2
CO 5		2	3	3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcome(PO)			
	PO 1	PO 2	PO 3	PO 6
CLO 1	3			
CLO 2	3	2		
CLO 3	3		3	
CLO 4		3	2	
CLO 5	2			
CLO 6	2			
CLO 7			3	
CLO 8	2		3	
CLO 9			3	3
CLO 10	3			3
CLO 11		2		
CLO 12		2		3
CLO 13		2		
CLO 14			2	3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT:

CIE Exams	PO1, PO2, PO3, PO 6	SEE Exams	PO1, PO2, PO3, PO 6	Seminar and Term Paper	PO1, PO2, PO3, PO6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES –INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT -I	WIRELESS SYSTEM&RANDOM ACCESS PROTOCOLS	Classes: 08
Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).		

UNIT – II	WIRELESS LANS	Classes: 10
Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology.		

UNIT – III	THE IEEE 802.11 STANDARD FOR WIRELESS LANS	Classes: 08
Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol.		

UNIT - IV	WIRELESS PANS	Classes: 10
Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatter net formation.		

UNIT -V	THE IEEE 802.15 WORKING GROUP FOR WPANS	Classes: 09
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband..		

TEXT BOOKS:
1. Carlos de Morais Cordeiro, Dharma Prakash Agrawal, "AdHoc and Sensor Networks", World Scientific, 2011. 2. Vijay K.Garg, "Wireless Communications and Networking", Morgan Kaufmann Publishers, 2009.
REFERENCES:
1. Kaveh Pahlaram, Prashant Krishnamurthy, "Wireless Networks", PHI, 2002. 2. Marks Ciampor, Jeorge Olenewa, "Wireless Communication", Cengage Learning, 2007.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand and analyze first and second generation cellular systems.	Introduction, first and second generation cellular systems, Cellular communications from 1G to3G Wireless 4G systems, The wireless Spectrum	T1: 5.1, 5.2, R1: 1.7
4-6	Analyze Cellular Communications from 1G to 3G.	Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA)	T1:6.1,6.2, 6.3, T1: 6.4-6.6
7-9	Explain Wireless 4G systems, The Wireless Spectrum.	Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Transmission Techniques: Wireless Networks	T1:6.4-6.6, T1:6.7-6.8, 6.15 R2:7.1, 8.1
10-13	DescribeCarrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).	comparison of wired and Wireless LANs, WLAN Technologies: Infrared technology, UHF narrowband technology	T1:7.1, 7.4 T1:7.7, 7.8-7.10 R2:7.2
14-16	Explain WLAN Topologies and analyze transmission techniques	Spread Spectrum technology, Network Architecture, Physical layer, The Medium access control layer	T1: 6.12, 9.4,9.6 R2: 4.2,

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
17-20	Describe importance of Wireless Local Area Networks.	MAC Layer issues: Hidden terminal problem, Reliability, Collision avoidance, congestion avoidance, Congestion control	T1: 7.12,10.4, R2: 4.2, T1: 10.6
21-22	Explain Network architecture and analyze MAC layer issues.	Security, The IEEE 802.11e MAC protocol. The IEEE 802.11e MAC protocol. Introduction, importance of wireless PANs, the Bluetooth technology: history and applications	T1: 10.5, T1: 8.1,8.2, 8.4,8.5,8.6 R2: 4.4
23-27	Describe importance of Wireless Private Area Networks.	Technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch, Bluetooth security	T1: 8.2,8.9 R2: 4.4,
28-36	Explain Bluetooth technology and Bluetooth specifications.	Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering,	T1: 8.12, 8.13, 8.14
37-40	Analyze Enhancements to Bluetooth	QoS and Dynamics Slot Assignment, Scatter net formation., The IEEE 802.15.3, The IEEE 802.15.4, ZigBee components and network topologies	T1: 9.1, 9.2,9.3
41-45	Describe IEEE 802.15.3, The IEEE 802.15.4	The IEEE 802.15.4 LR-WPAN device architecture, physical layer, data link layer, the network layer, applications, IEEE 802.15.3a ultra wideband.	R1:7.1,7.3 R1:7.4,7.7

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY /PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Currently available Wireless Communication and Networks	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 6
2	Interfacing Modules	Work Shops/ Guest Lectures / NPTEL	PO 2, PO 6

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED PRORAMMING LABORATORY**			
Course Code	BESB09			
Programme	M.Tech (ES)			
Semester	I	ECE		
Course Type	Core			
Regulation	IARE - R18			
	Lectures	**Tutorials**	**Practical**	**Credits**
	-	-	3	2
Course Faculty	Mr. S.Lakshmana chari, Assistant Professor			

I. COURSE OVERVIEW:

This course provides knowledge of embedded C programming language. This covers the concepts for reading data from port pins of microcontroller, understanding the interfacing of data I/O devices, serial communication, and port on P89V51RD2 microcontroller. Through laboratory experiments and out-of-class assignments, students are provided learning experiences that enable them to provide in-depth knowledge about embedded processor, its hardware and software, explain programming concepts and embedded programming in C and assembly language and explain real time operating systems, inter-task communication and an embedded software development tool.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	--	I	Microprocessors and Microcontrollers Laboratory	--

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Programming Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	CHALK & TALK	✔	VIVA	✘	ASSIGNMENTS	✘	MOOCs
✔	LCD / PPT	✘	SEMINARS	✔	MINI PROJECT	✘	VIDEOS
✘	OPEN ENDED EXPERIMENTS						

V. EVALUATION METHODOLOGY:

Ccontinuous internal assessment (CIA):

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, with 20 marks for day to day evaluation and 10 marks for Internal Examination (CIE).

Semester End Examination (SEE):

The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the this courses is contains 12 experiments. The question paper pattern is as follows: Two full questions with 'either' 'or' choice will be drawn from each set. Each set contains 4 questions.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 10 marks for Continuous Internal Examination (CIE), 20 marks for Day to Day Evaluation.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Day to Day Evaluation	
CIA Marks	10	20	30

Continuous Internal Examination (CIE):

Two CIE exam shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration consisting of two sets.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, and storage technology	3	Lab related Exercises
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Lab related Exercises / Mini projects
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	1	Lab related Exercises
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	2	Lab related Exercises
PO 6	Independently carry out research / investigation and development work to solve practical problems	2	Lab related Exercises

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Use embedded C for reading data from port pins
II	Understand the interfacing of data I/O devices with microcontroller.
III	Understand serial communication and port RTOS on microcontroller.

VIII. COURSE OUTCOMES (COs):

CO Code	CO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB09.01	CO 1	Ability to write the programs for LED blinking and to interface the devices like switch, buzzer and LCD with P89V51RD2.	PO 1, PO 3	2
BESB09.02	CO 2	Ability to write the programs for interfacing of data I/O devices like seven segment display, keypad and RS232 with P89V51RD2.	PO 1, PO 2	3
BESB09.03	CO 3	Ability to write the programs for interfacing stepper motor and temperature sensor.	PO 4	2
BESB09.04	CO 4	Ability to understand real time operating systems, inter- task communication and analog to digital conversions.	PO 1, PO 3	2
BESB09.05	CO 5	Ability to write the programs for interfacing digital to analog conversion and elevator.	PO 6	2

3= High; 2 = Medium; 1 = Low

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO 1	3		1				
CO 2	3	2					
CO 3				2			
CO 4	3		1				
CO 5						2	

3= High; 2 = Medium; 1 = Low

X. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, PO 3, PO 4	SEE Exams	PO 1, PO 3, PO 4	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2, PO 3, PO 4, PO 6	Student Viva	PO 3, PO 6,	Mini Project	PO 2	Certification	-
Term Paper	-						

XI. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XII. SYLLABUS:

S No.	Experiment
1	Program to toggle all the bits of port P1 continuously with 250 ms delay.
2	Program to interface a switch and a buzzer to two different pins of a port such that the buzzer should sound as long as the switch is pressed.
3	Program to interface LCD data pins to port P1 and display a message on it.
4	Program to interface seven segment display.
5	Program to interface keypad. Whenever a key is pressed, it should be displayed on lcd.
6	Program to transmit message from microcontroller to PC serially using RS232. Program to receive a message from PC to microcontroller serially using RS232.
7	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
8	Program to read data from temperature sensor and display the temperature value.
9	Program Port RTOS on to 89V51 Microcontroller and verify. Run 2 to 3 tasks simultaneously on 89V51 SDK. Use LCD interface, LED interface, Serial communication.
10	Program to convert analog signal into digital (ADC).
11	Program to convert digital into analog (DAC).
12	Program to interface Elevator.

XIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Learning Objectives	Topics to be covered
1-3	Over view of Micro controller architecture.	Open the micro controller P89V51RD2 kit box and study the architecture.
4-6	Understand the LED toggling.	Program to toggle all the bits of port P1 continuously with 250 ms delay.
7-9	Understand the concepts of buzzer.	Program to interface a switch and a buzzer to two different pins of a port such that the buzzer should sound as long as the switch is pressed.
10-12	Understand the concept of LCD interfacing.	Program to interface LCD data pins to port P1 and display a message on it.
13-15	Understand seven segment display interface.	Program to interface seven segment display.
16-18	Understand the concept of keypad.	Program to interface keypad. Whenever a key is pressed, it should be displayed on lcd.
19-21	Understand the concept of serial communication.	Program to transmit message from microcontroller to PC serially using RS232. Program to receive a message from PC to microcontroller serially using RS232.
22-24	Understand the working principle of temperature sensor.	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
25-27	Understand the working principle of temperature sensor.	Program to read data from temperature sensor and display the temperature value.
28-30	Understand the concepts of RTOS.	Program Port RTOS on to 89V51 Microcontroller and verify. Run 2 to 3 tasks simultaneously on 89V51 SDK. Use LCD interface, LED interface, Serial communication.

31-33	Understand ADC and DAC.	Program to convert analog signal into digital (ADC) and digital into analog (DAC).
34-36	Understand interface of elevator.	Program to interface Elevator.

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II SEMESTER

INSTITUTE OF AERONAUTICAL ENGINEERING

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED SYSTEM ARCHITECTURE**				
Course Code	**BESB11**				
Programme	**M.Tech**				
Semester	**II**				
Course Type	**Core**				
Regulation	**IARE-R18**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Mr.K.Ravi, Assistant Professor**				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of embedded systems design paradigms, architectures. Subsequently the course covers important concepts like interpret possibilities and challenges, both with respect to software and hardware. In later units analysis of a system both as whole and in the included parts, to understand how these parts interact in the functionality and properties of the system.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES003	I	Computer Architecture	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded System Architecture	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each module carries equal weight age in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminar and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 6	Independently carry out research / investigation and development work to solve practical problems.	2	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understanding of fundamental embedded systems design paradigms, architectures.
II	Interpret possibilities and challenges, both with respect to software and hardware.
III	Analyze a system both as whole and in the included parts, to understand how these parts interact in the functionality and properties of the system.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe different Embedded system models, ISA architecture models.	CLO 1	Describe different Embedded system models, embedded standards, block diagrams Embedded board using von Neuman model.
		CLO 2	Demonstrate EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models.
CO 2	Demonstrate Internal processor design: ALU, memory.	CLO 3	Understand Internal processor design: ALU, registers, control unit, clock management
		CLO 4	Identify different processor i/o, interrupts, processor buses, processor performance
CO 3	Distinguish different memory managements.	CLO 5	Distinguish ROM, RAM, cache, auxiliary memory, memory management.
		CLO 6	Identify performance of Board buses:

COs	Course Outcome	CLOs	Course Learning Outcome
			Arbitration and timing, PCI bus example, integrating bus with components.
CO 4	Describe Middleware and applications and layers.	CLO 7	Understand Middleware and applications: PPP, IP middleware UDP, Java. Application layer: FTP client, SMTP, HTTP server and client.
		CLO 8	Describe Application layer: FTP client, SMTP, HTTP server and client.
CO 5	Design and development architectural patterns and reference models.	CLO 9	Design and development of architectural patterns and reference models.
		CLO 10	Creating the architectural structures and evaluating the architecture, debugging testing, and maintaining.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES004.01	CLO 1	Understand the different Embedded system models, embedded standards, block diagrams Embedded board using von Neuman model.	PO 1	3
BES004.02	CLO 2	Identify different ISA architecture models, application specific ISA models and general purpose ISA models.	PO 1	2
BES004.03	CLO 3	Understand Internal processor design: ALU, registers, control unit, clock management.	PO 2	2
BES004.04	CLO 4	Distinguish different processor i/o, interrupts, processor buses, processor performance.	PO 2	2
BES004.05	CLO 5	Understand ROM, RAM, cache, auxiliarymemory,memory management.	PO 3	3
BES004.06	CLO 6	Identify performance of Board buses: Arbitration and timing, PCI bus example, integrating bus with components	PO 3	3
BES004.07	CLO 7	Understand Middleware and applications: PPP, IP middleware UDP, Java	PO 6	1
BES004.08	CLO 8	Describe Application layer FTP client, SMTP, HTTP server and client	PO 6	1
BES004.09	CLO 9	Describe Design and development of architectural patterns and reference models	PO 1, PO 6	2

BES004.10	CLO 10	Creating the architectural structures and evaluating the architecture, debugging testing, and maintaining	PO 1, PO 6	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	2	1	1	1
CO 2		1	1	
CO 3	1			
CO 4	2		1	1
CO 5			3	1

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 6
CLO 1	3			
CLO 2	2			
CLO 3		2		
CLO 4		2		
CLO 5			2	
CLO 6			2	
CLO 7				1
CLO 8				1
CLO 9	3			2
CLO 10	3			2

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO2, PO3, PO6	SEE Exams	PO1, PO2, PO3, PO6	Seminar and Term Paper	PO1, PO2, PO3, PO6
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES –INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I	**INTRODUCTION TO EMBEDDED SYSTEMS**	**Class: 09**
Embedded system model, embedded standards, block diagrams, powering the hardware: Embedded board using von Neuman model; EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models: Instruction level parallelism.		
UNIT II	**PROCESSOR HARDWARE**	**Class: 09**
Internal processor design: ALU, registers, control unit, clock, on chip memory, processor i/o, interrupts, processor buses, processor performance.		
UNIT III	**SUPPORT HARDWARE**	**Class: 09**
Board memory: ROM, RAM, cache, auxiliary memory, memory management, memory performance. Board buses: Arbitration and timing, PCI bus example, integrating bus with components, bus performance.		
UNIT IV	**SOFTWARE**	**Class: 09**
Middleware and applications: PPP, IP middleware UDP, Java. Application layer: FTP client, SMTP, HTTP server and client.		
UNIT V	**ENGINEERING ISSUES OF SOFTWARE**	**Class: 09**
Design and development: architectural patterns and reference models: Creating the architectural structures, documenting the architecture, analyzing and evaluating the architecture, debugging testing, and maintaining.		
TEXT BOOKS:		
1. Tammy Noergaard, “Embedded system architecture”, Elsevier, 2006.Charles H. Roth Jr, Lizy Kurian.		
REFERENCES:		
1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C”, the publisher Paul Temme, 2011.		

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understand the basic concepts of Embedded system model, embedded standards	Introduction: Embedded system model, embedded standards, block diagrams powering the hardware: Embedded board using von Neuman model	T1:1.1, 1.2
4-6	Describe overall Embedded board using von Neuman model.	Powering the hardware: Embedded board using von Neuman model.	T1:2.1, R1:2.2
7-9	Understand the different ISA architecture models	EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models: Instruction level parallelism.	T1:2.2, 2.3
10-13	Describe Internal processor design	Internal processor design: ALU, registers, control unit, clock	T1:4.1, 4.2, 4.3 R1:4.2
14-16	Implementing the concepts of processor.	On chip memory, processor i/o, interrupts, processor buses, processor performance.	T1:4.2, 4.4
17-20	Understand the concepts of different memories.	Board memory: ROM, RAM, cache, auxiliary memory, memory management, memory performance.	T1: 5.1, 5.2 R1:5.5,5.6
21-22	Describe the concepts of board buses.	Board buses: Arbitration and timing, PCI bus example, integrating bus with components, bus performance.	T1:6.1, 6.2, 6.4
23-27	Understand Middleware and applications.	Middleware and applications: PPP, IP middleware UDP, Java.	T1:7.2, 7.3, 7.4 R1:7.1,7.4,7.5
28-36	Describe Application layer and different clients.	Application layer: FTP client, SMTP, HTTP server and client.	T1:8.1, 8.3
37-40	Understand design and development of architectural patterns	Design and development: architectural patterns and reference models: Creating the architectural structures	T1:5.3 R1:5.2
41-45	Understanding the concept of architecture.	Documenting the architecture, analyzing and evaluating the architecture, debugging testing, and maintaining.	T1:5.5, 5.6, 5.7, R1:5.8

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Embeddedstandards,and Embedded block diagrams	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 6
2	Application layer: FTP client, SMTP	Work Shops/ Guest Lectures / NPTEL	PO 3, PO 6

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTERNET OF THINGS (IoT)**				
Course Code	BESB12				
Programme	M.Tech (ES)				
Semester	II				
Course Type	Core				
Regulation	IARE - R18				
Course Structure	Theory			Practical	
	Lectures	Tutorials	Credits	Laboratory	Credits
	3	-	3	4	2
Course Faculty	Mr.K.Swathi, Assistant Professor				

I. COURSE OVERVIEW:

The Internet of Things is transforming our physical world into a complex and dynamic system of connected devices on an unprecedented scale. Advances in technology are making possible a more widespread adoption of IoT, from micro cameras to smart sensors that can asses crop conditions on a farm, to the smart home devices that are becoming increasingly popular.

The course covers the concepts of communication technologies, computer networks, cloud computing, and terms including the basic components of hardware and software. This course helps the students in gaining the knowledge about the sensor devices, different communication technologies like RFID, Bluetooth, and programming microcontroller for sending data to cloud.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES201	I	Embedded System Architecture	3

III. MARKS DISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Internet of Things	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

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20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, storage technology.	3	Seminars, Lab session
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Seminar & Term paper
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars, Lab session
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	Term paper
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	3	Term paper

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Learn the basic issues, policy and challenges in the Internet of Things.
II	Understand the components and the protocols in Internet of Things.
III	Understand the various modes of communications and build a small low cost embedded system with Internet of Things.
IV	Learn to manage the resources and deploy the resources into business.
V	Understand the cloud and internet environment.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define IOT and understand building blocks of Internet of things and characteristics.	CLO 1	Understand principles of Internet of Things (IoT).
		CLO 2	Understand the components of internet of things.
		CLO 3	Explain different communication technologies like RFID, Bluetooth, Zigbee, Wifi, Mobile internet etc.
CO 2	Understand the programming of microcontroller for IOT	CLO 4	Explain embedded communication software and software partitioning.
CO 3	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.	CLO 5	Discuss device and router management.
		CLO 6	Explain clustering and software agents.
		CLO 7	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.
CO 4	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.	CLO 8	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.

COs	Course Outcome	CLOs	Course Learning Outcome
		CLO 9	Explain the internet of things in context of EURIDICE.
		CLO 10	Understand ontology and apply ontology engineering in the internet of things
CO 5	Able to realize the set upof Cloud environment and understand web enabling constrained devices.	CLO 11	Explain set up of cloud environment and sending data from microcontroller to cloud.
		CLO 12	Discuss case studies related to internet of things.
		CLO 13	Identify common approaches used for future developments of IoT.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BES006.01	CLO 1	Understand principles of Internet of Things(IoT) .	PO 1	3
BES006.02	CLO 2	Understand the components of internet of things.	PO 1	3
BES006.03	CLO 3	Explain different communication technologies like RFID, Bluetooth, Zigbee, Wifi, Mobile internet etc.	PO 1, PO 3	3
BES006.04	CLO 4	Explain embedded communication software and software partitioning .	PO 1	3
BES006.05	CLO 5	Discuss device and router management.	PO 1, PO 2	2
BES006.06	CLO 6	Explain clustering and software agents.	PO 1, PO 2	2
BES006.07	CLO 7	Understand the concepts of data synchronization and fundamental concepts of agility and autonomy.	PO 1, PO 2	3
BES006.08	CLO 8	Understand the meaning of DiY and middleware technologies needed for DiY internet of things.	PO 2, PO 3	3
BES006.09	CLO 9	Explain the internet of things in context of EURIDICE.	PO 2, PO 3	3
BES006.10	CLO 10	Understand ontology and apply ontology engineering in the internet of things	PO 3, PO 6	3
BES006.11	CLO 11	Explain set up of cloud environment and sending data from microcontroller to cloud.	PO 3, PO 6	2
BES006.12	CLO 12	Discuss case studies related to internet of things.	PO 6, PO 7	2
BES006.13	CLO 13	Identify common approaches used for future developments of IoT.	PO 6, PO 7	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CO 1	3		3		
CO 2	3				
CO 3	2	3			
CO 4		1	3	2	
CO 5			2	3	3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CLO 1	3				
CLO 2	3				
CLO 3	3		3		
CLO 4	3				
CLO 5	2	3			
CLO 6	2	3			
CLO 7	2	3			
CLO 8		2	3		
CLO 9		2	3		
CLO 10			3	3	
CLO 11			3	2	
CLO 12				2	3
CLO 13				2	3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO3, PO5	SEE Exams	PO1, PO3, PO5, PO 6	Seminar and Term Paper	PO1, PO2, PO3, PO7
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT I	INTRODUCTION	Class:09
Definition – phases – Foundations – Policy– Challenges and Issues - identification - security – privacy. Components in internet of things: Control Units – Sensors – Communication modules – Power Sources – Communication Technologies – RFID – Bluetooth – Zigbee – Wifi – Rflinks – Mobile Internet – Wired Communication.		
UNIT II	**PROGRAMMING THE MICROCONTROLLER FOR IOT**	**Class:09**
Ecosystem, embedded communications software, software partitioning, module and task decomposition: Partitioning case study , protocol software, debugging protocols, tables and other data structures, table access routines, buffer and timer management, management software, device and router management: CLI based management and HTTP based management, agent to protocol interface, device to manager communication, system setup, boot and post-boot configuration, saving and restoring the configuration.		
UNIT III	**RESOURCE MANAGEMENT IN THE INTERNET OF THINGS**	**Class:09**
Clustering - Software Agents - Data Synchronization - Clustering Principles in an Internet of Things Architecture - The Role of Context - Design Guidelines -Software Agents for Object. Data Synchronization- Types of Network Architectures - Fundamental Concepts of Agility and AutonomyEnabling Autonomy and Agility by the Internet of Things-Technical Requirements for Satisfying the New Demands in Production - The Evolution from the RFID-based EPCNetwork to an Agent basedInternet of Things- Agents for the Behaviour of Objects.		
UNIT IV	**BUSINESS MODELS FOR THE INTERNET OF THINGS**	**Class:09**
The Meaning of DiY in the Network Society- Sensor-actuator Technologies and Middleware as a Basis for a DiY Service Creation Framework - Device Integration - MiddlewareTechnologies Needed for a DiY 36 | P a g e Internet of Things Semantic Interoperability as a Requirement for DiY Creation -Ontology-Value Creation in the Internet of Things-Application of Ontology Engineering in the Internet of Things-Semantic Web-Ontology - The Internet of Things in Context of EURIDICE - Business Impact.		
UNIT V	**FROM THE INTERNET OF THINGS TO THE WEB OF THINGS**	**Class:09**
Resource-oriented Architecture and Best Practices- Designing REST ful Smart Things - Web- enabling Constrained Devices - The Future Web of Things - Set up cloud environment – send data from microcontroller to cloud – Case studies – Open Source e-Health sensor platform – Be Close Elderly monitoring – Other recent projects.		

TEXT BOOKS:
1. Charalampos Doukas, "Building Internet of Things with the Arduino", Create space, April 2002. 2. Dieter Uckelmann et.al, "Architecting the Internet of Things", Springer, 1st Edition, 2011.
REFERENCES:
1. Luigi Atzor et.al, "The Internet of Things: A survey, ", Journal on Networks, Elsevier Publications, October 2010.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Define IOT and understand the components of internet of things	Definition, phases, Foundations Policy, Challenges and issues, identification, security, privacy. Components in internet of things	T1:1.1, 1.5
4-6	Describe Communication modules Communication Technologies	Control units, sensors, communication modules, power sources, communication technologies	T1:2.7
7-9	Understand RFID, Bluetooth, Zigbee	RFID, Bluetooth, Zigbee, Wifi, Rflinks, mobile internet, wired communication.	T2:2.2, 2.3
10-13	Understand ecosystem and embedded communication software	Ecosystem, embedded communications software, software partitioning, module and task decomposition: Partitioning case study	T1:3.1, 3.2, 3.3
14-16	Define protocol software, debugging protocols, tables	Protocol software, debugging protocols, tables and other data structures, table access routines, buffer and timer management, management software	T1:4.2, 4.4
17-20	Understand the concepts of device and router management	Device and router management: CLI based management and HTTP based management, agent to protocol interface, device to manager communication, system setup, boot and post-boot configuration, saving and restoring the configuration	T2: 5.1, 5.2
21-22	Understand clustering software Agents and data synchronization	Clustering, software agents, data synchronization, clustering principles in an Internet of Things architecture, the role of context design guidelines, software agents for object	T2:6.1, 6.2, 6.4
23-27	Define Types of Network Architectures - Fundamental Concepts of Agility.	Data synchronization, types of network Architectures, fundamental concepts of agility and autonomy enabling by the	T2:7.2, 7.3, 7.4

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
		Internet of Things, technical requirements for satisfying the new demands in production, the evolution from the RFID-based EPC Network to an agent based Internet of Things, agents for the behaviour of objects.	
28-32	Understand the Meaning of DiY in the Network Society- Sensor-actuator Technologies	The meaning of DiY in the network society, Sensor actuator technologies and Middleware as a basis for a DiY service creation framework, Device Integration, Middleware Technologies needed for a DiY	T1:8.1, 8.3
32-36	Understand application of Ontology Engineering in the Internet of Things	Interoperability as a requirement for DiY creation, Ontology, value creation in the Internet of Things, application of Ontology engineering in the Internet of Things, semantic web, Ontology, the Internet of Things in context of EURIDICE business impact.	T1:8.1, 8.3
37-40	Demonstrate resource-oriented Architecture	Resource oriented architecture and best practices designing REST full smart things, web enabling constrained devices	T1:8.6
41-45	Demonstrate Set up cloud environment – send data from microcontroller to cloud	The future web of things, set up cloud environment, send data from microcontroller to cloud, case studies, open source e-Health sensor platform, be close elderly monitoring, other recent projects..	T1:8.8, 8.9

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY/PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Real time implementation of simple modules using IoT.	Application oriented Projects and Seminars	PO 2, PO 3, PO 6
2	Program modelling	Seminars / Guest Lectures / NPTEL	PO 1, PO 6, PO 7

Prepared By:
Mr. K Swathi, Assistant Professor

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN				
Course Code	BESB16				
Programme	M.Tech (ES)				
Semester	II	ECE			
Course Type	Elective				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Course Faculty	Mrs. G.Mary swarna latha, Assistant Professor				

I. COURSE OVERVIEW:

This course provides the basic knowledge over the hardware units and devices for design of embedded systems. It also provides the information about the architectures of embedded RISC processors and system on chip processor design of embedded systems. This course is intended to Analyze interrupt latency, context switching time, for development of device drives for timing devices.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Embedded System Design	3
PG	BESB06	I	Principles of Distributed Embedded Systems	3

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microcontrollers for embedded system design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make- examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weight age in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Technical Seminar and Term Paper	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations are conducted during I year II semester and a term paper with overview of topic is to be prepared. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, and storage technology	2	Term paper, Seminar
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Term paper, Seminar
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	3	Term paper
PO 6	Independently carry out research / investigation and development work to solve practical problems	2	Term paper, Seminar

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Understand hardware units and devices for design of embedded systems.
II	Use architectures of embedded RISC processors and system on chip processor design of embedded systems.
III	Analyze interrupt latency, context switching time, for development of device drives for timing devices.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Ability to understand embedded hardware and software and how this applies to design of embedded system.	CLO 1	Understand principles of embedded systems design and their classification.
		CLO 2	Understand processor embedded into a system.
		CLO 3	Explain embedded hardware units and devices in system.
		CLO 4	Understand concept of embedded software and issues in designing complex system.
		CLO 5	Discuss design process in embedded system.
		CLO 6	Explain formalization of system design.
CO 2	Describe the architecture of 8051 and PIC controller.	CLO 7	Understand key concepts of 8051 architecture, input/output ports and circuits, external memory, counters and timers.
		CLO 8	Understand key concepts of PIC controllers, memory interfacing, I/O devices.
		CLO 9	Learn memory controller and memory arbitration schemes.
CO 3	Understand the PSOC architecture and instruction set of ARM processor in thumb mode.	CLO 10	Acquire the knowledge on Programmable system on chip architectures.
		CLO 11	Understand key concepts of continuous timer blocks, switched capacitor blocks, I/O blocks, digital blocks and programming of PSOC.
		CLO 12	Distinguish between Embedded CISC and RISC processor architecture.
		CLO 13	Explain ARM processor architecture, registers set, and modes of operation and overview of Instructions.
CO 4	Understand the exceptions, interrupt handling schemes and device driver.	CLO 14	Understand and apply Exceptions and Interrupt handling Schemes, Context and periods for context switching in embedded system design.
		CLO 15	Understand and apply Exceptions and Interrupt handling Schemes, Context and periods for context switching in embedded system design.
		CLO 16	Explain Device driver using interrupt service routine.
		CLO 17	Understand serial port device driver and device drivers for internal programmable timing devices.
CO 5	Acquire knowledge in serial communication and Ethernet protocols.	CLO 18	Explain the need of Serial communication protocols and Ethernet protocols.
		CLO 19	Understand SDMA, Channel and IDMA.
		CLO 20	Explain the necessity of external bus interface.

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes(PO)			
	PO 1	PO 2	PO 3	PO 6
CO 1	2	2	3	2
CO 2	2	2	3	
CO 3	2	2		
CO 4	2	2		2
CO 5		2	3	

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB16.01	CLO 1	Understand principles of embedded systems design and their classification.	PO1	2
BESB16.02	CLO 2	Understand processor embedded into a system.	PO1	2
BESB16.03	CLO 3	Explain embedded hardware units and devices in system.	PO1	2
BESB16.04	CLO 4	Understand concept of embedded software and issues in designing complex system.	PO1 PO6	2
BESB16.05	CLO 5	Discuss design process in embedded system.	PO1 PO2	2
BESB16.06	CLO 6	Explain formalization of system design.	PO3	3
BESB16.07	CLO 7	Understand key concepts of 8051 architecture, input/output ports and circuits, external memory, counters and timers.	PO3	3
BESB16.08	CLO 8	Understand key concepts of PIC controllers, memory interfacing, I/O devices.	PO1	2
BESB16.09	CLO 9	Learn memory controller and memory arbitration schemes.	PO1 PO2	2
BESB16.10	CLO 10	Acquire the knowledge on Programmable system on chip architectures.	PO1 PO2	2
BESB16.11	CLO 11	Understand key concepts of continuous timer blocks, switched capacitor blocks, I/O blocks, digital blocks and programming of PSOC.	PO1	2
BESB16.12	CLO 12	Distinguish between Embedded CISC and RISC processor architecture.	PO1	2
BESB16.13	CLO 13	Explain ARM processor architecture, registers set, and modes of operation and overview of Instructions.	PO1	2
BESB16.14	CLO 14	Understand and apply Exceptions and Interrupt handling Schemes, Context and periods for context switching in embedded system design.	PO3	3
BESB16.15	CLO 15	Understand and apply Exceptions and Interrupt handling Schemes, Context and	PO1	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
		periods for context switching in embedded system design.		
BESB16.16	CLO 16	Explain Device driver using interrupt service routine.	PO1	2
BESB16.17	CLO 17	Understand serial port device driver and device drivers for internal programmable timing devices.	PO3 PO6	3
BESB16.18	CLO 18	Explain the need of Serial communication protocols and Ethernet protocols.	PO3	3
BESB16.19	CLO 19	Understand SDMA, Channel and IDMA.	PO2 PO3	3
BESB16.20	CLO 20	Explain the necessity of external bus interface.	PO3	3

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CLOs	POs						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CLO 1	3						
CLO 2	2						
CLO 3	2						
CLO 4	2					2	
CLO 5	2	2					
CLO 6			3				
CLO 7			3				
CLO 8	2						
CLO 9	2	2					
CLO 10	2	2					
CLO 11	2						
CLO 12	2						
CLO 13	2						
CLO 14			3				
CLO 15	2						
CLO 16	2						
CLO 17			3			2	
CLO 18			3				

CLOs	POs						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CLO 19		2	3				
CLO 20			3				

XII. ASSESSMENT METHODOLOGIES–DIRECT:

CIE Exams	PO 1, P0 2 PO 3, PO 6	SEE Exams	PO 1, P0 2 PO 3, PO 6	Assignments	PO 2	Seminars	PO 3
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 6						

XIII. ASSESSMENT METHODOLOGIES–INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

MODULE -I	INTRODUCTION TO EMBEDDED SYSTEMS	Classes: 09
Overview of embedded systems, processor embedded into a system, embedded hardware units and devices in system, embedded software, complex system design, design process in embedded system, formalization of system design, classification of embedded systems.		
MODULE - II	**MICROCONTROLLERS**	**Classes: 09**
8051 architecture, input/output ports and circuits, external memory, counters and timers, PIC controllers; Interfacing processor 8051, PIC, memory interfacing, I/O devices, memory controller and memory arbitration schemes.		
MODULE - III	**EMBEDDED RISC PROCESSORS**	**Classes: 09**
Programmable system on chip architectures, continuous timer blocks, switched capacitor blocks, I/O blocks, digital blocks, programming of PSOC. Embedded RISC processor architecture, ARM processor architecture, registers set, modes of operation and overview of Instructions		
MODULE - IV	**INTERRUPTS AND DEVICE DRIVERS**	**Classes: 09**
Exceptions and Interrupt handling Schemes, Context and periods for context switching, deadline and interrupt latency; Device driver using interrupt service routine, serial port device driver and device drivers for internal programmable timing devices.		
MODULE - V	**NETWORK PROTOCOLS**	**Classes: 09**
Serial communication protocols, Ethernet protocol, SDMA, Channel and IDMA, external bus interface.		
Text Books:		
Raj Kamal, "Embedded Systems, Architecture Programming and Design", Tata Mc Graw Hill, 2 nd Edition, 2008.		

Muhammad Ali Mazidi, Rolin D. Mckinaly, Danny Causy, "PIC Microcontroller and Embedded Systems", Pearson Education, 1st Edition, 2008. 44.
Robert Ashpy, "Designers Guide to the Cypress PSOC", Elsevier, 1st Edition, 2005.

Reference Books:

Jonathan W. Valvano – Brookes / Cole, "Embedded Microcomputer Systems, Real Time Interfacing", Thomas Learning, 1st Edition, 1998.
Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developers Guides, Design & Optimizing System Software", Elsevier, 1st Edition, 2004.
John B. Peatman, "Designing with PIC Microcontrollers", PH Inc, 1st Edition, 1998.

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	CLOs	Reference
1.	Introduction	CLO 1	T1: 1.1.1
2.	Overview of embedded systems	CLO 1	T1: 1.1.2
3.	Processor embedded into a system		T1: 1.2
4.	Embedded hardware units and devices in system	CLO 1	T1: 1.3
5.	Embedded software	CLO 8	T1: 1.4
6.	Complex system design	CLO 5	T1: 1.7
7.	Design process in embedded system	CLO 5	T1: 1.8
8.	Formalization of system design	CLO 6	T1: 1.9
9.	Classification of embedded systems	CLO 5	T1: 1.11
10.	8051 architecture	CLO 6	T1: 2.1.1
11.	Input/output ports and circuits	CLO 5	T1: 2.1.3
12.	External memory	CLO 7	T1: 2.1.4
13.	Counters and timers	CLO 7	T1: 2.1.5
14.	PIC controllers	CLO 2	T2: 1.2
15.	Interfacing processor 8051	CLO 8	T1: 2.1.6
16.	PIC, memory interfacing	CLO 8	T2: 2.1
17.	I/O devices	CLO 9	T2: 2.2
18.	Memory controller	CLO 10	T2: 2.3
19.	Memory arbitration schemes	CLO 11	T1: 2.4
20.	Programmable system on chip architectures	CLO 11	T3:1.1
21.	Continuous timer blocks,	CLO 11	T3:1.2
22.	Switched capacitor blocks	CLO 14	T3:2.4
23.	I/O blocks, digital blocks,	CLO 16	T3:2.5
24.	Programming of PSOC.	CLO 18	T3:3.1
25.	Embedded RISC processor architecture	CLO 16	T1: 2.3.1
26.	ARM processor architecture,	CLO 18	T1: 2.3.3
27.	Registers set	CLO 16	T1: 2.3.3
28.	Modes of operation and overview of Instructions	CLO 15	T1: 2.3.3
29.	Exceptions and Interrupt handling Schemes.	CLO 15	T1: 4.4
30.	Exceptions and Interrupt handling Schemes.	CLO 15	T1: 4.4
31.	Context and periods for context switching,	CLO 15	T1: 4.6
32.	Context and periods for context switching,	CLO 14	T1: 4.6
33.	Deadline and interrupt latency	CLO 14	T1: 4.6
34.	Device driver using interrupt service routine	CLO 15	T1: 4.9

Lecture No.	Topics to be covered	CLOs	Reference
35.	Serial port device driver	CLO 17	T1: 4.9.4
36.	Device drivers for internal programmable timing devices.	CLO 18	T1: 4.9.5
37.	Device drivers for internal programmable timing devices.	CLO 18	T1: 4.9.5
38.	Serial communication protocols,	CLO 18	T1: 3.10.1
39.	Serial communication protocols	CLO 18	T1: 3.10.2
40.	Ethernet protocol	CLO 18	T1: 3.10.3
41.	Ethernet protocol	CLO 13	T1: 3.10.4
42.	SDMA,	CLO 13	T1: 3.10.5
43.	Channel	CLO 13	T1: 3.10.6
44.	IDMA	CLO 12	T1: 3.11
45.	External bus interface	CLO 20	T1: 3.12

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs
1	Design examples of embedded system.	Project	PO 1, PO 2, PO 3
2	Program modelling	Seminars / Guest Lectures / NPTEL	PO 2,PO 3, PO 6
3	Case studies of different embedded system applications.	Seminars / Guest Lectures / NPTEL	PO 1, PO 3,PO6

Prepared by:
Ms. G Mary Swarna Latha, Assistant Professor **HOD, ECE**

INSTITUTE OF AERONAUTICAL ENGINEERING

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Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	EMBEDDED SYSTEM LABORATORY			
Course Code	BESB19			
Programme	M.Tech (ES)			
Semester	II	ECE		
Course Type	Core			
Regulation	IARE - R18			
	Lectures	Tutorials	Practical	Credits
	-	-	3	2
Course Faculty	Mrs. G.Mary swarna latha, Assistant Professor			

I. COURSE OVERVIEW:

This course provides knowledge of Embedded System Lab. This covers the concepts for reading data from port pins of microcontroller, the interfacing of LED, KEYPAD and various motors to ARM7 (LPC2148). Along with this interfacing amplifiers, filters, converters, ALU operations and PSOC (CY8C29466, 24X1).

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES101	I	Embedded Programming Laboratory	2

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded System Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	CHALK & TALK	✔	VIVA	✘	ASSIGNMENTS	✘	MOOCs
✔	LCD / PPT	✘	SEMINARS	✔	MINI PROJECT	✘	VIDEOS
✘	OPEN ENDED EXPERIMENTS						

V. EVALUATION METHODOLOGY:

Continuous Internal Assessment (CIA):

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, with 20 marks for day to day evaluation and 10 marks for Internal Examination (CIE).

Semester End Examination (SEE):

The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the this courses is contains 12 experiments. The question paper pattern is as follows: Two full questions with 'either' 'or' choice will be drawn from each set. Each set contains 4 questions.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 10 marks for Continuous Internal Examination (CIE), 20 marks for Day to Day Evaluation.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Day to Day Evaluation	
CIA Marks	10	20	30

Continuous Internal Examination (CIE):

Two CIE exam shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration consisting of two sets.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded systems and sub areas IOT, processor technology, and storage technology	3	Lab related Exercises
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Lab related Exercises
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing	3	Lab related Exercises
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Lab related Exercises
PO 6	Independently carry out research / investigation and development work to solve practical problems	3	Lab related Exercises
PO 7	Recognize the need to engage in lifelong learning through continuing education and research	2	Lab related Exercises

3= High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Use embedded C for reading data from port pins.
II	Understand the interfacing of data I/O devices with microcontroller.
III	Understand serial communication, port RTOS on microcontroller

VIII. COURSE OUTCOMES (COs):

CO Code	CO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB19.01	CO 1	Ability to write the programs for LED blinking and to interface the devices like LCD and KEYPAD with ARM7 (LPC2148).	PO 1, PO3 PO 6, PO7	2
BESB19.02	CO 2	Ability to write the programs for interfacing of I/O devices like MOTORS, LED with ARM7 (LPC2148).	PO 1, PO 3 PO 4, PO6 PO7	3
BESB19.03	CO 3	Ability to write the programs for interfacing programmable gain amplifier, study of various characteristics of Filters with PSOC (CY8C29466, 24X1).	PO 1, PO 2 PO 3, PO 4 PO 6, PO7	2
BESB19.04	CO 4	Ability to write the programs for interfacing converters, digital functions with PSOC (CY8C29466, 24X1).	PO 1, PO 2 PO 3, PO 4 PO 6, PO7	3
BESB19.05	CO 5	Ability to write the programs to do ALU operations and timing operations by interfacing PSOC (CY8C29466, 24X1).	PO 1, PO 2 PO 3, PO 4 PO 6, PO7	3

3= High; 2 = Medium; 1 = Low

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO6	PO7
CO 1	3		2		2	2
CO 2	2		3	3	2	3
CO 3	3	2	2	3	2	2
CO 4	3	3	2	2	3	2
CO 5	3	2	3	2	3	2

3= High; 2 = Medium; 1 = Low

X. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, PO 3, PO 4	SEE Exams	PO 1, PO 3, PO 4	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2, PO 3, PO 6	Student Viva	PO 1, PO 2, PO 3, PO 4 , PO 6	Mini Project	PO 6, PO 7	Certification	-
Term Paper	-						

XI. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XII. SYLLABUS:

S No.	Experiment
1	Program to toggle all the led to port and with some time delay.
2	Program to Interface LCD to ARM7 and display message on screen.
3	Program to Interface keypad with ARM7.
4	Program to Interface LED with ARM7.
5	Program to Stepper motor interfacing with ARM7.
6	Program to Interface DC motor with ARM7.
7	Program to implement Study and characterization of the Programmable Gain Amplifier (PGA): Gain bandwidth Product through PSOC.
8	Program to implement Low pass, High pass and Band pass filters and their characterization using PSOC.
9	Program to do Experiments with on-chip ADC's and DAC's using PSOC.
10	Program to implement Digital Function Implementation using Digital Blocks. a. Timer experiment b. Counter for blinking LED c. PWM experiment d. Digital buffer and digital inverter USING PSOC.
11	Program to implement Logical/Arithmetic functions using PSOC Microcontroller.
12	Program to implement Timer operation in different Modes using PSOC

XIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Learning Objectives	Topics to be covered
1-3	Over view of Micro controller architecture.	Open the micro controller kit box and study the architecture.
4-6	Understand the LED blinking.	Program to toggle all the led to port and with some time delay.
7-9	Understand the concepts of LCD.	Program to Interface LCD to ARM7 and display message on screen.
10-12	Understand the keypad structure.	Program to Interface keypad with ARM7.
13-15	Understand the design LED.	Program to Interface LED with ARM7.
16-18	Understand the design of stepper motor.	Program to Stepper motor interfacing with ARM7.
19-21	Understand the design of DC motor.	Program to Interface DC motor with ARM7.
22-24	Understand the characteristics of programmable gain amplifier.	Program to implement Study and characterization of the Programmable Gain Amplifier (PGA): Gain bandwidth Product through PSOC.
25-27	Understand the concepts of filters.	Program to implement Low pass, High pass and Band pass filters and their characterization using PSOC.
28-30	Understand the functionality ADC and DAC.	Program to do Experiments with on-chip ADC's and DAC's using PSOC.
31-33	Understand digital function implementation.	Program to implement Digital Function Implementation using Digital Blocks.

		a. Timer experiment b. Counter for blinking LED c. PWM experiment d. Digital buffer and digital inverter USING PSOC.
34-36	Understand ALU operation and timers.	Program to implement Logical/Arithmetic functions using PSOC Microcontroller.
37-39	Understand timer operation.	Program to implement Timer operation in different Modes using PSOC
40-42	Internal Lab Exam	CIE-I

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTERNET OF THINGS LABORATORY**				
Course Code	BESB20				
Programme	M.Tech (ES)				
Semester	II				
Course Type	Core				
Regulation	IARE - R18				
Course Structure	Theory			Practical	
	Lectures	Tutorials	Credits	Laboratory	Credits
	-	-	-	4	2
Course Faculty	Mr.K.Swathi, Assistant Professor				

I. COURSE OVERVIEW:

The Internet of Things is transforming our physical world into a complex and dynamic system of connected devices on an unprecedented scale. Advances in technology are making possible a more widespread adoption of IoT, from micro cameras to smart sensors that can asses crop conditions on a farm, to the smart home devices that are becoming increasingly popular.

The course covers the concepts of communication technologies, computer networks, cloud computing, and terms including the basic components of hardware and software. This course helps the students in gaining the knowledge about the sensor devices, different communication technologies like RFID, Bluetooth, and programming microcontroller for sending data to cloud.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BES201	I	Embedded System Architecture	3

III. MARKS DISTRIBUTION

Subject	SEE Examination	CIA Examination	Total Marks
Internet of Things Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	pen Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	**Performance**	**Calculations and Graph**	**Results and Error Analysis**	**Viva**	**Total**
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IOT, processor technology, storage technology.	3	Lab related Exercises
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Lab related Exercises/Mini projects
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Lab related Exercises
PO 6	Independently carry out research / investigation and development work to solve practical problems.	3	Lab related Exercises
PO 7	Recognize the need to engage in lifelong learning through continuing education and research.	3	Lab related Exercises

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the IoT using Arduino programming.
II	Understand the interfacing of data I/O devices with Arduino.
III	Understand the design steps using Rasberry Pi.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the design of IOT with arduino and android.	CLO 1	Design and develop IOT with arduino programming
		CLO 2	Understand the Controlling RGB LED using Arduino and Wi-Fi Module.
		CLO 3	Understand the Programming for Internet of things with Android and Arduino
CO 2	Understand the programming of Bluetooth modules with various applications.	CLO 4	Understand the Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application
CO 3	Understand the concepts of interface temperature with android.	CLO 5	Understand the Interface Temperature sensor and Monitoring using IoT with Arduino Uno and display
		CLO 6	Understand the to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android.

COs	Course Outcome	CLOs	Course Learning Outcome
		CLO 7	Understand the Programming for Node MCU for track location without using GPS module and fundamental concepts of agility and autonomy.
CO 4	Understand the Wi-Fi module using Raspberry pi to connect devices.	CLO 8	Analyze how to send data from Arduino to Webpage using Wi-Fi module
		CLO 9	Analyze Internet of things (IoT) by using a Raspberry Pi to connect devices.
		CLO 10	Develop and design how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle
CO 5	Understand the development of motion sensor using Arduino and IoT.	CLO 11	Develop and interface a motion sensor to use GPIO pins with a Raspberry Pi.
		CLO 12	Develop and design interface Gas sensor for detection and monitoring using Arduino and IoT.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BESB20.01	CLO 1	Design and develop IOT with arduino programming	PO 1	3
BESB20.02	CLO 2	Understand the Controlling RGB LED using Arduino and Wi-Fi Module	PO 1	3
BESB20.03	CLO 3	Understand the Programming for Internet of things with Android and Arduino	PO 1, PO 3	3
BESB20.04	CLO 4	Understand the Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application	PO 1	3
BESB20.05	CLO 5	Understand the Interface Temperature sensor and Monitoring using IoT with Arduino Uno and display digital value on LCD.	PO 1, PO 2	2
BESB20.06	CLO 6	Understand the to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android Application.	PO 1, PO 2	2
BESB20.07	CLO 7	Understand the Programming for Node MCU for track location without using GPS module	PO 1, PO 2	3
BESB20.08	CLO 8	Analyze how to send data from Arduino to Webpage using Wi-Fi module	PO 2, PO 3	3
BESB20.09	CLO 9	Analyze Internet of things (IoT) by using a Raspberry Pi to connect devices.	PO 2, PO 3	3

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BESB20.10	CLO 10	Develop and design how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle	PO 3, PO 6	3
BESB20.11	CLO 11	Develop and interface a motion sensor to use GPIO pins with a Raspberry Pi.	PO 3, PO 6	2
BESB20.12	CLO 12	Develop and design interface Gas sensor for detection and monitoring using Arduino and IoT	PO 6, PO 7	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CO 1	3		3		
CO 2	3				
CO 3	2	3			
CO 4		1	3	2	
CO 5			2	3	3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CLO 1	3				
CLO 2	3				
CLO 3	3		3		
CLO 4	3				
CLO 5	2	3			
CLO 6	2	3			
CLO 7	2	3			
CLO 8		2	3		
CLO 9		2	3		
CLO 10			3	3	
CLO 11			3	2	

Course Learning Outcomes (CLOs)	Program Outcomes (PO)				
	PO 1	PO 2	PO 3	PO 6	PO 7
CLO 12				2	3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO1, PO3, PO5	SEE Exams	PO1, PO3, PO5, PO 6	Seminar and Term Paper	-
Viva	-	Mini Project	-	Laboratory Practices	PO1, PO2, PO3, PO7

XIII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

LIST OF EXPERIMENTS	
Week-1	**IOT WITH ARDUINO PROGRAMMING**
Introduction to Internet of Things (IoT) using Arduino programming	
Week-2	**CONROLLING RGB LED**
Programming for Controlling RGB LED using Arduino and Wi-Fi Module	
Week-3	**IOT TO CONTROL REMOTE LED**
Programming for Internet of things with Android and Arduino. Build an Arduino IoT to control a remote LED	
Week-4	**INTERFACING BLUETOOTH MODULE**
Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application	
Week-5	**INTERFACING TO TEMPERATURE SENSOR**
Programming to Interface Tempaetaure sensor and Monitoring using IoT with Arduino Uno and display digital value on LCD.	
Week-6	**INTERFCAING IR SENSOR**
Programming to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android Application.	
Week-7	**TRACK LOCATION**
Programming for Node MCU for track location without using GPS module	
Week-8	**SEND DATA FROM ARDUINO TO WEB PAGE**
Programming for how to send data from Arduino to Webpage using Wi-Fi module	
Week-9	**IOT WITH RASBERRY PI**
Introduction to Internet of things (IoT) by using a Raspberry Pi to connect devices.	
Week-10	**SETUP WI-FI ON RASBERRY PI USING USB**
Programming for how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle	
WeeK-11	**SETUP WI-FI ON RASBERRY PI USING USB**

Programming to interface a motion sensor to use GPIO pins with a Raspberry Pi.	
Week-12	**INTERFACE TO GAS SENSOR**
Programming to interface Gas sensor for detection and monitoring using Arduino and IoT	
Text Books:	
1. Mark torvalds, "Arduino Programming: Step-by-step guide to mastering arduino hardware and software(Arduino, Arduino projects, Arduino uno, Arduino starter kit, Arduino ide, Arduino yun, Arduino mega, Arduino nano) Kindle Edition 2. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008.	
REFERENCES:	
1. Luigi Atzor et.al, "The Internet of Things: A survey, ", Journal on Networks, Elsevier Publications, October 2010.	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Week No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Introduction to Internet of Things (IoT) using Arduino programming	CLO 1, CLO 2	T1:1.4
2	Programming for Controlling RGB LED using Arduino and Wi-Fi Module	CLO 1, CLO 2	T1:1.5
3	Programming for Internet of things with Android and Arduino. Build an Arduino IoT to control a remote LED	CLO 1, CLO 2, CLO 3	T1:2.5
4	Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application	CLO 1, CLO 2, CLO 4	T1:2.5
5	Programming to Interface Tempaetaure sensor and Monitoring using IoT with Arduino Uno and display digital value on LCD.	CLO 1, CLO 2, CLO 5	T1:22.7
6	Programming to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android Application.	CLO 1, CLO 2, CLO 6	T1:6.3
7	Programming for Node MCU for track location without using GPS module.	CLO 1, CLO 2, CLO 7	T1:7.5
8	Programming for how to send data from Arduino to Webpage using Wi-Fi module	CLO 1, CLO 2, CLO 8	T1:8.5
9	Introduction to Internet of things (IoT) by using a Raspberry Pi to connect devices.	CLO 1, CLO 2, CLO 9	T1:12.2
10	Programming for how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle.	CLO 1, CLO 2, CLO 10	T1:12.3
11	Programming to interface a motion sensor to use GPIO pins with a Raspberry Pi.	CLO 1, CLO 2, CLO 11	T1:12.10
12	Programming to interface Gas sensor for detection and monitoring using Arduino and IoT	CLO 1, CLO 2, CLO 12	T1:13.2

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY/PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Real time implementation of simple modules using IoT.	Application oriented Projects and Seminars	PO 2, PO 3, PO 6
2	Program modeling	Seminars / Guest Lectures / NPTEL	PO 1, PO 6, PO 7

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED WIRELESS SENSOR NETWORKS**				
Course Code	**BESB14**				
Programme	**M.Tech**				
Semester	**II**				
Course Type	**Core**				
Regulation	**IARE - R18**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	**-**	**3**	**-**	**-**
Course Faculty	**Dr. China Venkateswarlu, Professor**				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of wireless, embedded, internetworked sensor/actuator systems, an emerging technology that can provide visibility into and control over complex physical processes. Sensor net systems have applications to many societal-scale problems including health, safety, energy, and the environment. However, their design raises challenges across all areas of computer systems research, including platform architecture, power systems, operating systems, embedded databases, networking, data management, and machine learning. Many of these challenges stem from severe energy-constraints, deep physical embedding, volatile network connectivity, and small physical form factor, all of which present different design issues than traditional computing systems, and require a different design approach.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB14	I	Embedded System Design	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Wireless Sensor Networks	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9^{th} and 17^{th} week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of embedded system and sub areas IoT, Processor technology, storage technology.	3	Term paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Term paper and Guest Lectures
PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminar and Guest Lectures
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	NPTEL Videos and Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the concepts of sensor networks to use in embedded wireless sensor networks.
II	Use sensor programming in wireless sensor networks.
III	Analyze wireless sensor networks for different applications.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Define the hardware and other components, energy level of consumption of sensor nodes.	CLO 1	Understanding the basic concept of WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture
		CLO 2	Study of hardware components, energy consumption of sensor nodes
		CLO 3	Examine the various operating systems and execution environments, some examples of sensor nodes
CO 2	Describe various principles involved in the design of Sensor network scenarios.	CLO 4	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit
		CLO 5	Describe the functions of design principles for WSNs
CO 3	Demonstrate features of Sensor programming, introduction to tiny OS programming.	CLO 6	Study the features of service interfaces of WSNs, gateway concepts
		CLO 7	Study the features of Sensor programming, introduction to tiny OS programming
		CLO 8	Understand the fundamentals of programming sensors using nes C
CO 4	Collect functions of design principles for WSNs.	CLO 9	Study the features of Algorithms for WSN Techniques for protocol programming
		CLO 10	Understand the concepts of cooperating objects and sensor networks

COs	Course Outcome	CLOs	Course Learning Outcome
CO 5	Discuss performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring.	CLO 11	Study the features of system architectures, Study the design issues and design of programming models
		CLO 12	Implement Wireless sensor networks for environmental monitoring
		CLO 13	Analyze the performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring
		CLO 14	Analyze the performance of Inter-vehicle communication networks

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BESB14.01	CLO 1	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit	PO 3, PO 4,	3, 3
BESB14.02	CLO 2	Describe the functions of design principles for WSNs	PO 2, PO 3,	2, 3
BESB14.03	CLO 3	Study the features of service interfaces of WSNs, gateway concepts	PO 4	3
BESB14.04	CLO 4	Study the features of Sensor programming, introduction to tiny OS programming	PO 3	3
BESB14.05	CLO 5	Understand the fundamentals of programming sensors using nes C	PO 1	3
BESB14.06	CLO 6	Study the features of Algorithms for WSN Techniques for protocol programming	PO 1, PO 2	3, 2
BESB14.07	CLO 7	Understand the concepts of cooperating objects and sensor networks	PO 1, PO 3	3, 3
BESB14.08	CLO 8	Study the features of system architectures, Study the design issues and design of programming models	PO 1, PO 2	3, 2, 2
BESB14.09	CLO 9	Implement Wireless sensor networks for environmental monitoring	PO 2, PO 7	2, 2
BESB14.10	CLO10	Analyze the performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring	PO 4, PO 7	3, 2
BESB14.11	CLO 11	Analyze the performance of Inter-vehicle communication networks	PO 2, PO 4	2, 3
BESB14.12	CLO 12	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit	PO 3, PO 4	3, 3
BESB14.13	CLO 13	Describe the functions of design principles for WSNs	PO 2, PO 3	2, 3
BESB14.14	CLO 14	Study the features of service interfaces of WSNs, gateway concepts	PO 4	3

3 = High; 2 = Medium; 1 = Low2

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes(PO)			
	PO 1	PO 2	PO 3	PO 4
CO 1	3	2	3	
CO 2		2	3	3
CO 3	3		3	3
CO 4	3	2	3	
CO 5	3	2		3

3 = High; 2 = Medium; 1 = Low2

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcome(PO)			
	PO 1	PO 2	PO 3	PO 4
CLO 1	3	2		
CLO 2		2		
CLO 3			3	
CLO 4			3	3
CLO 5		2	3	
CLO 6				3
CLO 7			3	
CLO 8	3			
CLO 9	3	2		
CLO 10	3		3	
CLO 11	3	2		
CLO 12		2		
CLO 13				3
CLO 14		2		3

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT:

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 3 PO 4,	Seminar and Term Paper	PO 1, PO 2 PO 3, PO 4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES –INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT-I	**INTRODUCTION TO WSN**	**Classes: 09**
Introduction to WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture, hardware components, energy consumption of sensor nodes, operating systems and execution environments, some examples of sensor nodes.		
UNIT-II	**NETWORK ARCHITECTURE**	**Classes: 09**
Sensor network scenarios, optimization goals and figures of merit, design principles for WSNs, service interfaces of WSNs, gateway concepts.		
UNIT-III	**SENSOR NETWORK IMPLEMENTATION:**	**Classes: 09**
Sensor programming, introduction to tiny OS programming and fundamentals of programming sensors using nes C. Algorithms for WSN: Techniques for protocol programming.		
UNIT-IV	**PROGRAMMING MODELS:**	**Classes: 09**
An introduction to the concept of cooperating objects and sensor networks, system architectures and programming models.		
UNIT-V	**CASE STUDIES:**	**Classes: 09**
Wireless sensor networks for environmental monitoring, wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.		

Text Books:

1. Holger karl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley, 1st Edition, 2005.
2. Liljana Gavrilovska, Srdjan Krco, Veljko Milutinovic, Ivan Stojmenovic, Roman Trobec, "Application and Multidisciplinary Aspects of Wireless Sensor Networks", Springer, London Limited, 1st Edition, 2011.

Reference Books:

1. Michel Banatre, Pedro Jose Marron, Anibal Ollero, A. Dam Wolisz, "Cooperating Embedded Systems and Wireless Sensor Networks", John Wiley & Sons, 1st Edition, 2008.
2. Seetharaman Iyengar, Nandhan, "Fundamentals of Sensor Network Programming Applications and Technology", John Wiley & Sons, 1st Edition, 2008.

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1-3	Understanding the basic concept of WSN, challenges for WSNs, characteristic requirements, required mechanisms, single node architecture	Introduction to WSN, challenges for WSNs, characteristic requirements, required mechanisms	T1:2.3 to 2.7 R1: 1.5 to 1.8
4-6	Study of hardware components, energy consumption of sensor nodes	Single node architecture, hardware components	T1:4.1 to 4.8 R2: 2.7 to 2.8
7-9	Examine the various operating systems and execution environments, some examples of sensor nodes	energy consumption of sensor nodes, operating systems and execution environments, some examples of sensor nodes	T1:7.1 to 7.9 R1: 2.15 to 2.16
10-13	Discuss the various principles involved in the design of Sensor network scenarios, optimization goals and figures of merit	Sensor network scenarios, optimization goals and figures of merit	T1:8.1 to 8.4 R1: 3.4 to 3.5
14-16	Describe the functions of design principles for WSNs	design principles for WSNs, service interfaces of WSNs, gateway concepts	T1:8.8 to 8.9 R1: 3.8 to 3.9
17-20	Study the features of service interfaces of WSNs, gateway concepts	Sensor programming, introduction to tiny OS programming and fundamentals of programming sensors using nes C	T2: 8.13 to 8.14 R1: 3.12 to 3.13
21-24	Study the features of Sensor programming, introduction to tiny OS programming	Algorithms for WSN: Techniques for protocol programming	T2: 9.4 to 9.6 R1: 4.5 to 4.7
25-28	Study the features of Algorithms for WSN Techniques for protocol programming	An introduction to the concept of cooperating objects and sensor networks	T2: 9.10 to 9.11 R1: 5.1 to 5.5
29-32	Understand the concepts of cooperating objects and sensor networks	system architectures and programming models	T2: 1.6 R1: 5.10 to 5.12
32-36	Study the features of system architectures, Study the design issues and design of programming models	Wireless sensor networks for environmental monitoring	T2: 1.9 R2: 2.1 to 2.3
37-40	Implement Wireless sensor networks for environmental monitoring	wireless sensor networks with mobile nodes	T2: 2.7 to 2.8 R2: 3.1 to 3.5
41-45	Analyze the performance of wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring.	autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.	T2: 4.5 to 4.6 R2: 5.8 to 5.9

XVI. GAPS IN THE SYLLABUS-TO MEET INDUSTRY /PROFESSIONAL REQUIREMENTS:

S No	Description	Proposed Actions	Relevance with POs
1	Design of Sensor network scenarios	Seminars / NPTEL	PO 1, PO 3, PO 4
2	OS programming technology	Seminars / Guest Lectures / NPTEL	PO 2, PO 4, PO 7
3	Low-Power Networking Systems	Laboratory Practices	PO 3, PO 4

Prepared By:

Dr. China Venkateswarlu, Professor **HOD, ECE**

III SEMESTER

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**EMBEDDED REAL TIME OPERATING SYSTEMS**			
Course Code	**BESB22**			
Programme	**M.Tech (ES)**			
Semester	**III**	**ECE**		
Course Type	**Elective**			
Regulation	**R18**			
Course Structure	**Theory**		**Practical**	
	Lectures	**Tutorials**	**Practicals**	**Credits**
	3	**-**	**-**	**3**
Course Faculty	**Dr. S China Venkateswarlu, Professor, ECE**			

I. COURSE OVERVIEW:

Embedded Real-Time Operating System presents computing environment that reacts to input within a specific time period. A real-time deadline can be so small that system reaction appears instantaneous. The term real-time computing has also been used, however, to describe "slow real-time" output that has a longer, but fixed, time limit. Learning the difference between real-time and standard operating systems is as easy as imagining yourself in a computer game. Each of the actions you take in the game is like a program running in that environment. A game that has a real-time operating system for its environment can feel like an extension of your body because you can count on a specific "lag time:" the time between your request for action and the computer's noticeable execution of your request. A standard operating system, however, may feel disjointed because the lag time is unreliable. To achieve time reliability, real-time programs and their operating system environment must prioritize deadline actualization before anything else. In the gaming example, this might result in dropped frames or lower visual quality when reaction time and visual effects conflict.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
PG	BESB01	I	Principles of Distributed Embedded System	3

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Embedded Real Time Operating Systems	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each module carries equal weight age in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems and sub areas IoT, Processor technology, and Storage technology.	3	Seminar and Term Paper
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Guest Lectures

PO 3	Respond to global policy initiatives and meet the emerging challenges with sustainable technological solutions in the field of electronic product designing.	3	Seminars
PO 4	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems.	3	Guest Lecturers

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:

I	Understand and analyze theory and implementation of tasks.
II	Analyze synchronization problems and to use semaphore operations.
III	Analyze interrupt service routines for interrupts and timers.

VIII. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understanding the UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write), process control (fork, vfork, exit, wait, waitpid, exec).	CLO 1	Understanding the basic concept of UNIX/LINUX, overview of commands.
		CLO 2	Study of file I/O (open, create, close, lseek, read, write),
		CLO 3	Examine the process control (fork, vfork, exit, wait, waitpid, exec).
CO 2	Examine the RTOS, history of OS, Scheduler, objects, services, characteristics of RTOS, defining a task, asks states and scheduling, task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue, states, content, storage, operations and use.	CLO 4	Discuss the RTOS, history of OS, Scheduler, objects, services, characteristics of RTOS, defining a task.
		CLO 5	Understand asks states and scheduling, task operations, structure, synchronization, Communication.
		CLO 6	Examine the concurrency, defining Semaphores, operations and use.
		CLO 7	Describe the defining message Queue, states, content, storage, operations and use..
CO 3	Describe the Objects, Services AND I/O, Pipes, event registers, signals, other building blocks, component configuration. Basic I/O concepts, I/O subsystem	CLO 8	Study the Objects, Services AND I/O, Pipes, event registers, and signals.
		CLO 9	Study the other building blocks, component configuration.
		CLO 10	Describe the Basic I/O concepts, I/O subsystem..
CO 4	Study Exceptions, Interrupts and Timers, Exceptions, interrupts, applications, processing of exceptions and spurious interrupts, real time clocks, programmable timers, timer interrupt Service routines, soft timers, operations.	CLO 11	Understand Exceptions, Interrupts and Timers, Exceptions, interrupts.
		CLO 12	Study applications, processing of exceptions and spurious interrupts.
		CLO 13	Describe real time clocks, programmable timers, timer interrupt.
		CLO 14	Understand the Service routines, soft timers, operations.
CO 5	Analyze Case Studies 0f RTOS, RT linux, Micro C/OS-II,Vx works, embedded linux, tiny OS and	CLO 15	Study Case Studies 0f RTOS, RT linux
		CLO 16	Understand RT linux, Micro C/OS-II,Vx works, embedded linux

	basic concepts of android OS.	CLO 17	Study RT linux, Micro C/OS-II,Vx works, embedded linux, tiny OS.
		CLO 18	Examine tiny OS and basic concepts of android OS.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PEO's Mapped	Strength of Mapping
BESB22.01	CLO 1	Understanding the basic concept of UNIX/LINUX, overview of commands..	PO 1 PO 2	2
BESB22.02	CLO 2	Study of file I/O (open, create, close, lseek, read, write).	PO 2	2
BESB22.03	CLO 3	Examine the process control (fork, vfork, exit, wait, waitpid, exec).	PO 3	3
BESB22.04	CLO 4	Discuss the RTOS, history of OS, Scheduler, objects, services, characteristics of RTOS, defining a task.	PO 3 PO 4	3
BESB22.05	CLO 5	Understand asks states and scheduling, task operations, structure, synchronization, Communication.	PO 2 PO 3	2
BESB22.06	CLO 6	Examine the concurrency, defining Semaphores, operations and use.	PO 4	3
BESB22.07	CLO 7	Describe the defining message Queue, states, content, storage, operations and use..	PO 3	3
BESB22.08	CLO 8	Study the Objects, Services AND I/O, Pipes, event registers, and signals.	PO 1	3
BESB22.09	CLO 9	Study the other building blocks, component configuration.	PO 1 PO 2	2
BESB22.10	CLO 10	Describe the Basic I/O concepts, I/O subsystem..	PO 1 PO 3	3
BESB22.11	CLO 11	Understand Exceptions, Interrupts and Timers, Exceptions, interrupts.	PO 1 PO 2	2
BESB22.12	CLO 12	Study applications, processing of exceptions and spurious interrupts.	PO 2	2
BESB22.13	CLO 13	Describe real time clocks, programmable timers, timer interrupt.	PO 4	3
BESB22.14	CLO 14	Understand the Service routines, soft timers, operations.	PO 3 PO 4	2
BESB22.15	CLO 15	Study Case Studies 0f RTOS, RT linux.	PO 2 PO 3	3
BESB22.16	CLO 16	Understand RT linux, Micro C/OS-II,Vx works, embedded linux	PO 3 PO 4	2
BESB22.17	CLO 17	Study RT linux, Micro C/OS-II,Vx works, embedded linux, tiny OS.	PO 2 PO 3	2
BESB22.18	CLO 18	Examine tiny OS and basic concepts of android OS.	PO 3 PO 4	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 4
CO 1	3	2	3	
CO 2	3	2	3	3
CO 3	3		3	3
CO 4	3	2	3	
CO 5	3	2		3

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Learning Outcomes (CLOs)	Program Outcomes (PO)			
	PO 1	PO 2	PO 3	PO 4
CLO 1	3	2		
CLO 2		2		
CLO 3			3	
CLO 4			3	
CLO 5		2	3	
CLO 6		2	3	
CLO 7			3	
CLO 8	3			
CLO 9	3	2		
CLO 10	3		3	
CLO 11	3	2		
CLO 12		2		
CLO 13			2	
CLO 14			2	
CLO 15				
CLO 16		2		
CLO 17		2		
CLO 18		2		

3 = High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES –DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 3 PO 4	Seminar and Term Paper	PO 1, PO 2 PO 3, PO 4
Viva	-	Mini Project	-	Laboratory Practices	-

XIII. ASSESSMENT METHODOLOGIES -INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

Unit-I	**INTRODUCTION :**
Introduction to UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write), process control (fork, vfork, exit, wait, waitpid, exec).	
Unit-II	**REAL-TIME OPERATING SYSTEMS :**
Brief history of OS, defining RTOS, Scheduler, objects, services, characteristics of RTOS, defining a task, asks states and scheduling, task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue, states, content, storage, operations and use.	
Unit-III	**OBJECTS, SERVICES AND I/O :**
Pipes, event registers, signals, other building blocks, component configuration. Basic I/O concepts, I/O subsystem	
Unit-IV	**EXCEPTIONS, INTERRUPTS AND TIMERS :**
Exceptions, interrupts, applications, processing of exceptions and spurious interrupts, real time clocks, programmable timers, timer interrupt service routines, soft timers, operations.	
Unit-V	**CASE STUDIES OF RTOS :**
RT linux, Micro C/OS-II, Vx works, embedded linux, tiny OS and basic concepts of android OS.	
Text Books:	
5. Qing Li, “Real Time Concepts for Embedded Systems”, Elsevier, 1st Edition, 2011	
Reference Books:	
1. Rajkamal, “Embedded Systems, Architecture, Programming and Design”, Tata Mc Graw Hill, 2nd Edition, 2003. 2. Richard Stevens, “Advanced UNIX Programming”, Addison-Wesley Professional, 3rd Edition, 2013 3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, Addison Wesley, 1st Edition, 2002	
Web References:	
1. http://nptel.ac.in/courses/106105036/ 2. https://www.youtube.com/watch?v=rpdygqOI9mM 3. https://www.youtube.com/watch?v=hELr9-7aAG8	
E-Text Books:	
1. www.nptel.ac.in/courses/108105057/Pdf/Lesson-31.pdf 2. www. nptel.ac.in/courses/106108101/pdf/Lecture_Notes/Mod%208_LN.pdf	

XV. COURSE PLAN:

The course plan is meant as a guideline. There may probably be changes.

Lecture No	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write),	UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write),	T2:3.1 to 3.7
4-6	Introduction to process control (fork, vfork, exit, wait, waitpid, exec).	Introduction to process control (fork, vfork, exit, wait, waitpid, exec).	T2:3.1 to 3.7
7-9	Examine the to process control-fork, vfork, exit, wait, waitpid, exec..	process control- fork, vfork, exit, wait, waitpid, exec..	T2:8.1 to 8.17
10-13	Discuss the Real-Time Operating Systems , Brief history of OS, defining RTOS, Scheduler	Real-Time Operating Systems , Brief history of OS, defining RTOS, Scheduler	T1:8.1 to 8.11
14-16	Describe the objects, services, characteristics of RTOS, defining a task, asks states and scheduling	objects, services, characteristics of RTOS, defining a task, asks states and scheduling	T1:8.1 to 8.11
17-20	Study the task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue,	task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue,	T1:9.1 to 9.6 T1:10.1 to 10.5
21-24	Study the states, content, storage, operations and Pipes, event registers, signals, other building blocks, component configuration.	states, content, storage, operations and Pipes, event registers, signals, other building blocks, component configuration.	T1:13.1 to 13.6
25-28	Understand Basic I/O concepts, I/O subsystem	Basic I/O concepts, I/O subsystem	T1:13.1 to 13.6
29-32	Understand Exceptions, interrupts, applications, processing of exceptions and spurious interrupts	Exceptions, interrupts, applications, processing of exceptions and spurious interrupts	T1:13.1 to 13.6
33-36	Study the programmable timers, timer interrupt service routines, soft timers, operations.	timer interrupt service routines, soft timers, operations.	T1:11.1 to 11.3
37-40	Analyze RT linux, Micro C/OS-II, Vx works, embedded linux,	RT linux, Micro C/OS-II, Vx works, embedded linux,	T1:9.1 to 9.3
41-45	Examine the embedded linux, tiny OS and basic concepts of android OS.	embedded linux, tiny OS and basic concepts of android OS.	T1:13.1 to 13.6

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance with POs
1	Design of Sensor network scenarios	Seminars / NPTEL	PO 1, PO 3, PO 4
2	OS programming technology	Seminars / Guest Lectures / NPTEL	PO 3, PO 4
3	Low-Power Networking Systems	Laboratory Practices	PO 3, PO 4

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ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**RESEARCH METHODOLOGY AND IPR**				
Course Code	**BCSB31**				
Programme	**M.Tech**				
Semester	**III**				
Course Type	**Core**				
Regulation	**R18**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	2	**-**	**2**	**-**	**-**
Course Faculty	**Dr. P. Ashok Babu ,Professor**				

I. COURSE OVERVIEW:

Fundamental of Research Methodology and Data Collection is an excellent book that has a collection of basic concepts and terminologies in research method. It is filled with good ideas and tips on how to write very good articles that are fit for publication in reputable journals. The author has tried to identify problems encountered by young researchers and also proffered solutions to those problems. Detailed write-up on sampling techniques and sample size determination were well written and demonstrated in an excellent manner.It is also recommended to staff and students of all tertiary institutions especially those that want to learn how to become their best in research.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	-	-	Probability And Statistics	-

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Research Methodology and IPR	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	LCD / PPT	✔	Seminars	✔	Videos	✔	MOOCs
✔	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the experiments is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations and the term paper with overview of topic are conducted during II semester. The evaluation of technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems	3	Seminar and Term paper
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	3	Guest Lecture
PO 4	**Conduct investigations of complex problems:** Use researchbased knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to providevalid conclusions..	3	Seminar and Term paper
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	3	Seminar and Term paper
PO 6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	3	Seminar and Term paper

3 = High; 2 = Medium; 1 = Low

VII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Identify an appropriate research problem in their interesting domain.
II	Organize and conduct research project.
III	Understand the Preparation of a research project thesis report.
IV	Understand the law of patent and copyrights.
V	Understand the Adequate knowledge on IPR

VIII. COURSE OUTCOMES (COs):

Cos	Course Outcomes	CLOs	Course Learning Outcomes
CO1	Understand the research process and formulate the research problem	CLO1	Understand The Different Approaches of Research
		CLO2	Understand the features of good design, types of research design
CO2	Illustrate various measurement, scaling and estimate hypotheses values in research	CLO3	Understand the forecasting techniques and scale construction techniques
		CLO4	understand the time series analysis, interpolation and extrapolation;

CO3	Explore on various data collection methods and professional attitude, goals and ethics	CLO5	understand the collection of secondary data, cases and schedules .
		CLO6	Professional attitude and goals, concept of excellence, ethics in science and engineering
		CLO7	understand the participation in public debates on scientific issues
		CLO8	understand the famous frauds in science, and case studies.
CO4	Prepare a well-structured research paper and scientific presentations	CLO9	understand the techniques of interpretation, and making scientific presentation
		CLO10	understand the patent laws, patent and searching process.
CO5	Explore on various IPR components and process of filing	CLO11	understand the importance of intellectual property rights.
		CLO12	understand the rights to perform the, copy right ownership issues.

IX. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
BCSB31.01	CLO 1	Understand The Different Approaches of Research	PO1,PO2	3
BCSB31.02	CLO 2	Understand the features of good design, types of research design,	PO 1 PO2	3
BCSB31.03	CLO 3	Understand the forecasting techniques and scale construction techniques	PO 2, PO4	3
BCSB31.04	CLO 4	understand the time series analysis, interpolation and extrapolation;	PO1,PO 2 &PO4	3
BCSB31.05	CLO 5	understand the collection of secondary data, cases and schedules .	PO2,PO5	2
BCSB31.06	CLO 6	Professional attitude and goals, concept of excellence, ethics in science and engineering	PO1,PO5	3
BCSB31.07	CLO 7	understand the participation in public debates on scientific issues	PO 1,PO3	3
BCSB31.08	CLO 8	understand the famous frauds in science, and case studies.	PO1,PO4 & PO6	3
BCSB31.09	CLO 9	understand the techniques of interpretation, and making scientific presentation	PO4,PO5 &PO6	3
BCSB31.10	CLO 10	understand the patent laws, patent and searching process,	PO4,PO5, &PO6	2
BCSB31.11	CLO 11	understand the importance of intellectual property rights;	PO 5,PO6	3
BCSB31.12	CLO 12	understand the rights to perform the, copy right ownership issues	PO 5,PO6	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes				
	PO1	PO2	PO4	PO5	PO6
CO 1	3	3			
CO 2	3	3	3		
CO 3	3		3	3	
CO 4			3	3	3
CO 5				3	3

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1,PO 2 , PO4, PO5, PO6	SEE Exams	PO 1,PO 2 , PO4, PO5, PO6	Seminars and term paper	PO 6
VIVA	-	Student Viva	-	Mini Project	-

XII. ASSESSMENT METHODOLOGIES – INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

UNIT-I	**MEANING OF RESEARCH PROBLEM**	**Classes: 09**
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.		
UNIT-II	**LITERATURE STUDIES**	**Classes: 09**
Effective literature studies approaches, analysis Plagiarism, and Research ethics.		
UNIT-III	**TECHNICAL WRITING**	**Classes: 09**
Effective technical writing, how to write report, Paper Developing a Research Proposal. Format of research proposal, a presentation and assessment by a review committee.		
UNIT-IV	**NATURE OF INTELLECTUAL PROPERTY**	**Classes: 09**
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.		
UNIT-V	**PATENT RIGHTS AND NEW DEVELOPMENTS IN IPR**	**Classes: 09**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topic Outcomes	Topic/s to be covered	Reference
1	Understand the concept of types of research	Definition, types of research	T1:2.1
2	Understand the various Research Approaches	Research Approaches	T1:2.3
3	understand Research process, validity and reliability in research	Research process, validity and reliability in research	T1:2.3.1
4	understand the Features of good design	Features of good design	T1:7.2
5	Understanding the Types of research design	Types of research design	T1:7.3
6	Understand the Basic principles of experimental design	Basic principles of experimental Design	T1:7.4
7	Understand the various types Errors in measurement	Errors in measurement	T1:7.5
8-9	Understand the tests of sound measurement	tests of sound measurement	T1:8.1
10-11	Understand the scaling and scale construction techniques	scaling and scale construction techniques	T1:8.2
12-13	Understand the forecasting techniques	Forecasting techniques	T1:8.3
14	Understand the concept of time series analysis	time series analysis	T1:8.4
15	Interpolation and extrapolation	Interpolation and extrapolation.	T1:8.5
16	understand the Primary data, questionnaire and interviews	Primary data, questionnaire and interviews	T1:8.6
17-18	Understand the collection of secondary data, cases and schedules	collection of secondary data, cases and schedules	T1:9.1
19	understand the Professional attitude and goals	Professional attitude and goals	T1:9.2, 9.3
20	Understanding the scheduling in DOS concept of excellence	concept of excellence	T2:9.3.4
21	Understand real time OS in DOS environment	ethics in science and engineering	T1:9.5
22	Understand the some famous frauds in science	some famous frauds in science	T2:7.1
23	Understand the Case studies	Case studies	T2:7.2
24	Understand the Layout of a research paper	Layout of a research paper	T2:7.3
25	techniques of interpretation	techniques of interpretation	T2:7.4

26	Understand techniques of interpretation	techniques of interpretation	T2:8.3
27	Understand the making scientific presentation at conferences	making scientific presentation at conferences	T2:8.4
28	Understand the popular lectures to semi technical audience	popular lectures to semi technical audience	T3:8.5
29	Understand the participating in public debates on Scientific issues	participating in public debates on Scientific issues.	T3:8.6
30	Understand the types of intellectual property	Introduction, types of intellectual Property	T3:10.7
31	Understand the international organizations ,agencies and treaties	international organizations ,agencies and treaties	T3:10.8
32	Understand the importance of intellectual property rights	importance of intellectual property rights;	T3:10.9
33	understand the Law of copy rights, rights of reproduction	Law of copy rights: Fundamental of copy right law, originality of material, rights of reproduction	T3:11.7
34	understand the rights to perform the work publicly, copy right ownership issues	rights to perform the work publicly, copy right ownership issues	T3:11.7.1
35	understand copy right registration, notice of copy right	copy right registration, notice of copy right	T3:11.7.2
36	understand the international copy right law; Law of patents: Foundation of patent law, patent searching process,	international copy right law; Law of patents: Foundation of patent law, patent searching process,	T3:11.8
37	understand the ownership rights and transfer	ownership rights and transfer	T3:12.1-2

XIV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S NO	Description	Proposed actions	Relevance with POs
1	Knowledge on research problems.	Seminars/NPTEL	PO 2,PO 4

Prepared by:
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