INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE**				
Course Code	AEC507				
Programme	B.Tech				
Semester	VIII	ECE			
Course Type	Elective				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Chief Coordinator	**Ms. C Devisupraja, Assistant Professor**				

I. COURSE OVERVIEW:

Digital Signal Processing (DSP) is being used very widely in applications that include telecommunication equipment, multimedia systems, electronic and bio-medical instrumentation, automotive systems and many military and weapon systems. DSP chips, general processors or dedicated ASIC chips, are now able to process wide bandwidth signal of all sorts in real-time. Digital Signal Processors take real-world signals like voice, audio, video, temperature, pressure, or position that have been digitized and then mathematically manipulate them. DSPA is designed for performing mathematical functions like "add", "subtract", "multiply" and "divide" very quickly.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC013	VI	Micro processors and Micro controllers	4
UG	AEC012	VI	Digital Signal Processing	4

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital Signal Processors and Architectures	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✔	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Quiz
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	3	Assignments
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Mini Project
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and researchmethods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Seminars / Mini Project

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Seminars and Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Quiz and Assignments

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors.
II	Learn the architectural differences between DSP and General purpose processor.
III	Learn about interfacing of serial & parallel communication devices to the processor.
IV	Implement the DSP & FFT algorithms.

IX. COURSE OUTCOMES (COs):

Cos	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the basics of Digital Signal Processing and transforms.	CLO 1	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.
		CLO 2	Understand the inter-relationship between DFT and various transforms.
		CLO 3	Understand the IEE-754 floating point and source of errors in DSP implementations .
		CLO 4	Understand the fast computation of DFT and appreciate the FFT Processing.
CO 2	Able to distinguish between the architectural features of General purpose processors and DSP processors.	CLO 5	Understand the concept of multiplier and multiplier Accumulator.
		CLO 6	Design SMID ,VLIW architectures
		CLO 7	Understand the modified bus structures and memory access in PDSPs.
		CLO 8	Understand the special addressing modes in PDSPs.
CO 3	Understand the architectures of TMS320C54xx devices.	CLO 9	Understand the architecture of TMS320C54XX DSPs
		CLO 10	Understand the addressing modes and memory space of TMS320C54XX DSPs
		CLO 11	Understand the various interrupts and pipeline operation of TMS320C54XX processors.
		CLO 12	Analyze the Program control, instruction set and programming.
		CLO 13	Understand the concept of on-chip Peripherals.
CO 4	Discuss about various memory and parallel I/O interfaces.	CLO 14	Understand the significance of memory space organization
		CLO 15	Analyze external bus interfacing signals
		CLO 16	Explain about parallel I/O interface, programmed I/O
		CLO 17	Understand the significance of Interrupts and Direct Memory Access
CO 5	Discuss about various memory and parallel I/O interfaces.	CLO 18	Understand the basic concepts of convolution and correlation.
		CLO 19	Compare the characteristics of IIR and FIR filters

Cos	Course Outcome	CLOs	Course Learning Outcome
		CLO 20	Analyze the concepts of interpolation and decimation filters

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC013.01	CLO 1	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.	PO1	3
AEC013.02	CLO 2	Understand the inter-relationship between DFT and various transforms.	PO2	2
AEC013.03	CLO 3	Understand the IEE-754 floating point and source of errors in DSP implementations .	PO1	2
AEC013.04	CLO 4	Understand the fast computation of DFT and appreciate the FFT Processing.	PO2	1
AEC013.05	CLO 5	Understand the concept of multiplier and multiplier Accumulator.	PO2	3
AEC013.06	CLO 6	Design SMID ,VLIW architectures	PO3	3
AEC013.07	CLO 7	Understand the modified bus structures and memory access in PDSPs.	PO3	2
AEC013.08	CLO 8	Understand the special addressing modes in PDSPs.	PO1	2
AEC013.09	CLO 9	Understand the architecture of TMS320C54XX DSPs	PO3	3
AEC013.10	CLO 10	Understand the addressing modes and memory space of TMS320C54XX DSPs	PO4	2
AEC013.11	CLO 11	Understand the various interrupts and pipeline operation of TMS320C54XX processors.	PO1, PO2	2
AEC013.12	CLO 12	Analyze the Program control, instruction set and programming.	PO3	3
AEC013.13	CLO 13	Understand the concept of on-chip Peripherals.	PO3	2
AEC013.14	CLO 14	Understand the significance of memory space organization	PO3	2
AEC013.15	CLO 15	Analyze external bus interfacing signals	PO1	3
AEC013.16	CLO 16	Explain about parallel I/O interface, programmed I/O	PO1	2
AEC013.17	CLO 17	Understand the significance of Interrupts and Direct Memory Access	PO4	2
AEC013.18	CLO 18	Understand the basic concepts of convolution and correlation.	PO3	3
AEC013.19	CLO 19	Compare the characteristics of IIR and FIR filters	PO3	3
AEC013.20	CLO 20	Analyze the concepts of interpolation and decimation filters	PO3	3

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XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes	Program Outcomes (POs)				Program Specific Outcomes(PSOs)	
	PO1	PO2	PO 3	PO4	PSO 1	PSO 2
CO 1	3	2				
CO 2	2	3	3		2	
CO 3	2	2	3	2		2
CO 4	3		2	2	2	
CO 5			3			2

XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3														
CLO 2		2											1	3	
CLO 3	2												2		
CLO 4		2												3	
CLO 5		3												3	
CLO 6			3											2	
CLO 7			3											2	
CLO 8	2												3		
CLO 9			3										1		
CLO 10				2										3	
CLO 11	2	2											2		
CLO 12			3											2	
CLO 13			2											2	
CLO 14			2										2		
CLO 15	3												3		

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 16	2												2		
CLO 17				2										2	
CLO 18			3											1	
CLO 19			3											1	
CLO 20			3										2		

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO 1,PO 2, PO 3, PO4, PSO 1, PSO 2	SEE Exams	PO 1,PO 2, PO 3,PO 4, PSO 1, PSO 2	Assignments	-	Seminars	PO1,PO2, PO3,PO4, PSO 1, PSO 2
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 1,PO 2, PO 3, PO4, PSO 1, PSO 2						

XIV. ASSESSMENT METHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

UNIT – I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING
Introduction: Digital signal-processing system, discrete Fourier Transform (DFT) and fast Fourier transform (FFT), differences between DSP and other micro processor architectures; Number formats: Fixed point, floating point and block floating point formats, IEEE-754 floating point, dynamic range and precision, relation between data word size and instruction word size; Sources of error in DSP implementations: A/D conversion errors, DSP computational errors, D/A conversion errors, Q-notation.
UNIT – II: ARCHITECTURE OF PROGRAMMABLE DSPs
Multiplier and multiplier accumulator, modified bus structures and memory access in PDSPs, multiple access memory, multiport memory, SIMD, VLIW architectures, pipelining, special addressing modes in PDSPs, on-chip peripherals.
UNIT – III: OVERVIEW OF TMS320C54XX PROCESSOR
Architecture of TMS320C54XX DSPs, addressing modes, memory space of TMS320C54XX processors. Program control, instruction set and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation.

UNIT – IV: INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs
Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA).
UNIT – V: IMPLEMENTATIONS OF BASIC DSP ALGORITHMS
The Q-notation, convolution, correlation, FIR filters, IIR filters, interpolation filters, decimation filters, an FFT algorithm for DFT filters computation of the signal spectrum.
Text Books:
1. Avtar Singh and S. Srinivasan, Digital Signal Processing‖ Thomson Publications, 1st Edition, 2004. 2. Lapsley et al, DSP Processor Fundamentals, Architectures & Features‖, S. Chand & Co, 1 st Edition, 2000. 3. B. Ventakaramani, M. Bhaskar, Digital Signal Processors Architecture Programming and Applications, Tata McGraw-Hill, 1st Edition, 2006.
Reference Books:
1. Jonatham Stein, Digital Signal Processing‖, John Wiley, 1st Edition, 2000. 2. Sen M. Kuo&WoonSergGan, Digital Signal Processors Architectures, Implementation and Application‖, Pearson Practice Hall, 1st Edition, 2013. 3. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, A Practical Approach to Digital Signal Processing‖, New Age International, 1 st Edition, 2006. 4. Ifeachor E. C., Jervis B. W, Digital Signal Processing: A practical approach‖, Pearson Education, PHI/, 2nd Edition, 2002. 5. Peter Pirsch ,Architectures for Digital Signal Processing‖, John Weily, 1 st Edition, 2007.
Web References:
1. http://www.nptel.ac.in/

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Introduction To Digital Signal Processing	CLO 1	T3:2.1
2	Discrete Fourier Transform (DFT)	CLO 1	T3:2.1
3	Fast Fourier Transform (FFT)	CLO 1	T3:1.2
4	Differences Between DSP And Other Micro Processor Architectures	CLO 1	T3:1.1,1.2.2
5	Number Formats: Fixed Point, Floating Point And Block Floating Point Formats	CLO 2	T3:1.4
6	Number Formats: Fixed Point, Floating Point And Block Floating Point Formats	CLO 2	T3:1.3,1.8, 1.9
7	IEEE-754 Floating Point	CLO 1	T3:2.1
8	Dynamic Range And Precision	CLO 2	T3:2.2
9	Relation Between Data Word Size And Instruction Word Size	CLO 3	T3:2.3

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
10	Sources Of Error In DSP Implementations:	CLO 4	T3:2.4 T1:5.1-5.20
11	A/D Conversion Errors	CLO 4	T3:2.4 T1:5.1-5.20
12	DSP Computational Errors	CLO 4	T3:2.4 T1:5.1-5.20
13	D/A Conversion Errors, Q-Notation	CLO 4	T3:5.4
14	Multiplier And Multiplier Accumulator	CLO 4	T3:5.5
15	Modified Bus	CLO 4	T1:9.19 T3: 5.8
16	Memory Access In Pdsps	CLO 5	T3:5.7,5.6
17	Multiple Access Memory,	CLO 5	T3:5.1
18	Multiport Memory	CLO 5	T1-8.1,T1-8.7
19	Simd	CLO 5	T3:6.4.3 T1:14.9,14 .48
20	VLIW Architectures	CLO 8	T3:6.4,6.4 4
21	Pipelining	CLO 8	R3:2.1
22	Special Addressing Modes In PDSPs	CLO 9	R3:2.1
23	Special Addressing Modes In PDSPs	CLO 9	T3:1.2
24	On-Chip Peripherals.	CLO 9	T3:1.1
25	On-Chip Peripherals.	CLO 9	T3:1.4
26	Architecture Of TMS320C54XX DSPs	CLO 9	T3:1.3,1.8, 1.9
27	Addressing Modes	CLO 9	T3:2.1
28	Memory Space Of TMS320C54XX Processors	CLO 9	T3:2.2
29	Program Control, Instruction Set	CLO 13	T3:2.3
30	Instruction Set And Programming	CLO 13	T3:2.4T1:5 .1-5.20
31	On-Chip Peripherals	CLO 9	T3:2.4, T1:5 .1-5.20
32	Interrupts Of TMS320C54XX Processors	CLO 11	T3:2.4T1:5 .1-5.20
33	Interrupts Of TMS320C54XX Processors	CLO 11	T3:2.4T1:5 .1-5.20
34	Pipeline Operation.	CLO 12	T3:2.4T1:5 .1-5.20
35	Memory Space Organization	CLO 9	T3:5.4
36	External Bus Interfacing Signal	CLO 9	T3:5.5

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
37	Memory Interface	CLO 14	T2:3.1
38	Parallel I/O Interface	CLO 14	T2:3.1
39	Programmed I/O,	CLO 15	T2:3.2
40	Interrupts And I/O	CLO 15	T2:3.3
41	Direct Memory Access (DMA).	CLO 15	T2:5.1
42	The Q-Notation, Convolution, Correlation,	CLO14	T2:6.1,6.6,7.1 7.6, 8.1 -8.3
43	FIR Filters	CLO19	T2:6.1 to 6.6,7.1 to 7.6,
44	IIR Filters	CLO 19	T2:3.6
45	Interpolation Filters, Decimation Filters,	CLO 20	T2:3.4
46	An FFT Algorithm For DFT Filters	CLO 17	T2:3.6,3.4 R5:24.5- 24.7
47	Computation Of The Signal Spectrum.	CLO 20	T2:3.6,3.4 R5:24.5- 24.7

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. NO	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POs	RELEVANCE WITH PSOs
1	System on Chip	Seminars / NPTEL	PO 1, PO 2, PO 4	PSO 1

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