INSTITUTE OF AERONAUTICAL ENGINEERING

Dundigal, Hyderabad - 500 043

INFORMATION TECHNOLOGY

COURSE DESCRIPTION FORM

Course Title	**Digital Logic Design and Computer Organization**			
Course Code	A30402			
Course Structure	**Lectures**	**Tutorials**	**Practicals**	**Credits**
	4	1	-	4
Course Coordinator	**Mr. E. Sunil Reddy, Assistant Professor, IT**			
Team of Instructors	**Mr. E. Sunil Reddy, Assistant Professor, IT**			

I. COURSE OVERVIEW:

This course helps to get good knowledge in logic design can enable an engineer to recognize, formulate and solve many digital problems. It also helps in analyzing, designing and processing digital data. It deals with different operational units of computer and their interconnections. It gives a detailed description about layered view of computer system. It also helps in understanding function and structure of a computer, functional components of a computer, interconnection of components and performance of a computer.

II. PREREQUISITE(S):

Level	Credits	Periods	Prerequisite
UG	4	5	IT Workshop lab, Basic Mathematics

III. MARKS DISTRIBUTION

Sessional Marks	University End Exam Marks	Total Marks
There shall be 2 midterm examinations. Each midterm examination consists of subjective test. The subjective test is for 20 marks, with duration of 2 hours. Subjective test of each semester shall contain 5 one mark compulsory questions in part-A and part-B contains 5 questions, the student has to answer 3 questions, each carrying 5 marks. First midterm examination shall be conducted for the first two and half units of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. There shall be two assignments in every theory course. Marks shall be awarded considering the average of two assignments in each course.	75	100

IV. EVALUATION SCHEME:

1.	I Mid Examination	80 minutes	20
2.	I Assignment	-	5
3.	II Mid Examination	80 minutes	20
4.	II Assignment	-	5
5.	External Examination	3 hours	75

V. COURSE OBJECTIVES:

I. **Explain** the basic concepts like number systems including binary numbers and Boolean algebra principles.
II. **Apply** Boolean algebra to switching logic design and simplification.
III. **Discuss** about circuit layouts using logic gates, multiplexers, decoders, registers, counters, programmable logic arrays.
IV. **Explain** about flip-flops, counters, registers, shift registers.
V. **Understand** about synchronous and asynchronous sequential circuits.
VI. **Discuss** about memory, ROM, RAM, PLA and PAL.
VII. **Apply** methods of K-Maps and gate level simplifications.
VIII. **Identify** the basic components of computers.
IX. **Describe** the factors involved in Instruction set architecture design.
X. **Discuss** the Input-Output organization in depth
XI. **Explore** the memory Organization Techniques.

VI. COURSE OUTCOMES:

At the end of the course the students are able to:

1. **Understand** number systems, binary addition and subtraction, 2's complement representation and operations with this representation.
2. **Discuss** about digital logic gates and their properties.
3. **Explain** switching algebra theorems and apply them for logic functions.
4. **Identify** the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
5. **Evaluate** functions using various types of minimizing algorithms like Boolean algebra, Karnaugh map or Tabulation Method.
6. **Understand** bi-stable elements and different types of latches, flip-flops.
7. **Analyze** the design procedures of Combinational and Sequential logic circuits.
8. **Understand** the Computer Arithmetic and different types of operations.
9. **Analyze** memory organizations, PAL, PLA and memory hierarchy concepts..
10. **Differentiate** Instruction formats classification based on number of operands, size of instruction, an**d** way of accessing the data.
11. **List** the conditional Jump instructions using Flag register bits information and using the CMP instruction outcome.
12. **Explain** the interrupts Vectored and non vectored, Processor and I/O, Hardware and software in detail.
13. **Explain** different synchronous and asynchronous data transfer techniques.
14. **Explain** different I/O data transfer techniques with performance comparison.
15. **Differentiate** I/O mapped I/O and memory mapped I/O.
16. **Explain** the communication between I/O devices and IOP and Processor.
17. **Explain** the Memory Hierarchy and performance and cost comparison of different types of memory.

18. **Describe** how the data is transferred from virtual memory to Cache memory.
19. **Explain** cache memory mapping techniques and compare.

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program outcomes		Level	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, Engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	S	Assignments, Tutorials
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and Engineering sciences.	N	Assignments
PO3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	H	Assignments
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to Provide valid conclusions.	H	Projects
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the Limitations.	N	Mini Projects
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering Practice.	S	-----
PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, And demonstrate the knowledge of, and need for sustainable development.	S	-----
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	N	-----
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	S	-----
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design	S	-----

	Documentation, makes effective presentations, and give and receive clear instructions.		
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	N	-----
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest Context of technological change.	S	Projects

N - None **S - Supportive** **H - Highly Related**

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency Assessed by
PSO1	**Professional Skills:** The ability to research, understand and implement computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient analysis and design of computer-based systems of varying complexity.	H	Lectures and Assignments
PSO2	**Problem-solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	S	Tutorials
PSO3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	S	Seminars and Projects

N - None **S - Supportive** **H - Highly Related**

IX. SYLLABUS:

Unit I

Basic Structure of Computers: Computer Types, Functional units, Basic operational concepts, Bus structures, Software, Performance, multiprocessors and multi computers, Computer Generations.

Data Representation: Binary Numbers, Fixed Point Representation .Floating Point Representation. Number base conversions, Octal and Hexadecimal Numbers, components, Signed binary numbers, Binary codes.

Unit II

Digital Logic Circuits-I: Basic Logic Functions, Logic gates, universal logic gates, Minimization of Logic expressions. Flip-flops, Combinational Circuits.

Digital Logic Circuits-II: Registers, Shift Registers, Binary counters, Decoders, Multiplexers, Programmable Logic Devices.

Unit III

Computer Arithmetic: Algorithms for fixed point and floating point addition, subtraction, multiplication and division operations. Hardware Implementation of arithmetic and logic operations, High Performance arithmetic. **Instruction set & Addressing:** Memory Locations and Addresses, Machine addresses and sequencing, Various Addressing Modes, Intrusion Formats, Basic Machine Instructions,IA-32 Pentium example.

Unit IV

Processor Organization: Introduction to CPU, Register Transfers, Execution of Instructions, Multiple Bus Organization, Hardwired Control, Micro programmed Control.

Memory Organization: Concept of Memory, RAM,ROM memories, memory hierarchy, cache memories, virtual memory, secondary storage, memory management requirements.

Unit V

Input / Output Organization: Introduction to I/O, Interrupts- Hardware, Enabling and disabling Interrupts, Device Control, Direct memory access, buses, interface circuits, standard I/O Interfaces.

TextBooks

Computer Organization – Carl Hamacher, Zvonko Vranesic, Safwat Zaky, fifth edition, McGraw Hill.

Computer Architecture and Organization- An Integrated Approach, Miles Murdocca Vincent Heuring, Second Edition, Wiley India.

Computer Systems Architecture – M.Moris Mano, IIIrd Edition, Pearson.

References

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson
2. Computer- organization and Design- David A. Paterson and John L.Hennessy-Elsevier.
3. Fundamentals or Computer Organization and Design, - Sivarama Dandamudi Springer ed.
4. Digital Design – Third Edition, M.Morris Mano, Pearson Education/PHI.
5. Fundamentals of Logic Design, Roth, 5th Edition, Thomson.

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following course learning outcomes

Lecture No.	Course Learning Outcomes	Topics to be covered	Reference
1	Understand the need for digital systems	Introduction to Digital Logic Design and Computer Organization.	T3:1-4
2	**Understand** Basic Structure of Computers	Computer Types	T1:2-4
3	**Understand** Basic Structure of Computers	Functional units	T1:2-4

4	**Learn** operational concepts in computer	Basic operational concepts	T1:7-8
5	**Understand** Bus Structures and **Analyze** the concepts of Software	Bus structures, Software	T1:9-12
6	**Understand** Computer Performance	Performance	T1:13-18
7	**Discuss** Multiprocessors and Multicomputer, Know the Computer Generations	Multiprocessors and multi computers, Computer Generations	T1:18-19
8-9	**Discuss** about Data Representation	Binary Numbers	T3:68-73
10-11	**Understand** about Data Representation	Fixed Point Representation, Floating Point Representation	T3:71-83
12-13	**Discuss** about Data Representation	Number base conversions	T3:68-73
14	**Discuss** about Data Representation **and Understand** the complements	Octal and Hexadecimal Numbers, complements	T3:68-73
15	**Understand** Signed Binary Numbers	Signed binary numbers	T3:75-76
16	**Understand** Binary codes	Binary codes	T3:75-76
17-18	**Understand** Basic Logic Functions	Basic Logic Functions	T1:662
19	**Understand** the Logic Gates	Logic gates	T1:665
20	**Understand** universal logic gates	universal logic gates	T1:665
21-22	**Discuss** Minimization of Logic Expressions	Minimization of Logic expressions	T1:668-674
23-24	**Discuss** about FLIP-FLOPS	Flip-flops	T1:690-698
25	**Design** different combinational and sequential logic circuits.	Combinational Circuits	T3:20-24
26	**Learn** various Registers	Registers, Shift Registers	T3:50-55
27	**Discuss** about Binary Counters	Binary counters	T3:55-59
28-29	**Discuss** various types of Decoders	Decoders	T3:43-47
30	**Discuss** various types of Multiplexers	Multiplexers	T3:47-50
31	**Understand** Programmable Logic Devices	Programmable Logic Devices	T1:705-710

32	**Understand** Computer Arithmetic and hardware algorithm	Algorithm for fixed point addition, subtraction	T3:336-340
33-34	**Understand** the Multiplication of two fixed point numbers	Algorithm for fixed point multiplication	T3:342-348
35	**Understand** the division of two fixed point numbers	Algorithm for fixed point division	T3:350-355
36	**Understand** Computer Arithmetic and hardware algorithm	Algorithm for floating point addition, subtraction	T3:356-359
37	**Understand** the Multiplication and division of two floating point numbers	Algorithms for floating point multiplication and division operations	T3:361-364
38	**Discuss** Hardware Implementation of arithmetic and logic operations	Hardware Implementation of arithmetic and logic operations, High Performance arithmetic	T3:365-378
39	**Discuss** about Addresses and Memory Locations	Memory Locations and Addresses	T2:81-83
40	**Discuss** Machine Addresses and Sequencing	Machine addresses and sequencing	T2:85-56
41	**Discuss** Various Addressing Modes	Various Addressing Modes	T2:87-89
42	**Understand** Instruction Formats	Intrusion Formats	T2:90-92
43	**Understand** Instruction Formats	Basic Machine Instructions	T2:90-92
44-45	**Understand** IA-32 Pentium Example	IA-32 Pentium example	T1:155-185
46	**Learn** Introduction to CPU	Introduction to CPU	T1:411
47	**Understand** Register Transfers	Register Transfers	T1:415
48	**Understand** Execution of Instructions	Execution of Instructions	T1:411
49	**Discuss** Multiple Bus Organization	Multiple Bus Organization	T1:423
50	**Discuss** Hardwired Control	Hardwired Control	T1:425-428
51	**Discuss** Micro programmed Control	Micro programmed Control	T1:429-443
52	**Discuss** Concept of Memory	Concept of Memory	T1:291
53	**Discuss** RAM memories	RAM memories	T1:295-308
54	**Discuss** ROM memories	ROM memories	T1:309-

			313
55	**Understand** memory hierarchy, cache memories	memory hierarchy, cache memories	T1:314
56	**Discuss** cache memories	cache memories	T1:314-325
57-58	**Discuss** Virtual memory.	Virtual memory.	T1:337-339
59	**Discuss** secondary storage	secondary storage	T1:344-358
60	**Understand** memory management requirements	memory management requirements	T1:343
61	**Learn** Introduction to I/O	Introduction to I/O	T1:203
62-63	**Understand** Interrupts	Interrupts-Hardware, Enabling and disabling Interrupts	T1:208-211
64	**Discuss** Device Control	Device Control	T1:217
65	**Discuss** Direct memory access	Direct memory access	T1:234-237
66	**Discuss** Direct memory access, buses	Direct memory access, buses	T1:234-247
67	**Discuss** interface circuits	interface circuits	T1:248-257
68	**Understand** standard I/O Interfaces	standard I/O Interfaces	T1:259-272

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
I	H	H	N	N	N	N	N	N	N	N	N	S	H	S	N
II	S	H	H	N	N	N	N	N	N	N	N	N	H	S	N
III	N	H	S	S	N	N	N	N	N	N	N	N	S	H	N
IV	H	S	N	N	N	N	N	N	N	N	N	N	H	S	N
V	N	N	N	N	S	N	N	N	N	N	N	N	H	N	S
VI	N	H	H	N	S	N	N	N	N	N	N	N	H	S	S
VII	S	S	H	N	N	N	N	N	N	N	N	S	H	H	S

VIII	S	N	N	N	N	N	N	N	N	N	N	N	H	H	N
IX	S	N	H	N	S	N	N	N	N	N	N	S	S	H	N
X	S	S	N	N	N	N	N	N	N	N	N	S	H	S	N
XI	N	N	N	N	H	N	N	N	N	N	N	N	H	S	S

N=None **S - Supportive** **H - Highly Related**

XII MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Objectives	**Program Outcomes**											**Program Specific Outcomes**			
	PO 1	**PO 2**	**PO 3**	**PO4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO2**	**PSO3**
1	H	S	S	N	N	N	N	N	N	N	N	N	H	S	N
2	H	N	N	S	N	N	N	N	N	N	N	N	S	H	N
3	N	N	H	S	N	N	N	N	N	N	N	N	H	S	N
4	S	H	N	N	N	N	N	N	N	N	N	N	S	H	N
5	H	S	N	N	N	N	N	N	N	N	N	N	S	H	N
6	H	N	N	S	N	N	N	N	N	N	N	S	H	S	N
7	S	N	N	N	N	N	N	N	N	N	N	N	S	H	N
8	S	H	N	N	N	N	N	N	N	N	N	N	H	S	N
9	N	N	H	H	S	N	N	N	N	N	N	S	S	H	N
10	H	N	N	S	N	N	N	N	N	N	N	N	S	H	S
11	H	N	N	S	S	N	N	N	N	N	N	N	H	S	N
12	H	N	H	N	N	N	N	N	N	N	N	S	S	H	S
13	S	N	S	S	N	N	N	N	N	N	N	S	H	S	N
14	S	N	N	N	N	N	N	N	N	N	N	N	S	H	S
15	S	N	N	N	N	N	N	N	N	N	N	N	S	S	N
16	S	S	N	N	N	N	N	N	N	N	N	N	H	H	N
17	S	N	N	N	N	N	N	N	N	N	N	N	S	H	S
18	N	H	N	N	N	N	N	N	N	N	N	S	S	H	N
19	N	N	N	N	N	N	N	N	N	N	N	S	H	S	N

N=None **S=Supportive** **H=Highly Related**

Prepared by: Mr.E. Sunil Reddy, Assistant Professor, IT

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