INSTITUTE OF AERONAUTICAL ENGINEERING

Dundigal, Hyderabad - 500 043

COMPUTER SCIENCE AND ENGINEERING

COURSE DESCRIPTION FORM

Course Title	**COMPUTER ORGANIZATION**			
Course Code	A40506			
Regulation	**R13-JNTUH**			
Course Structure	Lectures	Tutorials	Practicals	Credits
	4	1	-	4
Course Coordinator	Ms.S.J.Sowjanya ,Assistant Professor			
Team of Instructors	Mr.K.Chiranjeevi, Ms.B.Tejeshwi			

I. COURSE OVERVIEW:

This course introduces the principles of computer organization and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O systems. It also deals with fundamentals of microprocessor, Assembly language programs. The main objective of this course is to examine how a computer operates at the machine level. It provides essential knowledge that are needed from engineering professionals to measure a simple PC performance. This course is presented to students by power point projections, lecture notes, course handouts, Assignments, Objective and subjective tests.

II. PREREQUISITES:

Level	Credits	Periods/Weeks	Prerequisites
UG	4	4	Basic Mathematics, Digital logic design, Basic concepts of Micro processor

III. COURSE ASSESSMENT METHODS:

a) Marks Distribution

Session Marks(25M)	University End Exam Marks	Total Marks
There shall be 2 midterm examinations. Each midterm examination consists of subjective type and objective type tests. The subjective test is for 10 marks, with duration of 1 hour. Subjective test of each semester shall contain 4 questions; the student has to answer 2 questions, each carrying 5 marks. The objective type test is for 10 marks with duration of 20 minutes. It consists of 10 multiple choice and 10 objective type questions, the student has to answer all the questions and each carries half mark. First midterm examination shall be conducted for the first two and half units of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. There shall be two assignments in every theory course. Marks shall be awarded considering the average of two assignments in each course.	**75**	**100**

IV. EVALUATION SCHEME:

S. No	Component	Duration	Marks
1	I Mid Examination	90 minutes	20
2	I Assignment	-	05
3	II Mid Examination	90 minutes	20
4	II Assignment	-	05
5	External Examination	3 hours	75

V. COURSE OBJECTIVES:

i. **Identify** the basic components of computers.

ii. **Describe** the factors involved in Instruction set architecture design.

iii. **Discuss** the Input-Output organization in depth.

iv. **Explore** the memory Organization Techniques.

v. **Discuss** pin description of 8086 microprocessor.

vi. **Illustrate** general instruction formats and addressing modes of 8086 microprocessor.

VI. COURSE OUTCOME:

1. **Differentiate** Instruction formats classification based on number of operands, size of instruction, and way of accessing the data?
2. **List** the conditional Jump instructions using Flag register bits information and using the CMP instruction outcome?
3. **Explain** the interrupts Vectored and non vectored, Processor and I/O, Hardware and software in detail?
4. **Explain** different synchronous and asynchronous data transfer techniques?
5. **Explain** different I/O data transfer techniques with performance comparison?
6. **Differentiate** I/O mapped I/O and memory mapped I/O?
7. **Explain** the communication between I/O devices and IOP and Processor?
8. **Explain** the Memory Hierarchy and performance and cost comparison of different types of memory?
9. **Draw** the memory map diagram to connect 16K RAM with each RAM Unit is 2K and the address range of RAM is 4FFF to 7FFF?
10. **Describe** how the data is transferred from virtual memory to Cache memory?
11. **Explain** cache memory mapping techniques and compare?
12. **Illustrate** the Pin diagram of 8086 with minimum and maximum mode operations?
13. **Explain** the architecture of 8086 with BIU and EU functionality with pipelining operation?
14. **Explain** the use of segmentation in 8086?
15. **Explain** the addressing modes of 8086?
16. **Explain** the conditional branch and call instructions?
17. **Explain** sorting algorithm and write the program using 8086 assembly language?

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Level	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	H	Assignments, Tutorials
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	H	Assignments
PO3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	S	Mini Projects
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	S	Projects
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	S	Mini Projects
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	N	--
PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	N	--
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	N	--
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	N	--
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	N	--
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	N	--
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	S	Projects

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO1	**Professional Skills:** The ability to research, understand and implement computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient analysis and design of computer-based systems of varying complexity.	H	Lectures, Assignments
PSO2	**Problem-solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	H	Projects
PSO3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	S	Guest Lectures

N - None S - Supportive H - Highly Related

IX. SYLLABUS:

UNIT-I

Basic computer organization-Functions of CPU, I/O Units, Memory, Instruction:

Instruction Formats-one address, two address, Zero address and three addresses and comparison; addressing modes with numeric examples: program control-Status bit conditions, conditional branch instructions, Program interrupts: Types of Interrupts.

UNIT-II

Input-Output organizations- I/O Interface, I/O Bus and Interface modules:

I/O Vs memory Bus , Isolated Vs Memory-Mapped I/O, Asynchronous data Transfer –strobe control ,Hand Shaking : Asynchronous Serial transfer-Asynchronous Communication interface , Modes of transfer Programmed I/O, Interrupt Initiated I/O,DMA; DMA controller, DMA Transfer, IOP-CPU-IOP Communication ,Intel 8089 IOP.

UNIT-III

Memory Organizations

Memory hierarchy ,Main Memory, RAM ,ROM Chips , Memory Address map, Memory Connection to CPU, associate memory ,cache Memory, Data cache ,Instruction cache, Miss and Hit ratio, Access time, associative ,set associative ,mapping, waiting into cache, Introduction to virtual memory

UNIT-IV

8086 CPU Pin Diagram – Special functions of general purpose registers, Segment register, Concept of pipelining, 8086 Flag register, Addressing modes of 8086.

UNIT-V 8086-instruction formats:

Assembly language programs involving branch & call instructions, sorting, evolving of arithmetic expressions.

TEXT BOOKS:

1. Morris Mano ," Computer system architecture:", Universities Press, 5e, 1992
2. Hall/A K Ray, "Advanced Micro Processor and Peripherals", PHI Learning

REFERENCES

1. William Stallings ,"Computer organization and architecture –sixth Edition", Pearson/PHI.
2. Andrew S.Tanenbaum,: Structured Computer Organization ", 4th Edition PHI/Pearson.
3. Sivaraama Dandamudi ,"Fundamentals or Computer Organization and Design", Springer Int.Edition.
4. john L.Hennessy and David A.Patterson ,"Computer Architecture a quantitative approach", ,Fourth Edition Elsevier.
5. Carl Hamacher, "Computer organization", fifth Edition,Mc Graw Hill

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following Course Learning Outcomes.

Lecture No.	Course Learning Outcomes	Topics to be covered	Reference
1-4	**Identify** different types of instructions and calculate their impact on performance of computer.	Instruction Formats, Comparison, Conditional Branch instructions	T1:8-4
5-6	**Understand** program control instructions using status bit conditions	program control- status bit conditions	T1:8-7
7-8	**Understand** different types of addressing modes used in an instruction.	Addressing Modes with numerical Examples	T1:8-5
9-12	**Ability to understand** interrupts and their impact on system performance.	Program Interrupts, Types of Interrupts	T1:8-7
13	**Identify** different ways of communicating with I/O devices and compare standard input-output interfaces.	I/O vs. memory Bus, Isolated vs. memory-mapped I/O	T1:11-2
14-20	**Understand** the concept of Asynchronous Transfers and modes of transfer.	Asynchronous Data Transfer, Asynchronous Serial transfer, Modes of Transfer	T1:11-3
21-23	**Describe** Speed of transfer using Direct Memory Access technique.	DMA	T1:11-6,R1:6-4
24-26	**Identify** Processor with Direct memory access capability and define Communication between CPU and IOP	Input-Output Processor(IOP),CPU-IOP, Intel 8089 IOP	T1:11-7,R1:6-9
27	**Understand** Asynchronous communication interface as both transmitter and receiver	Asynchronous Communication interface	T1:11-3
28-35	**Understand** the memory hierarchy and the function of RAM and ROM chips along with Connection between CPU and Memory	Memory Hierarchy, Main Memory, RAM and ROM Chips, Memory connection to CPU	T1:12-2
36-38	**Explain** Page table by means of Associative memory	Associative Memory	T1:12-4,R5:5.5
39-43	**Define** Cache memory and identify methods for specifying where memory blocks are placed in cache.	Cache Memory, Data Cache, Instruction Cache, Miss and Hit ratio, Access time	T1: 12-5, R5:5.5

Lecture No.	Course Learning Outcomes	Topics to be covered	Reference
44-47	**Know** the concept of virtual memory that involves defining address space .	Virtual memory, Memory Address map	T1:12-6, R5:5.7
48-53	**Learn** the configuration of pin diagram and Determine register organization with flag performance.	8086 CPU Pin Diagram, General purpose registers, Segment register, Flag register	T2: T1(1.1,1.2,1.3,1.4)
54-57	**Understand** the performance improvement using pipelining	Concept of Pipelining	T2:(4.1,4.2)
58-60	**Learn** the specifications of Addressing modes	Addressing Modes of 8086	T2:(2.2)
61-62	**Describe** different instruction formats	8086 Instruction formats	T2:(2.1,2.3)
63-64	**Understand** Assembly language programming and various types of instructions provided by 8086	Assembly Language programs involving Branch and call instructions	T2:(3.1,3.2)
65	**Identify** operations on arithmetic and sorting techniques.	Sorting, evaluation of arithmetic Expressions	T2(3.3,3.4)

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
I	H	H				H	H					S	H	S	
II	S	H	H										H	S	
III		H	S	S									S		
IV	H	S											H	S	
V					S								H		S
VI		H	H		S								H	S	S

S= Supportive H = Highly Related

XII. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	H	S	S			H	H						H	S	
2	H			S									S		
3			H		S								H	S	
4	S	H											S	H	
5	H	S											S	H	
6	H			S								S	H	S	

7	S			H									S	H	
8	S	H											H	S	
9			H	H	S							S	S	H	
10	H			S									S	H	S
11	H			S	S								H	S	
12	H		H									S	S	H	S
13															
14		S		S								S		S	
15	H			S											
16		S											S		S
17	S			S										S	S

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