INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

INFORMATION TECHNOLOGY

COURSE DESCRIPTOR

Course Title	**COMPUTER ORGANIZATION AND ARCHITECTURE**					
Course Code	**ACS004**					
Programme	B.Tech					
Semester	III	CSE	IT			
Course Type	Core					
Regulation	IARE - R16					
Course Structure	**Theory**			**Practical**		
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**	
	3	1	4	-	-	
Chief Coordinator	Mr.A.Praveen, Assistant Professor					
Course Faculty	Ms.A.Swapna, Assistant Professor					

I. COURSE OVERVIEW:

This course introduces the principles of basic computer organization, CPU organization, and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, register transfer languages, arithmetic, logic and shift micro operations, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O organization of computer, parallel processing and inter process communication and synchronization. This course in reached to student by power point presentations, lecture notes, and assignment questions ,previous model question papers, multiple choice questions and question bank of long and short answers.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC020	III	Digital Logic Design	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Computer Organization and Architecture	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Presentation on real-world problems
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignment
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	2	Seminar
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Seminar

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to research, understand and implement computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient analysis and design of computer-based systems of varying complexity.	1	Seminar
PSO 2	**Software Engineering Practices:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	-	-
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Understand the organization and architecture of computer systems and electronic computers.
II	Study the assembly language program execution, instruction format and instruction cycle.
III	Design a simple computer using hardwired and micro programmed control methods.
IV	Study the basic components of computer systems besides the computer arithmetic
V	Understand input-output organization, memory organization and management, and pipelining.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
CACS004.01	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.	PO 1	3
CACS004.02	CLO 2	Understand the interfacing concept with memory subsystem organization and input/output subsystem organization.	PO 1	3
CACS004.03	CLO 3	Understand instruction types, addressing modes and their formats in the assembly language programs.	PO 2	2
CACS004.04	CLO 4	Describe the instruction set architecture design for relatively simple microprocessor or Central Processing Unit.	PO 3	1
CACS004.05	CLO 5	Classify the functionalities of various micro operations such as arithmetic, logic and shift micro operations.	PO 3	2
CACS004.06	CLO 6	Understand the register transfer languages and micro operations involved in bus and memory transfers.	PO 2	2
CACS004.07	CLO 7	Describe the design of control unit with address sequencing and microprogramming Concepts.	PO 3, PO 4	1
CACS004.08	CLO 8	Understand the connections among the circuits and the functionalities in the hardwired control unit.	PO 2, PO 4	1
CACS004.09	CLO 9	Describe the various phases involved in the instruction cycle viz. fetching, decoding, reading effective address and execution of instruction.	PO 2	3
CACS004.10	CLO 10	Describe various data representations and explain how arithmetic and logical operations are performed by computers.	PO 4	1
CACS004.11	CLO 11	Classify the various instructions formats to solve the arithmetic expressions in different addressing modes.	PO 1, PO 4	1
CACS004.12	CLO 12	Understand the functionality of various instruction formats for writing assembly language programs.	PO 2	1
CACS004.13	CLO 13	Describe the implementation of fixed point and floating point addition, subtraction operations.	PO 1	3
CACS004.14	CLO 14	Understand the concept of memory hierarchy and different typed of memory chips.	PO 2	2
CACS004.15	CLO 15	Describe various modes of data transfer between CPU and I/O devices	PO 2, PO 3	1
CACS004.16	CLO 16	Understand the virtual memory concept with page replacement concept in memory organization	PO 2	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
CACS004.17	CLO 17	Describe the hardware organization of associate memory and understand the read and write operations	PO 1, PO 2	1
CACS004.18	CLO 18	Describe the parallel processing concept with multiple functional units.	PO 2	2
CACS004.19	CLO 19	Understand the multiprocessor concept with system bus structure and the concept of inter processor communication and synchronization.	PO 1	2
CACS004.20	CLO 20	Understand the different priority interrupts in the input-output organization in the computer architecture.	PO 1	2
CACS004.21	CLO 21	Possess the knowledge and skills for employability and to succeed in national and international level competitive examinations.	PO 2	1
CACS004.22	CLO 22	Possess the knowledge and skills to design advanced computer architecture for current industry requirements.	PO 1	1

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X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3												1		
CLO 2	3												1		
CLO 3		2													
CLO 4			1										1		
CLO 5			2										1		
CLO 6		2											1		
CLO 7			2	1											
CLO 8		2		1									1		
CLO 9		3													
CLO 10				1									1		
CLO 11	2			1									1		
CLO 12		1													
CLO 13	3												1		
CLO 14		2											1		

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 15		1	2										1		
CLO 16		2													
CLO 17	2	1											1		
CLO 18		2													
CLO 19	2												1		
CLO 20	2												1		
CLO 21		1													
CLO 22	1														

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XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1,PO 2, PO 3, PO 4	SEE Exams	PO 1,PO 2, PO 3, PO 4	Assignments	PO 2	Seminars	PO 3
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	-						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

Unit-I	INTRODUCTION TO COMPUTER ORGANIZATION
Basic computer organization, CPU organization, memory subsystem organization and interfacing, input or output subsystem organization and interfacing, a simple computer levels of programming languages, assembly language instructions, instruction set architecture design, a simple instruction set architecture.	
Unit-II	**ORGANIZATION OF A COMPUTER**
Register transfer: Register transfer language, register transfer, bus and memory transfers, arithmetic micro operations, logic micro operations, shift micro operations; Control unit: Control memory, address sequencing, micro program example, and design of control unit.	
Unit-III	**CPU AND COMPUTER ARITHMETIC**
CPU design: Instruction cycle, data representation, memory reference instructions, input-output, and interrupt, addressing modes, data transfer and manipulation, program control. Computer arithmetic: Addition and subtraction, floating point arithmetic operations, decimal arithmetic unit.	
Unit-IV	**INPUT-OUTPUT ORGANIZATION AND MEMORY ORGANIZATION**

Memory organization: Memory hierarchy, main memory, auxiliary memory, associative memory, cache memory, virtual memory; Input or output organization: Input or output Interface, asynchronous data transfer, modes of transfer, priority interrupt, direct memory access.	
Unit-V	**MULTIPROCESSORS**
Pipeline: Parallel processing, pipelining-arithmetic pipeline, instruction pipeline; Multiprocessors: Characteristics of multiprocessors, inter connection structures, inter processor arbitration, inter processor communication and synchronization.	
Text Books:	
1. M. Morris Mano, —"Computer Systems Architecture", Pearson, 3rd Edition, 2007. 2. John D. Carpinelli, —"Computer Systems Organization and Architecture", Pearson, 1st Edition, 2001. 3. Patterson, Hennessy, —"Computer Organization and Design: the Hardware/Software Interface", Morgan Kaufmann, 5th Edition, 2013.	
Reference Books:	
1. John. P. Hayes, —"Computer System Architecture", McGraw-Hill, 3rd Edition, 1998. 2. Carl Hamacher, Zvonko G Vranesic, Safwat G Zaky, —"Computer Organization", McGraw-Hill, 5th Edition, 2002. 3. William Stallings, —"Computer Organization and Architecture", Pearson Edition, 8th Edition, 2010.	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Basic Computer Organization	CLO 1	T1: 4.1-4.2
2-4	Memory Subsystem Organization And Interfacing, Input Or Output Subsystem Organization And Interfacing	CLO 2	T1: 4.3-4.4
5-7	Computer Levels Of Programming Languages, Assembly Language Instructions	CLO 3	T1: 3.1-3.2
8-12	Instruction Set Architecture Design, A Simple Instruction Set Architecture	CLO 4	T1: 3.3-3.4
13-15	Arithmetic Micro Operations, Logic Micro Operations	CLO 5	T2: 4.4-45
16-19	Control Unit: Control Memory, Address Sequencing	CLO 7	T2: 7.1-7.2
20-22	Design Of Control Unit	CLO 7	T2: 7.4
23	Data Representation	CLO 10	T2: 3.1-3.3
24-26	Memory Reference Instructions, Input- Output, And Interrupt	CLO 11	T2: 5.6-5.7
27-32	Addressing Modes, Program Control	CLO 11	T2: 8.5-8.7
33-35	Memory Reference Instructions, Data Transfer And Manipulation	CLO 12	T2: 8.6
36-38	Computer Arithmetic: Addition And Subtraction, Floating Point Arithmetic Operations	CLO 13	T2: 10.1-10.5
39-42	Memory Organization	CLO 14	T2: 12.1
43-45	Input Or Output Interface	CLO 15	T2: 11.2
46-48	Asynchronous Data Transfer, Modes Of Transfer	CLO 17	T2: 11.3-11.4
49	Priority Interrupt	CLO 20	T2: 11.5

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
50-51	Direct Memory Access	CLO 17	T2: 11.6
52-53	Pipeline: Parallel Processing	CLO 18	T2: 9.1-9.2
54	Instruction Pipeline	CLO 19	T2: 9.4
55-56	Multiprocessors	CLO 19	T2: 13.1
57-58	Inter Connection Structures	CLO 19	T2: 13.2
59-60	Inter Processor Arbitration	CLO 19	T2: 13.3

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S no	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Data Representation – Arithmetic multiplication , division	Seminars / Guest Lectures/ NPTEL	PO 1	PSO 1
2	RISC ,CISC Characteristics	Seminars / Guest Lectures/ NPTEL	PO 2	PSO 1
3	Vector Processing	Assignments	PO 1	PSO 1

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