INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	DIGITAL AND PULSE CIRCUITS				
Course Code	AEC019				
Programme	B.Tech				
Semester	IV	EEE			
Course Type	Foundation				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	4	-	3	-	-
Chief Coordinator	Dr. Vijay Vallabhuni, Associate Professor, ECE				
Course Faculty	Mrs. V. Bindusree, Assistant Professor, ECE				

I.   COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits. They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II.   COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC001	III	Electronic Devices and Circuits	4

III.   MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital and Pulse Circuits	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✔	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE):
The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz / Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Lectures, Assignments, Exercises
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Seminars, Lab related exercises
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	1	Assignments
PO 4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Five minute videos

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes (PSOs)	Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Lectures and Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	1	Seminars
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	2	Guest lectures

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Enrich the knowledge of probability on single random variables and probability distributions and apply the concept of correlation and regression to find covariance.
II	Analyze the given data for appropriate test of hypothesis and discuss the concept of sequential circuits and analyze sequential systems.
III	Interpret the concept of feedback and classify various types of feedback amplifiers and understand the principle of oscillation and design different types of oscillators.
IV	Design and analyze single stage and multi stage Amplifiers.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
CAEC019.01	CLO 1	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	PO 1 PO 2	2
CAEC019.02	CLO 2	Illustrate the switching algebra theorems and apply them for reduction of Boolean function.	PO 1 PO 2	2
CAEC019.03	CLO 3	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	PO 2	2
CAEC019.04	CLO 4	Discuss about digital logic gates and their properties, and implement logic gates using universal gates.	PO 2	2
CAEC019.05	CLO 5	Evaluate functions using various types of minimizing algorithms like Boolean algebra.	PO 1 PO 2	2
CAEC019.06	CLO 6	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	PO 2 PO 4	1
CAEC019.07	CLO 7	Design Gate level minimization using K-Maps and realize the Boolean function using logic gates.	PO 4	1
CAEC019.08	CLO 8	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	PO 3	1
CAEC019.09	CLO 9	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.	PO 3	1
CAEC019.10	CLO 10	Analyze and apply the design procedures of small sequential circuits to build the gated latches.	PO 2 PSO 2	2
CAEC019.11	CLO 11	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	PO 3	1
CAEC019.12	CLO 12	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 3	1
CAEC019.13	CLO 13	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 3	1
CAEC019.14	CLO 14	Understand the design analysis of feedback amplifiers & types of feedback circuits.	PO 2	2
CAEC019.15	CLO 15	Design various sinusoidal Oscillators like RC Phase shift, Wien bridge, Hartley and Colpitts oscillator for various frequency ranges.	PO 3	1
CAEC019.16	CLO 16	Analyze the design of BJT as single stage and multistage amplifier circuits.	PO 2	2
CAEC019.17	CLO 17	Implement the design analysis of coupling amplifiers and types of coupling circuits.	PO 2	2

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X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CAEC019.01	3	2												1	
CAEC019.02	3	2												1	
CAEC019.03		2												1	
CAEC019.04		2											3		
CAEC019.05	3	2												1	
CAEC019.06		2		1										1	
CAEC019.07				1										1	
CAEC019.08			1												
CAEC019.09			1												
CAEC019.10		2												1	
CAEC019.11			1											1	
CAEC019.12			1											1	
CAEC019.13			1										3		
CAEC019.14		2												1	
CAEC019.15			1												2
CAEC019.16		2													2
CAEC019.17		2												1	

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XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 2 PO 3, PO 4	Assignments	PO 1	Seminars	PO 2
Laboratory Practices	–	Student Viva	–	Mini Project	–	Certification	–
Term Paper	–						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Assessment of Course Outcomes (By Feedback, Once)	✔	Student Feedback on Faculty (Twice)	
✘	Assessment of Mini Projects By Experts			

XIII. SYLLABUS

Unit-I	BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS:
Introduction of binary numbers: Complements of numbers, codes, binary codes, binary code decimal code and its properties, unit distance codes, alpha numeric codes, error detecting and correcting codes;	

	Boolean algebra: Basic theorems and properties, switching functions, canonical and standard form.
Unit-II	**MINIMIZATION TECHNIQUES AND DESIGN OF MSI:**
	Minimization with theorem: Karnaugh map method, five variable map, prime and essential implications, don't care map entries, tabular method, partially specified expressions; combination all design: Arithmetic circuits, comparator, multiplexers, code converters, hazards and hazard free relations.
Unit-III	**SEQUENTIAL CIRCUITS DESIGN:**
	Basic differences between combinational and sequential logic circuits, binary cell, fundamentals of sequential machine operation, D Flip Flop, T Flip Flop, J K Flip Flop, design procedure for conversion of Flip Flops, conversion from one type of Flip-Flop to another, timing and triggering consideration, clock skew. Counters: Design of single mode counter, ripple counter, ring counter, shift register, shift register sequences, ring counter using shift register.
Unit-IV	**FEEDBACK AMPLIFIERS AND OSCILLATORS:**
	Feedback Amplifiers: Concepts of feedback, classification of feedback amplifiers, general characteristics of negative feedback amplifiers, effect of feedback on amplifier characteristics, voltage series, voltage shunt; Current series; Current shunt feedback configurations, illustrative examples; Oscillators: Classification of oscillators, condition for oscillations, RC phase shift oscillators; Generalized analysis of LC oscillators: Hartley and Colpitts oscillators, Wien Bridge and crystal oscillators, stability of oscillators.
Unit-V	**SINGLE STAGE AMPLIFIERS AND MULTISTAGE AMPLIFIERS**
	Single Stage Amplifiers: Classification of amplifiers, distortion in amplifiers, analysis of CE, CC and CB configurations with simplified hybrid model, analysis of CE amplifier with emitter resistance and emitter follower, Miller's theorem and its dual design of single stage RC coupled amplifier using BJT; Multistage amplifiers: Analysis of cascaded RC coupled BJT amplifiers, cascade amplifier, darlington pair, different coupling schemes used in amplifiers RC coupled amplifiers, transformer coupled amplifier, direct coupled amplifier.
Text Books:	
	1. M Morris Mano, Michael D Ciletti, "Digital Design", Pearson Education / PHI, 3rd Edition, 2008. 2. Fletcher W I, "An Engineering Approach to Digital Design", Prentice Hall India Learning Private Limited, 1990. 3. Zvi Kohavi, "Switching and Finite Automata Theory", Tata McGraw-Hill, 3rd Edition, 2004. 4. John M Yarbrough, "Digital logic applications and design", Thomson publications, 1st Edition, 2006. 5. J Millman, C C Halkias, "Integrated Electronics", Tata McGraw -Hill, 2008.
Reference Books:	
	1. Fredriac J Hill, Gerald R Peterson, "Introduction to Switching Theory and Logic Design", 3rd Edition, 2008. 2. Thomas L Floyd, "Digital Fundamentals", Pearson Publications, 10th Edition, 2013. 3. Roth, "Fundamentals of Logic Design", Thomson Publications,7th Edition, 2004 4. Comer, "Digital Logic and State Machine Design", Oxford Publications, 3rd Edition, 2013. 5. Rashid, "Electronic Circuit Analysis", Cengage Publishers, 12th Edition,2013 . 6. Robert L Boylestad, Louis Nashelsky, "Electronic Devices and Circuits Theory", PHI, 9th Edition, 2008.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Number systems, base conversion methods.	CLO 1	T1:1.1 to 1.5 R1: 3.1 to 3.5
6-8	Complements of numbers, codes- binary codes, BCD code and its	CLO 2	T1:1.7

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
	properties.		R1: 3.7 to 3.9
9-11	Unit distance code, alphanumeric codes, and error detecting and correcting codes.	CLO 2	T1:1.7 R1: 4.1 to 4.2
12-15	Basic theorems and its properties, switching functions, canonical and standard form.	CLO 4	T1:2.1 to 2.6 R2: 2.8 to 3.5
16-18	Algebraic simplification of digital logic gates, properties of XOR gates.	CLO 4	T1:2.8 R2: 3.3 to 3.7
19-21	Universal gates, Multilevel NAND/NOR realizations.	CLO 7	T1:3.7 to 3.8 R3: 2.7 to 2.9
22-24	Tabular method.	CLO 9	T1:3.5 to 3.9 R3: 3.8 to 3.9
25-32	Combinational design, arithmetic circuits- adders, subtractors.	CLO 9	T1:4.1 to 4.9 R4: 2.1 to 2.4
33-35	Serial adder, 1's complement subtractor, 2's complement subtractor.	CLO 11	T1:5.1 to 5.2 R4: 3.1 to 3.5
36-38	Combinational and sequential circuits, the binary cell, the fundamentals of sequential machine operation.	CLO 11	T1:5.3 to 5.5 R4: 5.1 to 5.8
39-42	Flip-flop, D-Latch Flip-flop, "Clocked T" Flip-flop, "Clocked JK "flip-flop.	CLO 13	T1:5.3 to 5.5 R4: 6.1 to 6.6
43-45	Design of a clocked flip-flop conversion from one type of flip-flop to another.	CLO 11	T1:5.3 to 5.5 R4: 6.7 to 7.9
46-48	Registers and counters	CLO 9	T1: 6.1 to 6.5 R4: 7.1 to 7.7
49-51	Feedback Amplifiers: Concepts of feedback, design of different feedback Amplifiers.	CLO 14	T3:12.1to12.4 R5: 4.1 to 4.8
52-54	Oscillators & design of types of oscillators	CLO 14	T3:15.2.1 to 15.2.2 R5: 7.1 to 7.4
55-58	Single stage & multi stage Amplifiers design of types	CLO 14	T3:8.4 R6: 6.1 to 6.6
59-60	Cascade & cascade amplifiers	CLO 14	T3:4.9.1 to 4.9.2 R6: 8.1 to 8.5

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S.No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Gate level Minimization.	Seminars / NPTEL	PO 1, PO 2, PO 4	PSO 1
2	Design of combinational circuits using universal gates.	Seminars / Guest Lectures / NPTEL	PO 2, PO 3, PO 4	PSO 1
3	Verilog programming for combinational and sequential circuits.	Laboratory Practices	PO 1, PO 3, PO 4	PSO 3

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