INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL IC APPLICATIONS USING VHDL**				
Course Code	AEC516				
Programme	B.Tech				
Semester	V	ECE			
Course Type	Elective				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Chief Coordinator	Dr. Vijay Vallabhuni, Associate Professor, ECE				
Course Faculty	Dr. K. Nehru, Professor, ECE Mr. D. Khalandar Basha, Assistant Professor, ECE				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits. They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Electronic Devices and Circuits	4
UG	AEC103	IV	Digital System Design Laboratory	2

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital IC applications using VHDL	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✔	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE):
The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz / Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Quiz / AAT**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	2	Lectures and Assignments
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	3	Seminars and Lab related exercises
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignments
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	3	Micro Project
PO 9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	3	Micro Project

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Lectures and Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Seminars

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Familiarization of Digital Logic families and design of combinational circuits using digital ICs.
II	Design of sequential circuits using digital ICs strategy of digital circuits using VHDL Programming.
III	Acquire knowledge of memories like SRAM, DRAM memories construction, operation and timing diagrams.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
CAEC516.01	CLO 1	Understand logic families of CMOS, TTL and ECL.	PO 1	2

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
CAEC516.02	CLO 2	Construct the circuits of CMOS basic gates like inverter, NAND, NOR, AOI and OAI logic with functionality verification.	PO 1, PO 3 PO 5	2
CAEC516.03	CLO 3	Construct the circuits of TTL logic family by understanding NAND, NOR gates with functionality verification.	PO 1	3
CAEC516.04	CLO 4	Identify the need of interfacing CMOS logic family with TTL logic family and interfacing TTL with CMOS logic.	PO 1	1
CAEC516.05	CLO 5	Understand the Static and dynamic electrical behavior of CMOS circuits.	PO 1	1
CAEC516.06	CLO 6	Understand the different design methods in VHDL.	PO 1	1
CAEC516.07	CLO 7	Acquire the basic constucts in VHDL programming.	PO 1	1
CAEC516.08	CLO 8	Understand the terms simulation and synthesis in the area of VLSI.	PO 1 PO 9	2
CAEC516.09	CLO 9	Familarization of basic combinational circuits viz decoders, encoders, multiplexers, demultiplexers, parity circuits.	PO 1	1
CAEC516.10	CLO 10	Familarization of basic arithmetic circuits for addition, subtraction and multiplication.	PO 1 PO 2	2
CAEC516.11	CLO 11	Distinguish between combinatorial and sequential circuits.	PO 1	1
CAEC516.12	CLO 12	Design sequential circuits like latches, flip-flops.	PO 1, PO 3 PO 5	3
CAEC516.13	CLO 13	Design sequential circuits like shift registers and counters.	PO 1, PO 3 PO 5	3
CAEC516.14	CLO 14	Understand synchronous design methodology	PO 1	1
CAEC516.15	CLO 15	Learns impediments to synchronous design	PO 1	1
CAEC516.16	CLO 16	Understand internal structure of SRAM and decoding mechanism	PO 1	1
CAEC516.17	CLO 17	Understand timing diagrams of SRAM for read and write operations	PO 1, PO 3 PO 9	2
CAEC516.18	CLO 18	Understand internal structure of DRAM	PO 1	1
CAEC516.19	CLO 19	Understand timing diagrams of DRAM for read and write operations	PO 1 PO 9	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	2														
CLO 2	3		1		2								2		
CLO 3	3												1		

CLO 4	1														
CLO 5	1														
CLO 6	1														
CLO 7	1														
CLO 8	1								2						
CLO 9	1														
CLO 10	1	2													
CLO 11	1												2		
CLO 12	1		3		3								3	2	
CLO 13	1		3		3								3	2	
CLO 14	1														
CLO 15	1														
CLO 16	1														
CLO 17	1		2						2				2		
CLO 18	1														
CLO 19	1								2				2		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 5 PO 9	SEE Exams	PO 1, PO 2 PO 3, PO 5 PO 9	Assignments	PO 1 PO 3	Seminars	PO 2
Laboratory Practices	–	Student Viva	–	Mini Project	–	Certification	–
Term Paper	–						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Assessment of Course Outcomes (By Feedback, Once)	✔	Student Feedback on Faculty (Twice)
✔	Assessment of Mini Projects By Experts		

XIII. SYLLABUS

Unit-I	CMOS LOGIC AND BIPOLAR LOGIC AND INTERFACING:
Introduction to logic families, CMOS logic, CMOS steady state electrical behavior, CMOSdynamic electrical behavior, CMOS logic families; Bipolar logic, transistor logic, TTL families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing, emitter coupled logic, comparison of logic families, familiarity with standard 74XX and CMOS 40XX series-ICs – specifications.	
Unit-II	**THE VHDL HDL AND ITS ELEMENTS:**
Design flow, program structure, types and constants, functions and procedures, libraries and packages; The VHDL design elements: Structural design elements, data flow design elements, behavioral design elements, time dimension and simulation synthesis.	
Unit-III	**COMBINATIONAL LOGIC DESIGN USING VHDL:**
Decoders, encoders, three state devices, multiplexers and demultiplexers, Code Converters, EX-OR gates and parity circuits, comparators, adders and subtractors, ALUs, combinational multipliers. VHDL modes for the above ICs. Design examples (using VHDL) - Barrel shifter, comparators, floating-point encoder, dual parity encoder.	
Unit-IV	**SEQUENTIAL LOGIC DESIGN:**
Latches and flip-flops, PLDs, counters, shift register, and their VHDL models, synchronous design methodology, impediments to synchronous design.	
Unit-V	**MEMORIES**
ROMs: Internal structure, 2D-decoding commercial types, timing and applications; Static RAM: Internal structure, SRAM timing, standard SRAMS, synchronous SRAMS; Dynamic RAM: Internal structure, timing, synchronous DRAMs; Familiarity with component data sheets : Cypress CY6116, CY7C1006, specifications.	
Text Books:	
1. John F.Wakerly, "Digital Design Principles & Practices", 3rd Edition, 2005, PHI/ Pearson Education Asia. 2. J. Bhasker, "VHDL Primer", Pearson Education / PHI, 3rd Edition. Pearson Higher Education.	
Reference Books:	
1. Charles H. Roth Jr., "Digital System Design Using VHDL", PWS Publications, 1998. 2. Alan B. Marcovitz, "Introduction to Logic Design", TMH, 2nd Edition, 2005. 3. Stephen Brown, ZvonkoVransesic, "Fundamentals of Digital Logic with Verilog Design", TMH, 2003. 4. Cypress Semiconductors Data Book (Download from website). 5. K. Lalkishore, "Linear Integrated Circuit Applications", Pearson Educations 2005.	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Introduction to Logic Family, MOS transistor operation.	CLO 1	T1: 3.3
2	CMOS logic and voltage levels, CMOS Inverter.	CLO 1	T1: 3.3
3	CMOS NAND and NOR gates.	CLO 2	T1: 3.3.4
4	CMOS AOI, OAI logic.	CLO 2	T1: 3.3.7
5	CMOS AND & OR gates.	CLO 2	T1: 3.3.7

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
6	CMOS XOR and XNOR gates.	CLO 2	T1: 3.3.7
7	CMOS steady state electrical behavior, CMOS dynamic Electrical behavior.	CLO 5	T1: 3.4
8	CMOS logic families, Diode Logic.	CLO 4	T1: 3.8-3.9
9	TTL NAND Gate.	CLO 3	T1: 3.10
10	TTL NOR Gate, CMOS/TTL interfacing, Low voltage CMOS logic and interfacing.	CLO 4	T1: 3.10. 3.12
11	Emitter Coupled Logic, Comparison of logic families, Familiarity with standard 74XX and CMOS 40XX series-ICs-Specifications.	CLO 4	T1:3.14
12	Design flow, Program structure, types and constants.	CLO 6	R5: 8.5-8.6
13	Functions and Procedures, Libraries and packages.	CLO 6	R5: 8.5-8.6
14	Structural design elements with example.	CLO 7	T1: 6.1-6.2
15	Data flow design elements with example.	CLO 7	T1: 6.1-6.2
16	Behavioral design elements with example.	CLO 7	T1: 6.3
17	Time dimension and simulation synthesis.	CLO 8	T1: 6.3
18	74x139 Decoder and VHDL model.	CLO 9	T1: 5.4.3
19	74x138 Decoder and VHDL model.	CLO 9	T1: 5.4.4
20	74x148 encoders and VHDL model.	CLO 9	T1: 5.5.2
21	Three state devices and VHDL model.	CLO 9	T1: 5.6
22	Multiplexers and VHDL model.	CLO 9	T1: 5.7
23	Multiplexers and VHDL model.	CLO 9	T1: 5.7
24	Demultiplexers and VHDL model.	CLO 9	T1: 5.7
25	Code Converters and VHDL model.	CLO 9	T1: 5.7
26	EX-OR gates and parity circuits, comparators and VHDL model.	CLO 9	T1: 5.8, 5.9
27	HA, FA adders and FA using HA and VHDL model.	CLO 10	T1:5.10
28	CLA adder and VHDL model.	CLO 10	T1: 5.10
29	Subtractors, FS using FA and VHDL model, ALUs and VHDL model.	CLO 10	T1: 5.10
30	Combinational multipliers.	CLO 10	T1: 5.11
31	Combinational multipliers VHDL model.	CLO 10	T1: 5.11
32	Barrel shifter.	CLO 10	T1: 6.1.1

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
33	Barrel shifter VHDL model.	CLO 10	T1: 5.1.2
34	Comparators, floating-point encoder and VHDL model.	CLO 10	T1: 5.1.3
35	Dual parity encoder and VHDL model.	CLO 10	T1: 5.13
36	Latches & flip-flops and VHDL model.	CLO 11	T1: 7.2
37	Realization of Lathes and Flip Flops, PLD and VHDL model.	CLO 12	T1: 7.2
38	Synchronous counters and VHDL model.	CLO 13	T1: 8.4
39	Asynchronous counters and VHDL model.	CLO 13	T1: 8.4
40	Shift register and VHDL model.	CLO 13	T1:8.5
41	Synchronous design methodology and impediments to synchronous design.	CLO 14 CLO 15	T1:8.7-8.8
42	ROMs Internal structure.	CLO 16	T1:8.6
43	2D-decoding ROMs, Commercial types, timing and applications.	CLO 16	T1: 8.2 R5: 4.4
44	Static RAM internal structure.	CLO 16	T1: 8.2 R5: 4.4
45	SRAM timing Standard SRAMS, synchronous SRAMS.	CLO 17	T1: 8.9
46	Dynamic RAM internal structure.	CLO 18	R6: 4.5
47	DRAM timing.	CLO 19	T1: 8.12-8.13
48	Synchronous DRAMs Familiarity with Component Data Sheets – Cypress CY6116, CY7C1006, Specifications.	CLO 18	T1: 10.6

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S.No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Design of combinational applications.	Laboratory Practices, Project/ NPTEL	PO 1, PO 2, PO 5	PSO 1
2	Design of sequential applications.	Laboratory Practices, Project	PO 1, PO 2, PO 5	PSO 1
3	Design of memories.	Seminars/ NPTEL	PO 1	PSO 1

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