INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

COMPUTER SCIENCE AND ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**ANALOG AND DIGITAL ELECTRONICS**				
Course Code	AECB05				
Programme	B.Tech				
Semester	THREE				
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	-	-
Chief Coordinator	Ms. M Lavanya, Assistant Professor				

COURSE OBJECTIVES:

Students will try to learn:	
I	The Fundamental knowledge of the operational principles and characteristics of semiconductor devices and their applications.
II	The basic concept of number systems, boolean algebra and optimized implementation of combinational and sequential circuits.
III	The perceive subsequent studies in the area of microprocessors, microcontrollers, VLSI design and embedded systems effectively use of fundamentals of digital electronics.

COURSE OUTCOMES:

At the end of the course students should be able to:

Course Outcomes		**Knowledge Level (Bloom's Taxonomy)**
CO1	**Recall** the properties of semiconductor materials which form the basis for the formation of PN junction diode.	Remember

CO2	**Illustrate** the volt-ampere characteristics of semiconductor devices for finding cut-in voltage, static, resistance and capacitance.	Understand
CO3	**Apply** the PN junction characteristics for the diode applications such as switch and rectifiers.	Apply
CO4	**Explain half** wave and full wave rectifier circuits with filter and without filters for conversion of alternating current in to direct current.	Understand
CO5	**Interpret** DC and AC load line analysis of different amplifiers for optimal operating level regardless of input, load placed on the device.	Understand
CO6	**Analyze** the input and output characteristics of transistor configurations and small signal h-parameter model for determining the input - output resistances, current gain and voltage gain	Analyze
CO7	**Compare** the binary decimal, octal and hexadecimal number systems in terms of basic arithmetic operations.	Analyze
CO8	**Identify** the functionality of logic gates, parity code and hamming code techniques for error detection and correction of single bit in digital systems.	Apply
CO9	**Apply** Boolean postulates and theorems, k-map and tabular methods for obtaining minimized Boolean expressions.	Apply
CO10	**Develop the** gate level combinational circuits to build adders, subtractors, multiplexers, demultiplexers, encoders and decoders.	Apply
CO11	**Describe** the operation of Flip-Flops and latches for constructing sequential circuits.	Understand
CO12	**Implement** the synchronous& asynchronous counters for memory storing applications.	Apply

MAPPING OF EACH CO WITH PO(s), PSO(s):

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	-	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	3	-	2	-	-	-	-	-	-	-	-	-	3	-	-
CO 6	3	-	1	-	-	-	-	-	-	-	-	-	-	-	-
CO 7	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 8	3	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 9	3	2	-	-	-	-	-	-	-	-	-	-	3	-	-
CO 10	3	1	-	-	-	-	-	-	-	-	-	-	-	-	-

CO 11	3	-	2	-	-	-	-	-	-	-	-	-	-	-	-
CO 12	-	2	2	-	-	-	-	-	-	-	-	-	3	-	-
TOTAL	**26**	**10**	**7**	-	-	-	-	-	-	-	-	-	**9**	-	-
AVERAGE	**2.6**	**1.6**	**1.7**	-	-	-	-	-	-	-	-	-	**3**	-	-

TUTORIAL QUESTION BANK

MODULE-I				
DIODE AND APPLICATIONS				
PART-A(Short Answer Questions)				
S.NO	**QUESTION**	**Blooms Taxonomy level**	**How does this subsume the level**	**Course outcomes**
1	Find the static resistance of PN diode from V-I characteristics.	Remember	--	CO 1
2	Define Fermi level.	Remember	--	CO 1
3	Define depletion region?	Remember	--	CO 2
4	List the Applications of diode.	Remember	--	CO 3
5	Outline the V-I characteristics of PN junction diode.	Understand	This would require the learner to **recall** the behavior of PN junction with applied bias. Then **outline** V-I characteristics of diode	CO 2
6	List the differences between ideal diode and practical diode.	Remember	--	CO 1
7	How diffusion capacitance is occurred in PN junction diode.	Remember	--	CO 1
8	Show the transition capacitance in PN junction diode.	Remember	--	CO 1
9	Explain drift current in PN diode.	Understand	This would require the learner to **recall** the conduction of diode in biasing. Then **explain** drift current component in PN diode	CO 1
10	Define efficiency and mention the efficiency of HWR and FWR.	Remember	--	CO 3
11	Illustrate the load line analysis of diode.	Understand	This would require the learner to **recall** the diode characteristics. Then **relate** load line to V-I characteristics of diode	CO 2
12	How diode acts as switch.	Understand	This would require the learner to **recall** the diode operation. Then **explain** how diode is used as switch	CO 3

13	Show the expression of ripple factor of half wave rectifier.	Understand	This would require the learner to **recall** rectifier formula and relate it.	CO 3
14	What is the dynamic resistance of PN junction diode.	Remember	--	CO 2
15	List the types of rectifiers.	Remember	--	CO 3
16	Classify the recovery times in PN diode.	Understand	This would require the learner to **recall** the switching times of diode. Then **list** the recovery times of PN diode	CO 1
17	What is the forward recovery time of PN junction diode.	Understand	This would require the learner to **recall** the switching times of diode. Then **write** the expression for forward recovery time	CO 1
18	Show the circuit for half wave rectifier using PN junction diode.	Remember	--	CO 3
19	What is the need for a filter in rectifier?	Remember	--	CO 3
20	Define cut-in voltage?	Remember	--	CO 3
PART-B(Long Answer Questions)				
1	Outline the V-I characteristics of p-n junction diode for forward bias and reverse bias voltages and represent the static and dynamic resistance of the diode in the characteristic curve.	Understand	This would require the learner to **recall** the V-I characteristics based on applied bias. Then **illustrate** the ideal and practical resistances.	CO 2
2	Summarize the static and dynamic resistances of a PN diode.	Understand	This would require the learner to **recall** the resistances of diode. Then **contrast** static and dynamic resistances	CO 2
3	Explain the following terms for a PN diode 1. Load line 2. Diode switching times. 3. Reverse saturation current.	Understand	This would require the learner to **recall** the diode operation. Then **explain** the terms due to the effect of load and temperature applied on diode	CO 2
4	Demonstrate the working of half-wave rectifier with circuit diagram and waveforms.	Understand	This would require the learner to **recall** the rectifier operation. Then **demonstrate** the half wave rectifier.	CO 3
5	Illustrate transition capacitance and Diffusion capacitance With suitable expression.	Understand	This would require the learner to **recall** the biasing of diode then **illustrate** the effect of capacitances.	CO 1
6	Illustrate the working of bridge full wave rectifier with circuit diagram and waveforms.	Understand	This would require the learner to **recall** the rectifier function then **explain** the bridge rectifier function using diodes.	CO 3
7	Explain the operation of PN- junction diode under forward bias and reverse bias condition and Sketch the V-I characteristics of p-n junction diode	Understand	This would require the learner to **recall** the V-I characteristics based on applied bias.	CO 3

8	Explain the differences between Static and dynamic resistances of a p – n diode.	Understand	This would require the learner to **recall** the rectifier operation. Then explain how bridge rectifier will work using diodes.	CO 3
9	Explain difference between intrinsic and extrinsic semiconductor.	Remember	--	CO 1
10	Discuss the following with respect to semiconductor: i. doping ii dopant iii donor iv acceptor..	Remember	--	CO 1
11	What is Rectification efficiency? Derive expression for the following Half wave rectifier Full wave rectifier	Understand	This would require the learner to **recall** rectifier formula. Then relate the factors related to half wave and full wave rectifiers.	CO 3
12	Explain the temperature dependence of VI characteristics of PN diode?	Understand	This would require the learner to **recall** its formula. Then **relate** the factors to full wave rectifier.	CO 3
13	Find the terms as referred to the half wave rectifier: Efficiency Average or D.C voltage Ripple factor.	Remember	--	CO 3
14	Explain what is hole is. How do they move in intrinsic semiconductor?	Remember	--	CO 1
15	Find the terms as referred to the full wave rectifier: PIV TUF Ripple factor.	Remember	--	CO 3
16	Find the ripple factor for the half wave rectifier with a shunt capacitor filter.	Remember	--	CO 3
17	List the merits and Demerits of half wave, full wave and bridge rectifier.	Remember	--	CO 3
18	Explain the formation of depletion region in an open circuited p-n junction with neat sketches.	Understand	This would require the learner to **recall** the construction of PN junction diode. Then **explain** how the depletion region is formed for unbiased	CO 1
19	What is d.c load line and explain the d.c load line analysis of p-n junction diode with relevant expressions.	Understand	This would require the learner to **recall** the load line analysis for diode. Then **explain** the DC load line	CO 2
20	Write the applications of p-n junction diode and explain how the p-n diode acts as a switch.	Understand	This would require the learner to **recall** the applications of diode **understand** the operation of diode and how it acts as a switch.	CO 3
PART-C(Analytical Questions)				
1	Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0C with reverse saturation current,	Remember	--	CO 2

	I_0 = 25μA and at an applied voltage of 0.2V across the diode.			
2	Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 250^0 C with reverse saturation current, Io = 5μA and at an applied voltage of 0.2V across the diode?	Remember	--	CO 2
3	The reverse saturation current of a silicon p – n junction diode is 10uA. Calculate the diode current for the forward-bias voltage of 0.6v at 25^0C.	Understand	This would require the learner to **recall,** the formula of diode and then assign values for parameters and **solve** the given parameters	CO 2
4	Determine the values of forward current in the case of P-N junction diode, with I_0=10 μA Vf=0.8V at T=300^0K.Assume silicon diode?	Remember	--	CO 3
5	The voltage across a silicon diode at room temperature of 300K is 0.7 V when 2 ma current flows through it. If the voltage increases to 0.75 v, Evaluate the diode current assuming VT=26mv.	Remember	--	CO 3
6	In a full wave rectifier ,the transformer rms secondary voltage from center tap to each end of the secondary is 50 V. The lad resistance is 900 ohms. If the diode resistance and transformer secondary winding resistance together has a resistance of 100ohms , determine the average load current and RMS value of load current.	Remember	--	CO 3
7	A half wave rectifier is used to supply 24V dc to a resistance load of 500 ohms and the diode has a forward resistance of 50 ohms. Calculate the maximum value of the ac voltage required at the input.	Remember	--	CO 3
8	A full wave rectifier delivers 50 W to a load of 200 ohms. If the ripple factor is 1%, calculate the AC ripple voltage across the load.	Understand	This would require the learner to **recall,** the formula of full wave rectifier and then assign values for parameters and **solve** the given parameters	CO 3
9	Determine the dynamic forward and reverse resistance of p-n Junction silicon diode when the applied voltage is 0.25 V at T=300K with give I_0=2 μA?	Remember	--	CO 1
10	A 230V, 50Hz voltage is applied to the primary of a 4:1 step down transformer used in a bridge rectifier having a load resistance of 600ohms.Assuming the diodes to be ideal ,determine (a) dc output voltage,(b) dc powered delivered to the load ,(c) PIV, and(d) output frequency	Remember	--	CO 3

MODULE-II				
BIPOLAR JUNCTION TRANSISTOR (BJT)				
PART-A(Short Answer Questions)				
1	Show the Bipolar Junction Transistor and label the terminals of transistor.	Understand	This would require the learner to **recall** the construction of transistor. Then **outline** the terminals of transistor	CO 5
2	Show the Q point in transistor characteristics.	Understand	This would require the learner to **recall** the operating point. Then **outline** the transistor operation	CO 5
3	Outline the symbols of NPN and PNP transistor.	Understand	This would require the learner to **identify** the symbolic representation of transistors then **show** the symbols of NPN and PNP transistors	CO 5
4	Show AC load line of transistor.	Understand	This would require the learner to **recall** the load line analysis then **find** AC load line from characteristics of transistor.	CO 5
5	Relate α, β and γ in bipolar transistor.	Understand	This would require the learner to **recall** the amplification factors in transistor. then **relate** the α, β and γ.	CO 5
6	List out h parameters in CE configuration.	Remember	--	CO 6
7	List the h parameters in CB configuration.	Remember	--	CO 6
8	Recall base width modulation in bipolar junction transistor.	Remember	--	CO 6
9	Show h parameters in CC configuration.	Understand	This would require the learner to **recall** the hybrid model of transistor. Then **outline** the parameters from h-model	CO 6
10	Show current amplification factor for CE configuration.	Understand	This would require the learner to **recall** the transistor operation. Then show amplification factor for CE based Transistor.	CO 6
11	When the transistor is said to be in cut-off region.	Remember	--	CO 6
12	List the various regions in a transistor and compare them with respect to doping and width.	Remember	--	CO 6
13	Outline the output characteristics of NPN transistor in Common Emitter configuration.	Understand	This would require the learner to **recall** the transistor operation. Then show the output characteristics in CE configuration	CO 6
14	Show the circuit of a Common Base configuration using PNP transistor.	Understand	This would require the learner to **recall** the transistor configuration then **construct** the configuration using Common base	CO 6

15	Show the relation between I_C, β, I_B and I_{CBO} in Bipolar Junction transistor.	Understand	This would require the learner to **recall** the transistor operation. Then **relate** the parameters.	CO 5
16	What is the significance of the arrow-head in the transistor symbol?	Remember	--	CO 5
17	Relate the active region for NPN transistor using Common Emitter configuration.	Understand	This would require the learner to **recall** the transistor operation. Then **relate** the active region for NPN transistor	CO 5
18	Label the various current components in a BJT.	Remember	--	CO 5
19	Name the current controlling devices.	Remember	--	CO 5
20	Relate dc and ac load lines of transistor.	Remember	--	CO 5
PART-B(Long Answer Questions)				
1	Explain the various current components in an NPN bipolar junction transistor With a neat diagram.	Understand	This would require the learner to **recall** the transistor operation. Then **relate** the current components in BJT.	CO 5
2	What factors are to be considered for selecting the operating point Q for an amplifier	Apply	This would require learner to recall the load line analysis, **understand** what factors are considered and apply those formulate to find operating point Q for an amplifier.	CO 2
3	Demonstrate the working of transistor in common emitter configurations and draw its input and output characteristics.	Understand	This would require the learner to **recall** the transistor construction. Then **demonstrate** the CE configuration	CO 6
4	Explain working of transistor in common base configurations and draw its input and output characteristics.	Understand	This would require the learner to **recall** the transistor construction. Then **demonstrate** the CB configuration	CO 6
5	Explain working of transistor in common collector configurations and draw its input and output characteristics.	Understand	This would require the learner to **recall** the transistor construction. Then **demonstrate** the CC configuration	CO 6
6	Show the h-parameters of a bipolar junction transistor in a small signal model.	Understand	This would require the learner to **recall** the hybrid model of transistor. Then **show** the parameters of BJT from h-model	CO 6
7	The common-base dc current gain of a transistor is 0.967. If the emitter current is 10 mA, Solve the value of base current.	Understand	This would require the learner to **recall** its formula for assigning the values to **solve** the base current	CO 6
8	The transistor has IE = 20 mA and α = 0.18. Find the values of I_C and I_B.	Remember	--	CO 6
9	Determine the h-parameters for the common base configuration using NPN transistor.	Understand	This would require the learner to **recall** the hybrid model of common base configuration. Then **show** the parameters of BJT from h-model	CO 6

10	Explain the CE configuration using h-parameter model.	Understand	This would require the learner to **recall** the hybrid model of common Emitter configuration. Then **show** the parameters of CE amplifier	CO 6
11	Illustrate the common collector configuration of BJT with relevant figures and explain its input and output characteristics.	Understand	This would require the learner to **recall** the transistor construction. Then **demonstrate** the CC configuration	CO 6
12	Explain the DC and AC load line analysis of a BJT.	Understand	This would require the learner to **recall** the load line analysis then **illustrate** Dc and AC load line for transistor.	CO 5
13	Draw the small-signal model of common base BJT amplifier. Derive expressions for voltage gain, input resistance current gain and output resistance?	Remember	This would require to **recall** the physical scenario to **find the**h-model to the CE configuration of transistor	CO 6
14	Draw the small-signal model of common collector BJT amplifier. Derive expressions for voltage gain, input resistance, current gain and output resistance?	Remember	--	CO 6
15	Draw the small-signal model of common emitter BJT amplifier. Derive expressions for voltage gain, input resistance current gain and output resistance?	Remember	--	CO 6
16	For a transistor circuit having $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5\ \mu A$, and $I_B = 100\ \mu A$, find I_C and I_E.	Remember	--	CO 6
17	Define following i) Active Region ii) Cut off region iii) Saturation region	Understand	This would require the learner to **recall** the amplification of the transistor and **understand** how transistor operates in three regions.	CO 6
18	The dc current gain of a transistor in CE mode is 100. Find its dc current gain in CB mode.	Remember	--	CO 6
19	List the formulae used to convert CE h-parameters to CB and CC	Remember	--	CO 6
20	Explain the small signal model of BJT CE Amplifier and derive expressions for voltage gain, input resistance current gain and output resistance of CE amplifier?	Understand	This would require the learner to **recall** the formulas for amplification factors in transistor. Then **solve** the parameters.	CO 6
PART-C(Analytical Questions)				
1	A CE Amplifier is drawn by a voltage source of internal resistance Rs=800Ω and RL = 1000Ω.The h-parameters are hie= 1kΩ hre= 2x10-4 , hfe=50 and hoe=25μA/V. Determine Ai, Ri, Av, Ro. Using exact analysis and approximate analysis.	Understand	This would require the learner to **recall** the formulas for amplification factors in transistor. Then **solve** the parameters.	CO 6

2	Determine Ai, Ri, Av, Ro For a CE Amplifier using NPN transistor with hie= 1200Ω hre= 0 hfe=36 and hoe=2x10-6 Mhos. Rs=500Ω and RL =2.5kΩ(neglect the effect of biasing circuit)	Apply	This would require r**ecall** the h-parameters, **understand** relevant h-model parameters and **apply** the h-model to the CE amplifier for measuring the gain parameters.	CO 6
3	For a CE Amplifier ,if Rs=RL=1000 Ω, hie= 1100Ω hre= 2.5x10-4hfe=50 and hoe=25μA/V. Find Ai, Ri, Av Ais , and Avs	Apply	This would require recall expression for performance of a CE amplifier parameters **(understand)** in terms of h model and apply to measure the gain parameters.	CO 6
4	A transistor operating in CB configuration has Ic = 2.98mA, I_E = 3mA and I_{C0} = 0.01mA. What current will flow in the collector circuit of this transistor when connected in CE configuration with base current of 30μA.	Understand	This would require the learner to **recall** the transistor operation under CE mode. Then **solve** the collector current.	CO 6
5	The transistor has a I_E =10mA and α=0.98. Determine the value of I_C AND I_B	Remember	----	CO 6
6	The h-parameters of a transistor in the CE amplifier mode are hie= 1100Ω hre= 2.5x10-4 hfe=50 and hoe=25μA/V. determine the current gain and input resistance of the amplifier for a load resistance RL=1K Ω	Remember	----	CO 6
7	For a CB Configuration Rs=1200 Ω,RL=1000 Ω.The h-parameters are hib= 22Ω hrb= 3x10-4 hfb=-0.98 and hob=0.5μA/V Find Ai, Ri, Av Ais , Ro and Avs using exact analysis.	Remember	----	CO 6
8	A transistor connected in CC configuration and its h-parameters are hie= 1100Ω hre= 2.5x10-4 hfe=-50 and hoe=24μA/V Find Ai, Ri, and Av	Understand	This would require the learner to **recall** the transistor operation in CE mode. Then **solve** the Ai, Ri, and Av of the CE Amplifier.	CO 6
9	For a transistor circuit having α = 0.97 find the value of β. If β=200, find the value of α.	Remember	--	CO 6
10	The h-parameters of a transistor used as an amplifier in the CE configuration are are hie= 800Ω hre= 5.4x10-4 hfe=-50 and hoe=80 x 10^{-6}. If the load resistance is 5k Ω Find Ai, Ri ,Ro and Av	Understand	This would require the learner to **recall** the transistor operation in CB mode. Then **solve** the Ai, Ri, and Av of the CB Amplifier.	CO 6
MODULE – III				
NUMBER SYSTEMS				
PART - A (Short Answer Questions)				
1	Write short notes on binary number systems.	Remember	---	CO 7
2	Explain 1's and 2's complement.	Understand	Learner to recall binary numbers and find the 1's and 2's complement.	CO 7
3	Discuss octal number system.	Understand	---	CO 7

4	Convert the octal numbers into binary, decimal and Hexadecimal numbers (45.5)8, (32.2)8.	Understand	---	CO 7
5	Show an example to convert gray code to binary code.	Remember	---	CO 7
6	Describe a short note on four bit BCD codes.	Remember	---	CO 7
7	Illustrate about unit –distance code? State where they are used.	Understand	Learner to recall the operation of gray code and find the unit distance code.	CO 7
8	List the applications of error correcting codes.	Remember	---	CO 8
9	Convert 10101101.0111 to octal equivalent and hexadecimal equivalent.	Remember	---	CO 7
10	Give the examples of unit distance codes	Remember	---	CO 7
	CIE-II			
1	Which gates are called as universal gate justify.	Understand	Learner to **recall** the operation of logic gates and **find** universal gates.	CO 8
2	State DeMorgan's theorem	Remember	---	CO 9
3	State Duality theorem.	Remember	---	CO 9
4	Draw the symbols and truth tables of XOR and XNOR gates	Remember	---	CO 9
5	Define sum of products and product of sum	Remember	---	CO 9
6	State and prove the distributive property of Boolean algebra.	Remember	---	CO 9
7	Simplify ABC+AB'C+ABC'	Understand	Learner to recall the operation of Boolean postulates and theorems and **Solve** the expression.	CO 9
8	Convert the given expression in standard SOP form Y= AC+AB+BC	Understand	Learner to **recall** the operation of conversions and **understand** the standard form and expand the expression.	CO 9
9	Convert the given expression in standard POS form Y= (A+B)(B+C)(A+C).	Understand	Learner to **recall** the operation of conversions and **understand** the standard form and expand the expression.	CO 9
10	List out the basic logic gates with truth tables	Remember	---	CO 9
	PART-B (Long Answer Questions)			
1	Explain error occurred in data transmission can be detected using parity bit?	Understand	Learner to **recall** the operation of parity generation and **understand** the error detecting code.	CO 8
2	Define weighted codes and non weighted codes with examples?	Remember	---	CO 8
3	Explain what do you mean by error detection and correcting code with examples.	Understand	Learner to **recall** the operation of parity generation and **understand** the error detecting code.	CO 8

4	Explain the gray to binary and binary- to-gray conversion with examples	Understand	Learner to **recall** binary and gray code and **understand** the conversion using Ex-or gate logic.	CO 7
5	Explain the conversion of AND/OR/NOT logic to NAND/ NOR logic with example.	Understand	This would require the learner to **recall** the operation of logic gate and **understand the** conversion to universal gates.	CO 8
6	Explain Self complemented codes.	Remember	---	CO 7
7	Differentiate between BCD code and 2421 code and XS-3.	Understand	Learner to **recall** the concept of BCD code, 2421 code and XS-3 code and **list** the differences.	CO 7
8	Solve the given 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors.	Apply	Learner to **recall** the Binary information and **understand** concept of hamming code and **apply** in solving the given data.	CO 8
9	Write the first 10 decimal digits in base 3 and base 16.	Remember	---	CO 7
10	A device transmits the binary data using even parity, the message is 1011001. Identify the receiver receives the correct data or not.	Remember	---	CO 8
	CIE-II			
1	Convert the given expression in standard POS form Y= (A+B)(B+C)(A+C).	Understand	This would require the learner to **recall** the operation of conversion to standard form and **expand** the expression.	CO 9
2	Give the Boolean expressions, symbols and truth tables for following gates, i) AND ii) NOR iii) EX-OR iv) OR v) EX-NOR.	Remember	---	CO8
3	Implement all the logic gates using NAND gate.	Apply	This would require the learner to **recall** the operation of logic gate and **understand** the conversion to NAND gate process and **apply** it for all logic gates.	CO8
4	Construct all the logic gates using NOR gate.	Apply	This would require the learner to **recall** the operation of logic gate and **understand** the conversion to NOR gate process and **apply** it for all logic gates	CO8
5	Solve the canonical SOP form of the following functions. i) Y(A,B) = A+B. ii) Y(A,B,C,D) = AB+ACD	Remember	----.	CO 9
6	Simplify the expression Z= AB+AB'. (A'C')'	Understand	This would require the learner to **recall** the operation of conversion to standard form and **simplify** the expression.	CO 9
7	Simplify the following 3 variable expression using Boolean algebra Y=	Understand	This would require the learner to **recall** the operation of conversion to	CO 9

	∏M(3,5,7).		standard form and **simplify** the expression.	
8	Simplify the following 3 variable expression using Boolean algebra Y= ∑m(1,3,5,7).	Understand	This would require the learner to **recall** the operation of conversion to standard form and **simplify** the expression.	CO 9
9	Explain standard SOP and POS forms with examples	Remember	---	CO 9
10	State and prove Boolean theorems and properties.	Remember	---	CO 9
PART-C (Problem Solving and Critical Thinking Questions)				
1	Convert the following Hexadecimal number to their Decimal equivalent (EAF1)16.	Understand	This would require the learner to **recall** the concept of binary and decimal number system and **find** the conversion.	CO 7
2	What is the gray code equivalent of the Hex Number 3A7. Find 9's complement of (25.639)10.	Remember	---	CO 7
3	Implement 7 bit hamming code for given message 1010 by using odd parity.	Apply	This would require the learner to **recall** the concept of odd parity and **understand** the using of parity bits in hamming code and to **implement** hamming code for given data	CO 8
4	Perform the subtraction using 1's complement and 2's Complement i) $(11010)_2 - (10000)_2$ ii) $(1000100)_2 - (1010100)_2$	Remember	---	CO 7
5	Convert following hexadecimal number to decimal, i) F2816 ii) BC216	Remember	---	CO 9
CIE-II				
1	Implement Y= AB'+A' B using 2 input NAND gates	Apply	This would require the learner to **recall** the concept of logic gates and **understand** the logic of NAND gate to **implement** the expression.	CO 8
2	Simplify using postulates and theorems of Boolean algebra i) (X+Y'+XY)(X+Y')X'Y ii) (AB+C+D)(C'+D)(C'+D+E)	Understand	This would require the learner to **recall** the concept of postulates and theorems of Boolean algebra to **simplify** the given expression.	CO 9
3	For each of the following expressions, construct the corresponding logic circuit using AND/OR/INVERT logic. i) Y=AB(C+D) ii) Z= (W+PQ')'	Remember	---	CO 9
4	Implement Y= AB'+A' B using 2 input NOR gates	Apply	This would require the learner to **recall** the concept of logic gates and **understand** the logic of NOR gate to **implement** the expression.	CO 8
5	Realize X-OR operation a)NAND gate b)NOR gate	Apply	This would require the learner to **recall** the concept of X-OR gate and	CO 8

			understand the logic of NAND and NOR gates to **implement** the X-OR operation.	
MODULE – IV				
MINIMIZATION OF BOOLEAN FUNCTIONS				
PART - A (Short Answer Questions)				
1	What is K-Map and State the limitations of karnaugh map.	Remember	-----	CO 9
2	Construct a 16 × 1 Mux using only 2 × 1 Mux	Understand	This would require the learner to **recall** concept of multiplexer and **understand the** design procedure of Boolean functions using multiplexer and this procedure can **implement** 16x1 Mux using 2x1 Mux with proper selection lines.	CO 10
3	Define even and odd parity.	Remember	----	CO 10
4	What is decoder? How do you convert a decoder in to a De- Multiplexer	Remember	----	CO 10
5	What is multiplexer? Give the size of a multiplexer.	Remember	----	CO 10
6	Define Implicant, Prime Implicant and Essential Prime Implicant.	Remember	----	CO 9
7	Sketch the Full adder using Logic Gates.	Understand	This would require the learner to **recall** the operation of full adder its truth table and **draw** the Full Adder circuit using logic gates.	CO 10
8	Draw the Half subtractor using NAND Gates.	Understand	This would require the learner to **recall** the operation of half subtractor its truth table and **draw** the half subtractor circuit using NAND gates.	CO 10
9	What is Demultiplexer? Give the size of a Demultiplexer.	Remember	----	CO 10
10	List some of the applications of multiplexer and de multiplexer	Remember	----	CO 10
11	Draw a Full adder using NOR Gates.	Understand	This would require the learner to **recall** the operation of full adder its truth table and understand the Full Adder using NOR gates.	CO 10
12	Draw Half subtractor using NOR Gates	Understand	This would require the learner to **recall** the operation of Half Subtractor its truth table and understand the Half Subtractor using NOR gates.	CO 10
13	Draw a Full subtractor using NAND Gates.	Understand	This would require the learner to **recall** the operation of full subtractor its truth table and	CO 10

			understand the Full Subtractor using NAND gates.	
14	Draw a Full subtractor using NOR Gates.	Understand	This would require the learner to **recall** the operation of full Subtractor its truth table and understand the Full Adder using NOR gates.	CO 10
15	State the truth table for full adder.	Remember	----	CO 10
16	Draw a Full adder using NAND Gates.	Understand	This would require the learner to **recall** the operation of full adder its truth table and understand. The Full Adder using NAND gates.	CO 10
17	Explain the differences between multiplexer and de multiplexer	Understand	This would require the learner to **recall** the operation of MUX and De-MUX, truth table and logic circuit. and **distinguish** between them in terms of number of inputs, outputs and their applications.	CO 10
18	Explain about J-K (NOR gates) Latch?	Understand	This would require the learner to **recall** the logic circuit and truth table of JK-latch using NOR gates and **explain** the operation JK-latch for various combinations of J and k inputs.	CO 11
19	Write the characteristic equations of SR, JK, D and T flip-flops.	Remember	-----	CO 11
20	Explain the differences between synchronous and asynchronous latch?	Understand	This would require the learner to **recall** the concept of synchronous and asynchronous latch and **find** the differences between them.	CO 11
PART-B (Long Answer Questions)				
1	Explain the design procedure of Synchronous Sequential circuit with an example?	Understand	This would require the learner to **recall** the concept of synchronous conversion and the design procedure of combinational logic circuits. And explain the design of code converters by taking an example.	CO 12
2	Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers?	Understand	This would require the learner to **recall** the basic structure and operation of shift register. And explain the operation in serial transfer mode also its applications.	CO 12
3	Explain about Binary Ripple Counter? What is MOD counter?	Understand	This would require the learner to **recall** the concept of asynchronous counter and mod counter. Then **explain** the operation of binary ripple counter.	CO 12
4	How do you convert Jk- Flip Flop to SR-Flip Flop	Understand	This would require the learner to **recall** operation of JK and SR flip-flops and their truth tables. Then convert the JK flip-flop into SR flip-flop **using**	CO 11

			excitation tables and characteristic tables.	
5	How do you convert T- Flip Flop to SR- Flip Flop	Understand	This would require the learner to **recall** the operation of T and SR flip-flops and their truth tables. Then convert the T flip-flop into SR flip-flop **using** excitation tables and characteristic tables.	CO 11
6	How do you convert D- Flip Flop to JK- Flip Flop	Understand	This would require the learner to **recall** operation of D and JK flip-flops and their truth tables. Then convert the D flip-flop into JK flip-flop **using** excitation tables and characteristic tables.	CO 11
7	Explain the JK and Master slave Flip-flop? Give its timing waveform?	Understand	This would require the learner to **recall** the operation of JK flip-flop and race around condition. Then **explain** how the race around condition is eliminated in Master slave flip-flop with the help of timing waveforms.	CO 11
8	Explain the Ripple counter design procedure. Also design a decade counters.	Understand	This would require the learner to **recall** the design procedure of ripple counter. And understand the decade counter which can count 10 pulses.	CO 12
9	Construct a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter?	Apply	This would require the learner to **recall** the operation of Counters and **understand** the design procedure of synchronous counter to **construct** a Ring counter and discuss the differences between Ring and Twisted Ring counter.	CO 12
10	Explain the JK – Flip-flop with the help of a logic diagram and characteristic table?	Understand	This would require the learner to **recall** the logic diagram and **understand** the characteristic table of JK flip-flop.	CO 11
11	Construct a logic circuit to convert gray code to binary code.	Apply	This would require the learner to **recall** the concept of gray code, binary code and **understand** the design procedure of combinational logic circuits to **implement** a logic circuit to convert gray code to its equivalent binary code using logic gates.	CO 10
12	Construct a logic circuit to convert binary code to gray code.	Apply	This would require the learner to **recall** the concept of gray code, binary code and **understand** the design procedure of combinational logic circuits to **implement** a logic circuit to convert binary code to its equivalent gray code using logic gates.	CO 10

13	Realize the Boolean expression for full subtractor and draw the logic circuit.	Understand	This would require the learner to **recall** the concept of full subtractor. Then **derive** the output equations of full subtractor and draw the circuit using logic gates.	CO 10
14	Implement the circuit to produce the octal number for given 4 bit binary number.	Apply	This would require the learner to **recall** the concept of octal number system **understand** the design procedure of combinational logic circuits. Then can **implement** a logic circuit to produce the octal number or the given 4 bit binary number.	CO 10
15	Explain 4-bit carry look-ahead adder with necessary diagram and relevant expressions.	Understand	This would require the learner to **recall** the concept of 4- bit carry look-ahead adder. Then **explain** the operation of 4-bit carry look-ahead adder and how it reduces the propagation delay compared to 4-bit parallel binary adder.	CO 10
16	Simplify the following Boolean expressions using K- map and implement them using logic gates. F (A, B, C, D)= AB'C'+ AC + A'CD' F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ	Understand	This would require the learner to **recall** the concept of simplifying a Boolean function using Karnaugh map. **Understand** the simplified function using logic gates.	CO 9
17	Implement a 64:1 MUX using 8:1 MUXs.	Apply	This would require the learner to **recall** the Boolean functions using multiplexer and **understand** the design procedure of boolen function using multiplexer to **implemen**t 64:1 Mux using 8:1 Mux with proper selection lines.	CO 10
18	Explain the working of 2 to 4 decoder and also implement a 2 to 4 decoder using 1 to 2 decoder.	Understand	This would require the learner to **recall** working of 2 to 4 and 1 to 2 decoder. And **understand** the 2 to 4 decoder using 1 to 2 decoders.	CO 10
19	Implement the full Subtractor circuit using half subtractor and justify with boolean expressions.	Apply	This would require the learner to **recall** the concept of subtractors and understand the logic of Half& full subtractors. Then **build** a Full subtractor using two Half subtractors.	CO 10
20	Simplify the following using Tabular method. $\sum m(1,2,3,5,9,12,14,15)+d(4,8,11)$	Understand	This would require the learner to **recall** the concept of simplifying a boolean function using Tabular method. Then can **simplify** the given boolean function by forming a table consisting of required number of columns.	CO 9
PART-C (Problem Solving and Critical Thinking Questions)				
1	Explain the working of 3-bit asynchronous up-down counter with necessary waveform and truth table.	Understand	This would require the learner to **recall** the concept of asynchronous counter. Then **explain** the operation of	CO 12

			a 3-bit asynchronous up-down counter.	
2	How do you convert Jk- Flip Flop to SR-Flip Flop	Understand	This would require the learner to **recall** operation of SR and JK flip-flops and their truth tables. Then convert the SR flip-flop into JK flip-flop **using** excitation tables and characteristic tables.	CO 12
3	Construct a 4-bit binary counter (using D flip flops) which counts all possible odd numbers only?	Apply	This would require the learner to **recall** the operation of D flip-flop **understand** the design procedure of counter and to **construc**t a counter which can count all possible odd numbers only using D flip-flops.	CO 12
4	Develop a Modulo-12 Synchronous up counters using T-Flip Flops and draw the Circuit diagram.	Apply	This would require the learner to **recall** the operation of T flip-flop and **understand** the design procedure of synchronous counter to **design** a Modulo-12 counter using T flip-flops.	CO 12
5	How do you convert Jk- Flip Flop to D-Flip Flop	Understand	This would require the learner to **recall** operation of D and JK flip-flops and their truth tables. Then convert the D flip-flop into JK flip-flop **using** excitation tables and characteristic tables.	CO 11
6	Construct a MOD-5 synchronous counter using flip flops and Implement it? Also draw the timing diagram?	Apply	This would require the learner to **recall** the operation of flip-flops to understand the design procedure of synchronous counter and to construct a Mod-5 counter which can count the given sequence using JK flip-flops.	CO 12
7	How do you convert SR- Flip Flop to JK-Flip Flop	Understand	This would require the learner to **recall** operation of JK and SR flip-flops and their truth tables. Then convert the SR flip-flop into JK flip-flop **using** excitation tables and characteristic tables.	CO 12
8	Build a 4- bit Twisted Ring counter using JK flip-flop?	Apply	This would require the learner to **recall** the concept of synchronous counter. **Understand** the design procedure to **build** a 4-bit twisted ring counter using JK flip-flops.	CO 12
9	Implement MOD5 up and Down counter?	Apply	This would require the learner to **recall** the concept of synchronous counter. **Understand** the design procedure to **implement** a Mod-5 Up and Down counter	CO 12
10	How do you convert Jk- Flip Flop to T-Flip Flop	Understand	This would require the learner to **recall** operation of T and JK flip-flops and their truth tables. Then convert the D flip-flop into JK flip-	CO 11

			flop **using** excitation tables and characteristic tables.	
MODULE – V				
Sequential Circuits Fundamentals				
PART - A (Short Answer Questions)				
1	Write the Differences combinational and sequential logic circuits?	Understand	This would require the learner to **recall** the block diagram of combinational and sequential circuits. Then **find** the differences between them.	CO 11
2	Explain basic difference between a shift register and counter?	Understand	This would require the learner to **recall** the basic structure and operation of shift register and counter. Then **explain** the differences between them.	CO12
3	Illustrate applications of shift registers?	Understand	This would require the learner to **recall** the basic structure and operation of shift register. Then can **find** its applications.	CO 12
4	Define bidirectional shift register?	Remember	----	CO 12
5	Write the Differences Flip-flop and latch?	Understand	This would require the learner to **recall** the concept of latch and flip-flop. Then **find** the differences between them.	CO 11
6	Define Counter?	Remember	----	CO 12
7	Classify the basic types of counters?	Understand	This would require the learner to **recall** the definition of counter. Then **find** the various types of counters.	CO 12
8	Write the Differences the advantages and disadvantages of ripple counters?	Understand	This would require the learner to **recall** the operation of ripple counter, and write the advantages and disadvantages of ripple counter over synchronous counter.	CO 12
9	Describe the applications of counters?	Understand	This would require the learner to **recall** the basic structure and operation of counters. Then can **find** its real time applications.	CO 12
10	Draw D-latch using NAND?	Remember	---	CO 11
11	Explain the operation of gated SR latch.	Understand	This would require the learner to **recall** the logic circuit and truth table of SR-latch. Then can **explain** the operation of SR-latch for various combinations of S and R inputs	CO 11
12	Define race around condition? How it can be avoided?	Understand	This would require the learner to **recall** the operation of JK flip-flop. Then can **find** the occurrence of race	CO 11

			around condition in JK flip-flop and also can discuss the remedy for it.	
13	Explain about S-R (NOR gates) Latch?	Understand	This would require the learner to **recall** the logic circuit and truth table of SR-latch using NOR gates. Then **explain** the operation SR-latch for various combinations of S and R inputs.	CO 11
14	Explain about S-R (NAND gates) Latch?	Understand	This would require the learner to **recall** the logic circuit and truth table of SR-latch using NAND gates. Then **explain** the operation SR-latch for various combinations of S and R inputs.	CO 11
15	Draw The truth table of gated D-Latch?	Understand	This would require the learner to **recall** the logic circuit and operation of D-latch and understand the truth table of D-latch based on the operation.	CO 11
16	List the advantages and disadvantages of Johnson counter.	Remember	----	CO 12
17	Draw The truth table of gated SR-Latch?	Understand	This would require the learner to **recall** the logic circuit and operation of SR-latch and understand the truth table of SR-latch based on the operation.	CO 11
18	Explain about J-K (NOR gates) Latch?	Understand	This would require the learner to **recall** the logic circuit and truth table of JK-latch using NOR gates. Then **explain** the operation JK-latch for various combinations of J and k inputs.	CO 11
19	Write the characteristic equations of SR, JK, D and T flip-flops.	Understand	This would require the learner to **recall** the truth tables of SR, JK, D and T flip-flops. **Understand** the characteristic equations using K-map	CO 11
20	Distinguish between synchronous and asynchronous latch?	Understand	This would require the learner to **recall** the concept of synchronous and asynchronous latch. Then **explain** the differences between them.	CO 11
PART-B (Long Answer Questions)				
1	Explain the design procedure of Synchronous Sequential circuit with an example?	Understand	This would require the learner to **recall** the concept of synchronous conversion and the design procedure of combinational logic circuits. Then can **explain** the design of code converters by taking an example.	CO 12
2	Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers?	Understand	This would require the learner to **recall** the basic structure and operation of shift register. Then can	CO 12

			explain the operation in serial transfer mode also its applications.	
3	Explain about Binary Ripple Counter? What is MOD counter?	Understand	This would require the learner to **recall** the concept of asynchronous counter and mod counter. Then **explain** the operation of binary ripple counter.	CO 12
4	How do you convert Jk- Flip Flop to SR- Flip Flop	Remember	----	CO 11
5	How do you convert T- Flip Flop to SR- Flip Flop	Remember	----	CO 11
6	How do you convert D- Flip Flop to JK- Flip Flop	Remember	----	CO 11
7	Explain the JK and Master slave Flip-flop? Give its timing waveform?	Understand	This would require the learner to **recall** the operation of JK flip-flop and race around condition. Then **explain** how the race around condition is eliminated in Master slave flip-flop with the help of timing waveforms.	CO 11
8	Explain the Ripple counter design procedure. Also design a decade counters.	Understand	This would require the learner to **recall** the design procedure of ripple counter. Then with the help of design procedure and **understand** the decade counter which can count 10 pulses.	CO 12
9	Construct a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter?	Understand	This would require the learner to **recall** the operation of Ring and Twisted Ring counter also the design procedure of synchronous counter. Then with the help of design procedure and **understand** the Ring counter and discuss the differences between Ring and Twisted Ring counter.	CO 12
10	Define JK – Flip-flop with the help of a logic diagram and characteristic table?	Understand	This would require the learner to **recall** the logic diagram and **understand** characteristic table of JK flip-flop.	CO 11
11	Explain the operation of RS and JK flip-flops with functional diagram and Truth tables. Also derive the characteristic equations.	Understand	This would require the learner to **recall** the logic diagram and characteristic table of RS and JK flip-flop. Then with the help of truth table and **explain** the characteristic equation of RS and JK flip-flop using K-map	CO 11
12	With the help of neat circuit diagram explain the working of Master Slave JK flip flop and also explain how race around condition is eliminated in it.	Understand	This would require the learner to **recall** the logic circuit and operation of Master slave JK flip-flop. Then **explain** how the race around condition is eliminated in Master slave flip-flop.	CO 11

13	Explain the operation of D and T flip-flops with functional diagram and Truth tables. Also derive the characteristic equations	Understand	This would require the learner to **recall** the logic diagram and characteristic table of D and T flip-flop. and **understand** the characteristic equation of D and T flip-flop.	CO 11
14	Develop a cyclic BCD up synchronous counter using T flip-flops	Apply	This would require the learner to **recall** the operation of T flip-flop **understand** the design procedure of synchronous counter ,to construct a BCD up synchronous counter using T flip-flops.	CO 12
15	Construct the transition table for the following flip-flops SR-F/F, D-F/F	Apply	This would require the learner to **recall** the logic diagram and understand characteristic table of D and SR flip-flop to **develop** the transition tables which can be used in conversion of flip-flops.	CO 11
16	Explain with a suitable logic and timing diagram: i) Serial-in-serial out shift register ii) Parallel-in-parallel-out unidirectional shift register.	Understand	This would require the learner to **recall** the concept of shift register. Then **explain** the operation of 4-bit shift register in SISO and PIPO modes with the help of logic and timing diagram.	CO 12
17	Construct a mod-11 up ripple counter using T flip-flops.	Apply	This would require the learner to **recall** the operation of T flip-flop and **understand** the design procedure of asynchronous counter to **construct** a Modulo-11ripple up counter using T flip-flops.	CO 12
18	Explain with a neat diagram and truth table, 4- bit SIPO shift register to store binary number 1011.	Understand	This would require the learner to **recall** the concept of shift register. Then **explain** the operation of 4-bit shift register in SIPO mode with the help of truth table and logic circuit.	CO 12
19	With neat logic diagram, explain the different modes of operation of universal shift register.	Understand	This would require the learner to **recall** the concept of universal shift register. Then **explain** its operation in different modes with the help of truth table and logic circuit.	CO 12
20	With the help of a schematic diagram, explain how a serial shift register can be transformed into a (i) ring counter (ii) Johnson counter.	Understand	This would require the learner to **recall** the concept of serial shift register. Then **explain** how it can be converted into a ring counter and Johnson counter.	CO 12
PART-C (Analytical Questions)				
1	Explain the working of 3-bit asynchronous up-down counter with necessary waveform and truth table.	Understand	This would require the learner to **recall** the concept of asynchronous counter. Then **explain** the operation of a 3-bit asynchronous up-down counter.	CO 12

2	Design a synchronous counter using JKFF to count the following sequence 0, 2, 5, 6, 0….. undesired states 1,3,4,7must go to 0 on the next clock pulse.	Apply	This would require the learner to **recall** the operation of JK flip-flop **understand the** design procedure of synchronous counter to **construct** a counter which can count the given sequence using JK flip-flops.	CO 12
3	Construct a 4-bit binary counter (using D flip flops) which counts all possible odd numbers only?	Apply	This would require the learner to **recall** the operation of D flip-flop and understand the design procedure of counter to **construct** a counter which can count all possible odd numbers only using D flip-flops.	CO 12
4	Develop a Modulo-12 Synchronous up counters using T-Flip Flops and draw the Circuit diagram.	Apply	This would require the learner to **recall** the operation of T flip-flop and understand the design procedure of synchronous counter. to **construct** a Modulo-12 counter using T flip-flops.	CO 12
5	How do you convert Jk- Flip Flop to D-Flip Flop	Remember	-----	CO 11
6	Construct a MOD-5 synchronous counter using flip flops and Implement it? Also draw the timing diagram?	Apply	This would require the learner to **recall** the concept of synchronous counter. **understand** the **design** procedure to construct a Mod-5 counter which can count the given sequence using JK flip-flops.	CO 12
7	Design a counter with the sequence 0,1,3,7,6,4,0 using JK FF	Apply	This would require the learner to **recall** the design procedure of synchronous counter **understand** the operation of JK-flip-flop. To **construct** a counter which can generate the given sequence using JK flip-flops?	CO 12
8	Build a 4- bit Twisted Ring counter using JK flip-flop?	Apply	This would require the learner to **recall** the design procedure of synchronous counter and **understand** the design procedure to **construct** a 4-bit twisted ring counter using JK flip-flops.	CO 12
9	Implement MOD5 up and Down counter?	Apply	This would require the learner to **recall** the design procedure of synchronous counter and **understand** of design procedure to **construct** a Mod-5 Up and Down counter	CO 12
10	How do you convert Jk- Flip Flop to T- Flip Flop	Remember	----	CO 11

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