INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

COMPUTER SCIENCE AND ENGINEERING

COURSE DESCRIPTOR

Course Title	**ANALOG AND DIGITAL ELECTRONICS**				
Course Code	AECB05				
Program	B.Tech				
Semester	THREE				
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	-	-
Course Coordinator	Ms.M.Lavanya, Assistant Professor				

I. COURSE OVERVIEW:

This course provides the basic knowledge over the construction and functionality of the basic electronic devices such as diodes and transistors. It also provides the information about the uncontrollable and controllable electronic switches and the flow of current through these switches in different biasing conditions and also will make them to learn the basic theory of switching circuits and their applications in specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuitsdetail. Starting from a problem statement they will learn to design circuits of logic gates that have a.They will learn to design counters, adders, sequence detectors.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B TECH	AHSB13	II	Semiconductor Physics

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIAExamination	Total Marks
Analog And Digital Electronics	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. **Therecouldbe a maximum of two sub divisions in aquestion.**

The expected percentage of cognitive level of the questions is broadly based on the criteria given in Table: 1.

Table 1: The expected percentage of cognitive level of questions in SEE.

Percentage of Cognitive Level	Blooms Taxonomy Level
10 %	Remember
50 %	Understand
25 %	Apply
15 %	Analyze
0 %	Evaluate
0 %	Create

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 2), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (Table 3).

Table 2: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams

Quiz –Online Examination:

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT):

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning center. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.The AAT chosen for this course is given in table 3**.**

Table 3: Assessment pattern for AAT

5 Minutes Video	Assignment	Tech-talk	Seminar	Open Ended Experiment
20%	30%	30%	10%	10%

VI. COURSE OBJECTIVES:

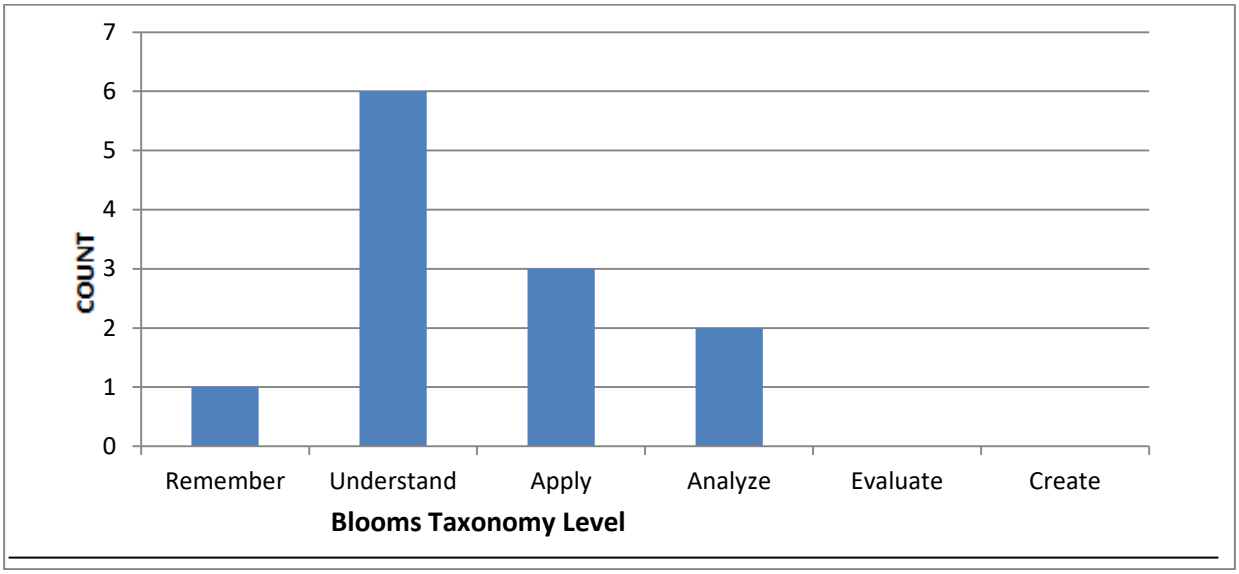
The students will try to learn:	
I	The Fundamental knowledge of the operational principles and characteristics of semiconductor devices and their applications.
II	The basic concept of number systems, Boolean algebra and optimized implementation of combinational and sequential circuits.
III	The perceive subsequent studies in the Area of microprocessors, microcontrollers, VLSI design and embedded systems effectively use of fundamentals of digital electronics.

VII. COURSE OUTCOMES:

After successful completion of the course, students will be able to:		
Course Outcomes		Knowledge Level (Bloom's Taxonomy)
CO 1	**Recall** the properties of semiconductor materials which form the basis for the formation of PN junction diode.	Remember

CO 2	**Illustrate** the volt-ampere characteristics of semiconductor devices for finding cut-in voltage, resistance and capacitance.	Understand
CO 3	**Apply** the pn junction characteristics for the diode applications such as switch and rectifiers.	Apply
CO 4	**Explain half** wave and full wave rectifier circuits with filter and without filtersfor conversion of alternating current in to direct current.	Understand
CO 5	**Interpret** DC and AC load line analysis of different amplifiers for optimal operating level regardless of input, load placed on the device.	Understand
CO 6	**Analyse** the input and output characteristics of transistor configurations and small signal h-parameter models for determining the input - output resistances, current gain and voltage gain	Analyze
CO 7	**Compare** the binary decimal, octal and hexadecimal number systems in terms of basic arithmetic operations.	Analyze
CO 8	**Identify** the functionality of logic gates, parity code and hamming code techniques for error detection and correction of single bit in digital systems.	Apply
CO 9	**Apply** Boolean postulates and theorems,k-map and tabular methods for obtaining minimized Boolean expressions.	Apply
CO 10	**Develop** gate level combinational circuits to built adders, subtractors, multiplexers, demultiplexers, encoder and decoders.	Apply
CO 11	**Describe** the operation of Flip-Flops and latches for constructing sequential circuits.	Understand
CO 12	**Implement** the synchronous& asynchronous counters for memory storing applications.	Apply

COURSE KNOWLEDGE COMPETENCY LEVELS



VIII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Strength	Proficiency Assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineeringfundamentals, and an	3	SEE, CIE, AAT, QUIZ

Program Outcomes		Strength	Proficiency Assessed by
	engineering specialization to the solution of complex engineering problems.		
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complexengineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	3	SEE, CIE, AAT, QUIZ
PO3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	SEE, CIE, AAT, QUIZ

3 = High; 2 = Medium; 1 = Low

IX. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Strength	Proficiency assessed by
PSO 1	Understand, design and analyze computer programs in the areas related to Algorithms, System Software, Web Design, Big data, Artificial Intelligence, Machine Learning and Networking.	1	Seminar

3 = High; 2 = Medium; 1 = Low

X. MAPPING OF EACH CO WITH PO(s), PSO(s):

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	√	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	√	√	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	-	√	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	√	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	√	-	√	-	-	-	-	-	-	-	-	-	-	-	-
CO 6	√	-	√	-	-	-	-	-	-	-	-	-	√	-	-
CO 7	√	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 8	√	√	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 9	√	√	-	-	-	-	-	-	-	-	-	-	√	-	-
CO 10	√	√	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 11	√	-	√	-	-	-	-	-	-	-	-	-	-	-	-
CO 12	-	√	√	-	-	-	-	-	-	-	-	-	√	-	-

XI. JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING –DIRECT

Course Outcomes	POs/ PSOs	Justification for mapping (Students will be able to)	No. of key competencies
CO1	**PO 1**	Recall the semiconductor device properties (**knowledge)** for understanding conduction, Fermi-levels, barrier potentials through energy band diagrams, diffusion and drift currents in the device characteristics by applying the principles of **science**	**1**
CO2	**PO 1**	Illustrate the volt-ampere characteristics (**knowledge**) of semiconductor devices to derive **mathematical model** for diode current, static and dynamic resistance by applying the principles of **mathematical** model and **science**	**2**
	PO 2	Understand the given **problem statement** and **formulate**the static and dynamic resistance from the volt-ampere characteristics of the semiconductor devicesusing **first principles of mathematics, natural sciences, and engineering sciences**	**5**
CO3	**PO 2**	Apply (**knowledge**) the given the diode application **problemstatement** and finding the **solution implementation** of rectifier circuits	**4**
CO4	**PO1**	Understand the pn junction characteristics for the diode applications of diode as switch, and rectifiers for **complex engineering problems** by applying the principlesof **mathematics, science**.	**2**
CO5	**PO 1**	Interpret (Understand) DC and AC load line analysis of different amplifiers for optimal operating level by applying**Mathematics, scienceengineering for complex engineering problems.**	**2**
	PO3	**Design** an amplifier from the AC and DC load line analysis by applying solutions for **complex engineering problems and design system components**.	**5**
CO6	**PO 1**	Analyse (Understand) the input and output characteristics of transistor configurations and determine the input output resistance, current and voltage gains by applying theprinciples of **mathematics, science**.	**2**
	PO3	**Design a transistor configuration and** find input andoutput characteristicsby applying in **design system components.**	**3**
	PSO1	Develop the capability to **analyze** and **design** simple circuits containing nonlinear elements such as transistors using the concepts of load lines, operating points and incremental analysis.	**2**
CO7	**PO 1**	Understand the number systems, binary addition and subtraction, 2's complement representation and operations, Complements of numbers, codes- binary codes, BCD code by applying its**mathematical properties**.	**1**
CO8	**PO 1**	Understand the **fundamentals** of basic logic gates and universal gate for the solution of **complex engineeringproblems** such as conversions of gates.	**2**
	PO2	Identify the given **problem statement** and solve it using error detecting and correcting codes by applying its **mathematical properties**.	**2**
CO9	**PO 1**	Identify the importance of SOP and POS canonical forms in the optimization of **conventional boolean** formulas in general and **digital circuits**.	**2**

Course Outcomes	POs/ PSOs	Justification for mapping (Students will be able to)	No. of key competencies
	PO 2	Understand the given **problem statement** and tabulate Unit distance code, alphanumeric codes, and error detecting and correcting codes by **using itsmathematical properties**.	**5**
	PSO1	Analyze the basic theorems and its properties, switching functions, canonical and standard form by applying its **mathematical models**.	**1**
CO10	**PO 1**	Demonstrate the design procedures of half and full Adders, subtractors, serial and parallel adders, BCD Adder for fundamental block realization in any processor **complex engineering problems** by applying the principlesof **mathematics**.	**2**
	PO 2	Explain the serial adder, 1's complement subtractor, 2's complement subtractor by applying Boolean **algebraic theorems**.	**1**
CO11	**PO 1**	Illustrate bi-stable elements like latches, flip-flop and illustrate the **excitation tables** of different flip flops for **memory storage elements**.	**2**
	PO3	**Development of solutions** for different data conversions of the flip flops by applying excitation tables and **design system components.**	**5**
CO12	**PO 2**	**Implement** the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops for **memory harvesting applications.**	**5**
	PO3	**Design solutions for**different type of counters using excitation table of flip flops by applying engineering **problems and design system components.**	**5**
	PSO 1	Develop the synchronous and asynchronous universal shift registers by applying the **fundamental blocks** of shift registers.	**1**

XII. TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAPPING

Course Outcomes	Program Outcomes / No. of Key Competencies Matched												Program Specific Outcomes/ Number of key competencies		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
	3	**10**	**10**	**11**	**1**	**5**	**3**	**3**	**12**	**5**	**12**	**12**	**2**	**2**	**2**
CO 1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	2	5	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	-	4	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	2	-	5	-	-	-	-	-	-	-	-	-	-	-	-
CO 6	2	-	3	-	-	-	-	-	-	-	-	-	1	-	-
CO 7	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-

CO 8	**2**	**2**	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 9	**2**	**5**	-	-	-	-	-	-	-	-	-	-	1	-	-
CO 10	**2**	**1**	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 11	**2**	-	**5**	-	-	-	-	-	-	-	-	-	-	-	-
CO 12	-	**5**	**5**	-	-	-	-	-	-	-	-	-	**1**	-	-

XIII. PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO, PSO):

Course Outcomes	**Program Outcomes / No. of key competencies**												**Program SpecificOutcomes / No. of key competencies**		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
	3	**10**	**10**	**11**	**1**	**5**	**3**	**3**	**12**	**5**	**12**	**12**	**2**	**1**	**2**
CO 1	33.3	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 2	66.7	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 3	0.0	40.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 4	66.7	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 5	66.7	50.0	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	100.0	0.0	0.0
CO 6	66.7	0.0	30.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 7	33.3	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 8	66.7	20.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 9	66.7	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	100.0	0.0	0.0
CO 10	66.7	10.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 11	66.7	0.0	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 12	0.0	50.0	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	100.0	0.0	0.0

XIV. COURSE ARTICULATION MATRIX (PO – PSO MAPPING)

COs and POs and COs and PSOs on the scale of 0 to 3, **0** being **no correlation**, **1** being the **low correlation**, **2** being **medium correlation** and **3** being **high correlation**.

0 – **0**≤ C≤ 5%–Nocorrelation; **2** – 40 % <C< 60%–Moderate.
1 – 5 <C≤ 40%– Low/ Slight; **3** – 60% ≤ C< 100%– Substantial /High

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	-	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	3	-	2	-	-	-	-	-	-	-	-	-	3	-	-
CO 6	3	-	1	-	-	-	-	-	-	-	-	-	-	-	-
CO 7	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 8	3	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 9	3	2	-	-	-	-	-	-	-	-	-	-	3	-	-
CO 10	3	1	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 11	3	-	2	-	-	-	-	-	-	-	-	-	-	-	-
CO 12	-	2	2	-	-	-	-	-	-	-	-	-	3	-	-
TOTAL	**26**	**10**	**7**	-	-	-	-	-	-	-	-	-	**9**	-	-
AVERAGE	**2.6**	**1.6**	**1.7**	-	-	-	-	-	-	-	-	-	**3**	-	-

XV. ASSESSMENT METHODOLOGY - DIRECT

CIE Exams	PO 1,PO 2	SEE Exams	PO 1,PO 2	Assignments	-	Seminars	PO 1
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	-						

XVI. ASSESSMENT METHODOLOGY - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✗	Assessment of Mini Projects by Experts		

XVII. SYLLABUS

MODULE-I	DIODE AND APPLICATIONS
Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times. Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive Filter	
MODULE-II	**BIPOLAR JUNCTION TRANSISTOR (BJT)**
Principle of Operation and characteristics - Common Emitter, Common Base, Common Collector Configurations, Operating point, DC & AC load lines, Transistor Hybrid parameter model, Determination of hparameters from transistor characteristics, Conversion of h-parameters.	
MODULE-III	**NUMBER SYSTEMS**
Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code. Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.	
MODULE-IV	**MINIMIZATION OF BOOLEAN FUNCTIONS**
Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method, Combinational Logic Circuits: Adders, Subtractors, comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations	
MODULE-V	**SEQUENTIAL CIRCUITS FUNDAMENTALS**
Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another. Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.	

Text Books:

1. Electronic Devices and Circuits "Jacob Millman", McGraw Hill Education, 2017
2. Electronic Devices and Circuits theory "Robert L. Boylestead, Louis Nashelsky",11th Edition, Pearson, 2009.
3. Switching and Finite Automata Theory, "ZviKohavi&Niraj K. Jha, 3rd Edition", Cambridge, 2010.
4. Modern Digital Electronics, "R. P. Jain, 3rd Edition", Tata McGraw-Hill, 2007.

Reference Books:

1. Pulse, Digital and Switching Waveforms, "J. Millman, H. Taub and Mothiki S. Prakash Rao", 2 Ed., McGraw Hill, 2008.
2. Electronic Devices and Circuits, "S. Salivahanan, N.Suresh Kumar, A Vallvaraj, 2nd Edition", TMH.
3. Digital Design, "Morris Mano", PHI, 4th Edition,2006.
4. Introduction to Switching Theory and Logic Design, "Fredriac J. Hill, Gerald R. Peterson",3rd Ed, John Wiley & Sons Inc.

XVIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Outcomes	Reference
1-5	Introduction to semiconductors, Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis.	CO 1	T2:1.1-1.8, 2.2
6-7	Diffusion and Transition Capacitances, Diode Applications, Switch-Switching times	CO 1	T2:1.10
8	Design Rectifier - Half Wave Rectifier & problems	CO 2	T2:2.7
9-10	Design Full Wave Rectifier & problems	CO 3	T2:2.8
11-12	Design Bridge Rectifier, Rectifiers with Capacitive Filter	CO 4	T2:2.8
15-16	Understand the concepts of Transistor operation	CO 6	T2:3.1-3.2
17-18	Characteristics of CB,CE,CC	CO 8	T2:3.3-3.7
19-21	Operating point, DC & AC load line Analysis & problems	CO 7	T2:4.2,7.1-7.4
22-25	Transistor Hybrid parameter model, Determination of h-parameters from transistor characteristics, Conversion of h-parameters.	CO 9	T2: 7.6 7.7, 8.9-8.10
26-27	Understand the need for digital systems, review of number systems, number base conversion	CO 10	T3:1.1 R3:1.1-1.4
28-30	Complements of numbers, Weighted codes & Non-weighted codes.	CO 11	T3:1.1-1.2 R3:1.5-1.7
31-32	error detecting and correcting codes, Digital Logic Gates	CO 12	T3:1.3 R3:1.7,7.4
33-35	Basic Theorems and Properties, Algebraic Simplification,	CO 13	T3:3.1-3.4 R3:2.1-2.4
36-37	Canonical and Standard Form	CO 14	T3:3.3-3.5 R3:2.6
38-39	Universal Gates, Multilevel NAND/NOR realizations.	CO 16	T3:5.1-5.3 R3:2.8,3.7-3.8
40-43	Identify basic building blocks of digital systems and Minimization using three variable; four variable; five variable K-Maps; Don‘t Care Conditions.	CO 15	T4:5.1.-5.10 R3:3.6
44-45	Understand Tabular Method	CO 15	T3:4.4-4.6 T4: 5.11 R3:3.10
46-47	Design Combinational Logic Circuits adders, subtractors.	CO 17	T4:6.1,6.4 R3:4.1-4.5
48-49	Design different combinational logic circuits comparators Multiplexers, Demultiplexer.	CO 14	T4:6.2-6.3,6.7 R3:4.8,4.11
50-51	Demonstrate the Encoders, Decoders.	CO 18	T4:6.3,6.10 R3:4.9-4.10
52-54	Code converters, Hazards & Hazard Free Relations	CO 18	T4:6.9,5.12
55	Combinational and sequential circuits, the binary cell, the Fundamentals of sequential machine operation, SR-Latch	CO 19	T4:7.1 R3:5.2-5.3
56-58	Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops. Timing & Triggering	CO 19	T4:7.2-7.6 R3:5.4-5.5
59-60	Excitation tables of Flip-flops, Conversion from one type of Flip-Flop to another	CO 19	T4:7.7-7.10 R3:5.5

61	Draw and explain about Shift Registers	CO 20	T4:8.1-8.3 R3:6.1-6.2
62	Implement Synchronous, Asynchronous Counters using flip flops	CO 21	T4:8.4-8.7 R3:6.3-6.5

Prepared By:
Ms M.Lavanya, Assistant Professor **HOD, CSE**