INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION FORM

Course Title	**DIGITAL DESIGN USING VERILOG HDL**			
Course Code	A40410			
Regulation	**R13-JNTUH**			
Course Structure	Lectures	Tutorials	Practicals	Credits
	5	-	-	4
Course Coordinator	Mr. D. Khalandar Basha, Associate Professor			
Team of Instructors	Mr. K. Arun sai, Assistant Professor, Mr. K Sudhakar Reddy, Assistant Professor, Mr. N Nagaraju, Assistant Professor			

I. COURSE OVERVIEW:

This course teaches designing digital circuits, behavioral and RTL modeling of digital circuits using Verilog HDL, verifying these models, and synthesizing RTL models to standard cell libraries and FPGAs. Students gain practical experience by designing, modeling, implementing and verifying several digital circuits

II. PREREQUISITE(S):

Level	Credits	Periods / Week	Prerequisites
UG	4	5	Switching Theory and Logic Design Good logical skills and logical analysis

III. COURSE ASSESMENT METHODS:

Sessional Marks (25 Marks)	University End Exam Marks	Total Marks
Mid Semester Test There shall be 2 midterm examinations. Each midterm examination consists of subjective type and Objective type tests. The subjective test is for 10 marks, with duration of 1 hour. The objective type test is for 10 marks with duration of 20minutes. It consists of 10 Multiple choice and 10 fill in the blanks. The student has to answer all the questions and each carries half mark. First midterm examination shall be conducted for the first two and half units of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. Marks shall be awarded considering the average of two midterm examinations in each course reason whatsoever, will get zero marks(s).	75	100

IV. EVALUATION SCHEME:

Mid Semester Test	25 marks
End Semester Examination	75 marks

V. COURSE OBJECTIVES:

1. To enable the student to Design digital circuits, Behavioral and RTL modelling of digital circuits using Verilog HDL.
2. To provide the student verifying the models.
3. To enable the student to synthesizing RTL models to standard cell libraries and FPGAs
4. To enable the student to gain practical experience by designing, modelling, implementing and verifying several digital circuits.
5. To provide student with Design Digital components and circuits that are testable, reusable and synthesizable

VI. COURSE OUTCOMES:

1. Describe Verilog Hardware Description Language
2. Lists various constructs and features in Verilog HDL
3. Model various designs in gate level modeling
4. Model various designs in data flow modeling
5. Model various designs in gate level modeling
6. Model various designs in behavioral level modeling
7. Model various designs in switch level modeling
8. Construct Test benches examine the functionality of the designs using behavioral model
9. Identify various Sequential Models
10. Design FSMs
11. Tests designs using various techniques
12. Write register transfer level (RTL) models of digital circuits.
13. Verify behavioral and RTL model.
14. Describe standard cell libraries and FPGAs
15. Synthesize RTL models to Standard cell libraries and FPGAs
16. Implement RTL models on FPGAs and testing & verification

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Level	Proficiency assessed by
PO1	**Engineering Knowledge** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems	S	Assignments
PO2	**Problem Analysis**	S	--

	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences		
PO3	**Design/Development of Solutions** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	H	Practice Sessions
PO4	**Conduct Investigations of Complex Problems** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions	S	Design Exercises
PO5	**Modern Tool Usage** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	H	Design Exercises Seminars, Paper Presentations
PO6	**The Engineer And Society** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice	N	--
PO7	**Environment and sustainability** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development	N	--
PO8	**Ethics** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice	N	--
PO9	**Individual and Team Work** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings	H	Projects
PO10	**Communication** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions	S	Document Preparation and Presentation
PO11	**Project management and finance** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments	H	Seminars Discussions
PO12	**Life-long learning** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change	H	Development of Prototype, Mini Projects

N = None **S = Supportive** **H = Highly Related**

VIII. HOW PROGRAM OUTCOMES ARE ASSESSED:

PROGRAM SPECIFIC OUTCOMES		LEVEL	PROFICIENCY ASSESSED BY
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	H	Lectures and Assignments
PSO 2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	S	Tutorials
PSO 3	**Successful career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	S	Seminars and Projects

IX. SYLLABUS:

UNIT - I

INTRODUCTION TO VERILOG:

Verilog as HDL, Levels of design Description, Concurrency, Simulation and Synthesis, Functional verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS:

Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT - II

GATE LEVEL MODELING:

Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State gates, Array of Instances of Primitives, Design of Flip – Flops with gate primitives, Delays, Strengths and contention Resolution, Net Types, Design of Basic Circuits.

MODELING AT DATA FLOW LEVEL:

Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to vectors, Operators.

UNIT - III

BEHAVIORAL MODELING:

Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, assignments with Delays, Wait Construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-Blocking Assignments, The case statement, Simulation Flow if and if-else constructs, assign–deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT - IV

SWITCH LEVEL MODELLING:

Basic Transistor Switches, CMOS Switch, Bi – directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES:

Parameters, Path Delays, Module Parameters, System Tasks and Functions, File – Based Tasks and Functions, Compiler Directives, Hierarchical Access, User-defined Primitives (UDP).

UNIT – V

SEQUENTIAL CIRCUIT DESCRIPTION:

Sequential Models – Feedback Model, Capacitive Model, Implicit Model, Basic Memory Components, Functional Register, Static Machine Coding, Sequential Synthesis

Component Test and Verification: Test bench – Combinational Circuit Testing, Sequential Circuit Testing, Test bench Techniques, Design Verification, Assertion Verification.

TEXT BOOKS:

1. T. R. Padmanabhan and B. Bala Tripura Sundari, Design through Verilog HDL –Wiley, 2009.**(T1)**
2. Zainalabdien Navabi, Verilog Digital System Design, TMH, 2nd Edition **(T2)**

REFERENCE BOOKS:

1. Fundamentals of Digital Logic design with Verilog Design – Stephen Brown and Zvonko Vranesic, TMH, 2nd Edition, 2010. **(R1)**
2. Advanced Digital Logic Design using Verilog, State Machine & Synthesis for FPGA – Sunggu Lee, Cengage Learning, 2012 **(R2)**
3. Verilog HDL – Samir Palnitkar, 2nd Edition, Pearson Education, 2009. **(R3)**
4. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005 **(R4)**

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following course learning outcomes:

Lecture No.	CLO	Unit	Course Learning Outcomes	Topics to be covered	Reference
1-3	1	I	**Outline** the importance of HDL in VLSI domain	Introduction To Verilog, Need of VLSI and HDLs	T1:1
4	2		**Identify** the various design styles in Verilog	Verilog as HDL, Levels of design Description	T1:2.1-2.2
5-7	3		**List** and Memorize the features of Verilog HDL.	Concurrency, Simulation and Synthesis Functional, Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.	T1: 2.3-2.10
8-11	4		**Indicates** the constructs inVerilog HDL	Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.	T1: 3.2 – 3.14
12	**5**	**II**	**Discuss** the constructs for gate level modelling	Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives	T1: 4.1 – 4.4

Lecture No.	CLO	Unit	Course Learning Outcomes	Topics to be covered	Reference
13-15	6		**Design**s gate level models	Illustrative Examples,	T1: 4.5
16	**7**		**Discuss** tri state gates	Tri-State Gates, Array of Instances of Primitives	T1: 4.6 – 4.7
17-19	**8**		**Design**s flip flop using Verilog	Design of Flip – Flops with gate primitives	T1: 5.2
20-21	**9**		**Lists** various delays in gate level modelling	Delays, Strengths and Contention Resolution, Net Types	T1: 5.3-5.5
22-24	**10**		**Design**s Verilog modules	Design of Basic Circuits.	T1: 5.6
25-27	**11**		**Identify** assignment statements in data flow model along with delays and vectors. **Lists** various operators	Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors. Operators (Unary, Binary, ternary)	T1: 6.2 – 6.5
28-30	**12**		**Design** data flow models	Examples	T1: 6.6
30-31	**13**	**III**	**Identify** the important features of behavioral modeling	Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct	T1: 7.1 – 7.5
32-33	**14**		**Design**s Verilog modules	Examples	T1: 7.6
34	**15**		**Lists** the delay features of behavioral modelling, wait construct	Assignments with Delays, *Wait* Construct, Multiple Always Blocks	T1: 7.7 – 7.9
35-36	**16**		**Designs** Verilog modules	Designs at Behavioral Level	T1: 7.10
37	**17**		**Differentiate** blocking and non-blocking statement	Blocking and Non-Blocking Assignments,	T1: 7.11
38	**18**		**Illustrate** Case construct and simulation flow	The case statement, Simulation Flow	T1: 7.12
39-40	**19**		**Illustrate** if, assign-deassign, repeat, for, disable, while, forever constructs	*if* and *if-else* constructs, *assign–deassign* construct, *repeat* construct, *for* loop, the *disable* construct, *while* loop, *forever* loop	T1: 8.2 – 8.8
41	**20**		**Illustrate** parallel blocks, force- release and event constructs	parallel blocks, *force-release* construct, Event.	T1 : 8.9 – 8.11
42-44	**21**		**Design**s Verilog modules	Exercises	T1: 8.12
45-47	**22**	**IV**	**Outline** basic switches in Verilog with delays, strength contention	Basic Transistor Switches, CMOS Switch, Bi – directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets.	T1: 10.2 – 10.7
48	**23**		**Discuss** parameter and path delay in behavioral modeling	Parameters, Path Delays, Module Parameters	T1: 11.2 – 11.4
49-50	**24**		**Lists** system tasks and functions in Verilog	System Tasks and Functions, File – Based Tasks and Functions, Compiler Directives, Hierarchical Access	T1: 11.5 – 11.8
51 -52	**25**		**Demonstrate** UDPs	User-defined Primitives (UDP).	T1: 9.4
53-54	**26**	**V**	**Classify** sequential models	Sequential Models – Feedback Model, Capacitive Model, Implicit	T2: 5.1

Lecture No.	CLO	Unit	Course Learning Outcomes	Topics to be covered	Reference
				Model	
55-56	**27**		**Demonstrate** memory design in Verilog	Basic Memory Components	T2: 5.2
57-58	**28**		**Discuss** various functional register	Functional Register	T2: 5.3
59-60	**29**		**Illustrate** Static machine coding	Static Machine Coding	T2: 5.4
61-62	**30**		**Explain** sequential synthesis	Sequential Synthesis	T2: 5.5
63	**31**		**Model** Test benches for both combinational and sequential circuits	Test bench – Combinational Circuit Testing, Sequential Circuit Testing	T2: 6.1
64	**32**		**Describe** test bench techniques	Test bench Techniques	T2: 6.2
65	**33**		**Describe** design verification and assertion verification	Design Verification, Assertion Verification	T2: 6.4,6.5

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAMME OUTCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	S	H	H			S			S				H		
2	H		S						H				S		
3	S	H	S			H	S		S		S		S		
4	H		S						H					S	
5	S	S	S		S						H	S			S
6		S			H							S			S

S = Supportive **H = Highly Related**

XII. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAMME OUTCOMES:

Course Outcomes	Program Outcomes													Program Specific Outcomes		
	PO 1	PO 2	PO 3	PO 3	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PO 13	PSO 1	PSO 2	PSO 3
1	H		S		S						H		S	H		
2			S								S		H	H		
3	H		S		S						H			S		
4	S		S		H								S	S		
5	S				S						H		S	H		
6	S		S		H										H	
7	H				S						S		S		S	

8	S		H		H										S	
9													S			S
10	H		S		H						S					S

S = Supportive **H = Highly Related**

Prepared By: Mr. D. Khalandar Basha, Associate Professor

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