INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

COMPUTER SCIENCE AND ENGINEERING

COURSE DESCRIPTION FORM

Course Title	**DIGITAL LOGIC DESIGN**			
Course Code	**A30401**			
Regulation	**R15 - JNTUH**			
Course Structure	Lectures	Tutorials	Practicals	Credits
	4	-	-	4
Course Coordinator	Ms.C.Deepthi Associate Professor, ECE			
Team of Instructors	Mr.C.Srihari, Assistant Professor, ECE Ms. Parvathy Sreekumar, Assistant Professor, ECE Mr.R.Gangadhar Reddy, Assistant Professor, ECE			

I. COURSE OVERVIEW:

The course addresses the concepts, principles and techniques of designing digital systems. The course teaches the fundamentals of digital systems applying the logic design and development techniques. This course forms the basis for the study of advanced subjects like Computer Architecture and Organization, Microprocessor through Interfacing and VLSI Design. Students will learn principles of digital systems logic design and distinguish between analog and digital representations. They will be able to analyze a given combinational or sequential circuit using k-map and Boolean algebra as a tool to simplify and design logic circuits. Construct and analyze the operation of a latch, flip-flop and its application in synchronous circuits.

II. PREREQUISITE(S):

Level	Credits	Periods/ Week	Prerequisites
UG	4	4	Engineering physics

III. MARKS DISTRIBUTION:

Sessional Marks	University End Exam marks	Total marks
Midterm Test There shall be two midterm examinations. Each midterm examination consists of essay paper, objective paper and assignment. The essay paper is for 10 marks of 60 minutes duration and shall contain 4 questions. The student has to answer 2 questions, each carrying 5 marks. The objective paper is for 10 marks of 20 minutes duration. It consists of 10	75	100

multiple choice and 10 fill-in-the blank questions, the student has to answer all the questions and each carries half mark. First midterm examination shall be conducted for the first two and half units of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are earmarked for assignments. There shall be two assignments in every theory course. Assignments are usually issued at the time of		
Sessional Marks	**University End Exam marks**	**Total marks**
commencement of the semester. These are of problem solving in nature with critical thinking. Marks shall be awarded considering the average of two midterm tests in each course.		

IV. EVALUATION SCHEME:

S. No	Component	Duration	Marks
1.	I Mid Examination	80 minutes	20
2.	I Assignment	-	5
3.	II Mid Examination	80 minutes	20
4.	II Assignment	-	5
5.	External Examination	3 hours	75

V. COURSE OBJECTIVES:

At the end of the course, the students will be able to:

I. Be familiar with number systems and Boolean algebra principles.
II. Be familiar Boolean functions, simplification methods and realization.
III. Master in analyzing combinational logic circuits and implementations.
IV. Master in analyzing sequential logic circuits and implementations.
V. Be familiar with synchronous and asynchronous sequential circuits. VI. Be familiar with memories like ROM, RAM, PAL and PLA.
VII. Master in analyzing gate level circuits and implementations.

VI. COURSE OUTCOMES:

After completing this course the student must demonstrate the knowledge and ability to:

1. **Understand**number systems, binary addition and subtraction, 2's complement representation and operations with this representation.
2. **Discuss** about digital logic gates and their properties.
3. **Explain** switching algebra theorems and apply them for logic functions.
4. **Identify** the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.

5. **Evaluate** functions using various types of minimizing algorithms like Boolean algebra, Karnaugh map or tabulation method.
6. **Understand** bi-stable elements and different types of latches and flip-flops.
7. **Analyze** the design procedures of Combinational and Sequential logic circuits.
8. **Design** gate level minimizations along with K-map techniques.
9. **Analyze** memory organizations, PAL, PLA and memory hierarchy concepts.
10. **Understand** about Asynchronous Sequential Circuits: reduction of state and follow tables, role free conditions.

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Level	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineeringfundamentals, and an engineering specialization to the solution of complex engineering problems.	H	Assignments, Tutorials
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complexengineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	H	Assignments
PO3	**Design/development of solutions**: Design solutions for complex engineering problems anddesign system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	S	Mini Projects
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and researchmethods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	S	Projects
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modernengineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	S	Mini Projects
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assesssocietal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	N	--
PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutionsin societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	N	--
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms ofthe engineering practice.	S	Assignments
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader indiverse teams, and in multidisciplinary settings.	S	Mini Projects
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineeringcommunity and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and	N	--

	receive clear instructions.		
PO11	**Project management and finance**: Demonstrate knowledge and understanding of theengineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	S	Projects
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage inindependent and life-long learning in the broadest context of technological change.	S	Projects

N - None **S - Supportive** **H - Highly Related**

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO1	**Professional Skills:** The ability to research, understand and implement computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient analysis and design of computer-based systems of varying complexity.	H	Lectures, Assignments
PSO2	**Problem-Solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	H	Projects
PSO3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	S	Guest Lectures

N - None **S - Supportive** **H - Highly Related**

IX. SYLLABUS:

UNIT – I

Digital Systems - Binary Numbers, Octal, hexadecimal and other base numbers, number base conversions, complements, signed binary numbers, floating point number representation, binary codes, error detecting and correcting codes, digital logic gates(AND, NAND,OR,NOR, Ex-OR, Ex-NOR), Boolean algebra , basic theorems and properties, Boolean functions, canonical and standard forms.

UNIT – II

GATE LEVEL MINIMIZATION: Gate –Level minimization and combination circuits , The K-Maps methods, three variable, four variable, five variable , sum of products , product of sums simplification, don't care conditions , NAND and NOR implementation and other two level implantation..

UNIT – III

Combinational Circuits (CC): Design procedure, combinational circuit for different code converters and other problems, binary adder, subtractor, multiplier, magnitude comparator, decoders, encoders, multiplexers, de- multiplexers

UNIT – IV

Synchronous Sequential Circuits: latches, flip-flops, analysis of clocked sequential circuits, design of counters, up-down counters, ripple counters, registers, shift registers, synchronous counters. Asynchronous sequential circuits: reduction of state and follow tables, role free conditions.

UNIT – V

Memory: random access memory, types of ROM, memory decoding, address and data bus, sequential memory, cache memory, programmable logic arrays, memory hierarchy in terms of capacity and access time.

Text books:

1.M. Morris Mano, Michael D. Ciletti, "Digital Design", 4e, Pearson Education/PHI, India, 2008.

References:

1. C.V.S. Rao, "Switching and Logic Design", 3e, Pearson Education, India, 2009.
2. Donald D. Givone, "Digital Principles and Design", Tata McGraw Hill, India, 2002.
3. Roth, "Fundamentals of Logic Design", 5e, Thomson, 2004.

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following course learning outcomes:

Lecture No.	Topics to be covered	Course Learning Outcomes	Reference
1 – 3	Introduction to digital systems, evolution and use of digital system, binary numbers, number base conversions, octal and hexadecimal numbers.	**Understand** the need for digital systems	T1: 1.3
4 – 6	Complements, signed binary numbers, binary codes, binary storage and registers, binary logic.	**Understand** the arithmetic operations carried by digital systems	T1: 1.5
7-10	Basic definitions, axiomatic definition of Boolean algebra, basic theorems and properties of Boolean algebra. Boolean functions, canonical and standard forms, logic operations in Boolean algebra.	**Learn** Boolean algebra and logical operations in Boolean algebra.	T1: 2.1
11 -14	Digital logic gates, product of sums simplification, don't-care conditions, sum of products simplification.	**Identify** basic building blocks of digital systems.	T1: 4.1, 4.2, 4.5, 4.8
15-16	NAND and NOR implementation, AND-ORINVERT,OR-AND-INVERT implementations, exclusive – OR function	**Design** functions using universal gates.	T1: 2.1, 2.2, 2.5, 4.7
17-19	Variable entered mapping, tabulation (Quine Mc Cluskey) method, determination and selection of prime implicants.	**Analyze** to avoid the redundant terms in Boolean functions.	T1: 3.1, 3.2, 4.3
20 - 23	Introduction, combinational circuits. Analysis procedure, design procedure of combinational logic circuits	**Discuss** the availability of different logic circuits.	T1: 3.6
24-27	Binary adder, binary subtractor, decimal adder, binary multiplier, magnitude comparator, decoder, encoders, multiplexers, sequential circuits, latches, flip-flops, analysis of clocked sequential circuits.	**Design**different combinational and sequential logic circuits.	T1: 3.3, 4.3

28-31	State reduction and assignment design procedure. clocked sequential circuits, registers, shift registers.	**Demonstrate** the design of sequential logic circuits..	T1: 3.4, 4.3
32-37	Ripple counters, synchronous counters, counter with unused states, ring counter, Johnson counter.	**Differentiate** types of counters.	T1: 5.1, 5.2
38-39	Introduction, Random-access memory, memory decoding	**Learn** various types of data storages.	T1: 5.3, 5.5
40-44	Error detection and correction, read-only memory, programmable logic array, programmable array logic.	**Discuss** error detection and correction in digital systems.	T1: 5.6
45-47	Sequential programmable devices. Flip-flops, latches and counters.	**Understand** construction of sequential programmable devices.	T1: 6.1, 6.2
48-49	Timing considerations, design with multiplexers, demultiplexers, encoders, decoders.	**Analyze** the concepts of multiplexers, encoders	T1: 1.3
50-52	Introduction, analysis procedure of asynchronous sequential logic, circuits with latches, design procedure, reduction of state and flow tables, race-free state assignment hazards.	**Demonstrate**the working of asynchronous sequential circuits.	T1: 8.2
53-55	Random access memory, types of ROM, memory decoding, address and data bus, sequential memory, cache memory, programmable logic arrays, memory hierarchy in terms of capacity and access time.	**Understand** the concept of memory hierarchy.	T1: 1.3, 7.2, 7.3, 7.6, 7.9

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
I	H	H										S	H	S	
II	S	H	H										H	S	
III		H	S	S									S	H	
IV	H	S											H	S	
V					S								H		S
VI		H	H		S								H	S	S
VII	S	S	H									S	H	H	S

S - Supportive H - Highly Related

XII. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	H	S	S										H	S	
2	H			S									S	H	
3			H		S								H	S	
4	S	H											S	H	
5	H	S											S	H	
6	H			S								S	H	S	
7	S			H					S		S		S	H	
8	S	H											H	S	
9			H	H	S				S		S	S	S	H	
10	H			S									S	H	S
11	H			S	S								H	S	
12	H		H									S	S	H	S

S - Supportive H - Highly Related

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