INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

COMPUTER SCIENCE ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL LOGIC DESIGN**				
Course Code	AEC020				
Programme	B.Tech				
Semester	III	CSE | IT			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Mrs. L Sruthi, Assistant Professor , ECE				
Course Faculty	Mrs. L Sruthi, Assistant Professor , ECE Mrs. J Swetha, Assistant Professor , ECE Mrs. V Bindusree, Assistant Professor , ECE				

I.   COURSE OVERVIEW:

The course will make them learn the basic theory of microprocessor and their applications in detail. Subsequently the course covers important concepts like how to write an assembly language programming. They will learn to write an assembly language programming for interfacing various I/O modules. They will learn to design different advance architectures to design a new communication interfaces.

II.   COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC005	II	Fundamentals of Electrical and Electronics Engineering	4

III.   MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital Logic Design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Quiz
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignments
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Seminars

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes (PSOs)	Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand ,analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based system of varying complexity.	2	Seminars and Assignments
PSO 2	**Software Engineering Practices:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	2	Quiz and Assignments
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra.
II	Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip flops and latches.
III	Understand about synchronous and asynchronous sequential logic circuits.
IV	Impart the basic understanding of memory organization, ROM, RAM, PLA and PAL.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC020.01	CLO 1	Understand the basic concept of number systems, binary addition and subtraction for digital systems.	PO 1	3
AEC020.02	CLO 2	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.	PO 1	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC020.03	CLO 3	Discuss about digital logic gates, error detecting and correcting codes for digital systems.	PO 1	3
AEC020.04	CLO 4	Describe the importance of SOP and POS canonical forms with examples.	PO 2	2
AEC020.05	CLO 5	Describe minimization techniques and other optimization techniques for Boolean formulas in general and digital circuits.	PO 2	2
AEC020.06	CLO 6	Evaluate Boolean algebra expressions by minimizing algorithms like sop and pos using Boolean Postulates and theorems.	PO 2	2
AEC020.07	CLO 7	Solve various Boolean algebraic functions using Karnaugh map and Tabulation Method.	PO 2	2
AEC020.08	CLO 8	Understand bi-stable elements and different type's combinational logic circuits.	PO 1	3
AEC020.09	CLO 9	Analyze the design procedures of Sequential logic circuits with the help of registers.	PO 1	3
AEC020.10	CLO 10	Discuss the concept of flip flops and latches by using sequential logic circuits.	PO 2	2
AEC020.11	CLO 11	Differentiate combinational logic circuits with sequential logic circuits along with examples.	PO 4	1
AEC020.12	CLO 12	Understand the concept of memory organization, read only memory and random access memory.	PO 1	3
AEC020.13	CLO 13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	PO 1	3
AEC020.14	CLO 14	Explain the concept of memory hierarchy in terms of capacity and access time.	PO 1	3
AEC020.15	CLO 15	Explain about Synchronous and Asynchronous Sequential Circuits: Reduction of state tables for Mealy and Moore machines.	PO 2	2
AEC020.15	CLO 16	Discuss about various memory concepts with respect to temporary and permanent memory organizations.	PO 1	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	2												2	2	
CLO 2	3												1		
CLO 3													3		
CLO 4		2											1		
CLO 5		2													
CLO 6		3												3	

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 7		2												2	
CLO 8	3												2		
CLO 9	2													2	
CLO 10		2													
CLO 11				2											
CLO 12	3														
CLO 13	2												1		
CLO 14	3														
CLO 15		2											2	2	
CLO 16		2											1		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2	SEE Exams	PO 1, PO 2	Assignments	PO 2	Seminars	PO 4
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 4						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

UNIT-I	NUMBER SYSTEMS AND CODES

Review of number systems, number base conversion; Binary arithmetic: Binary weighted and non-weighted codes; Complements: Signed binary numbers; Error Detection and Correcting Codes; Binary logic.

UNIT-II	BOOLEAN ALGEBRA AND GATE LEVEL MINIMIZATION

Postulates and theorems; representation of switching functions; SOP and POS forms; Canonical forms; Digital logic gates; Karnaugh Maps: Minimization using three variable; four variable; five variable KMaps; Don't Care Conditions; NAND and NOR implementation; Other Two-Level Implementation; Exclusive – OR function.

UNIT-III	DESIGN OF COMBINATIONAL CIRCUITS (CC)

Combinational Circuits: Analysis and Design Procedure; Binary adder and subtractors; Carry Look-a-head adder; Binary multiplier.

	Magnitude comparator;BCD adder; Decoders; Encoders; Multiplexers; Demultiplexer.
UNIT-IV	**DESIGN OF SEQUENTIAL CIRCUITS**
	Combinational Vs Sequential Circuits ; Latches, Flip Flops: RS flip flop, JK flip flop, T flip flop, D flip flop, Master-Slave Flip flop, Flip Flops excitation functions; Conversion of one flip flop to another flip flop; Shift Registers; Design of Asynchronous and Synchronous circuits; State Table, State diagram, State Reduction and State Assignment for Mealy and Moore Machines..
UNIT-V	**MEMORY**
	Random access memory; Types of ROM; Memory decoding; Address and Data bus; Sequential memory; Cache memory; Programmable logic arrays; Memory hierarchy in terms of capacity and access time

Text Books:

1. M. Morris Mano, Digital Design‖, Pearson Education/PHI, 3ʳᵈEdition 2001.
2. Charles H. Roth, Jr,Fundamentals of Logic Design‖, Thomson Brooks/Cole, 5thEdition, 2004.

Reference Books:

1. C. V. S. Rao, Switching Theory and Logic Design, Pearson Education, 1ˢᵗEdition, 2005.
2. M. Rafiquzzaman, Fundamentals of Digital Logic & Micro Computer Design‖, John Wiley, 5ᵗʰEdition, 2005.
3. Zvi. Kohavi, Switching and Finite Automata Theory‖, Tata McGraw-Hill, 2ⁿᵈEdition 1991.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Understand the need for digital systems, review of number systems, number base conversion	CLO 1	T1:1.1
6-10	Understand the arithmetic operations carried by digital systems.	CLO 4	T1:1.5
11-15	Learn Boolean algebra and Logical operations in Boolean algebra.	CLO 4	T1:2.2
16-20	Identify basic building blocks of digital systems and Minimization using three variable; four variable; five variable K-Maps; Don't Care Conditions.	CLO 5	T1:2.8
21-25	Discuss the Bistable multi with triggering methods. Fixed bias, self bias, unsymmetrical triggering, symmetrical triggering.	CLO 2	T1:3.5
26-28	Design functions using universal gates. NAND and NOR implementation; Other Two-Level Implementation; Exclusive –OR function.	CLO 6	T2:0.1
29-30	Discuss the availability of different logic circuits..	CLO 12	T2:3.2
31-35	Design different combinational logic circuits comparators multiplexers.	CLO 14	T1:3.1
36-40	Demonstrate the design of sequential logic circuits.	CLO 10	T1:4.3
41-44	Identify the significance of Master-Slave Flip flop.	CLO 13	T1:6.1
45-52	Design Flip Flops excitation functions; Conversion of one flip flop to another flip flop	CLO 15	R1:5.1
53-58	Understand and analyze the state tables, state diagram and state excitation table.	CLO 16	R1:5.3

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. N0	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Practical use of number systems	Seminars / NPTEL/Assignments	PO 1, PO 2	PSO 1
2	Applications of flipflops and latches	Seminars / NPTEL	PO 2, PO 4	PSO 1
3	Designing of circuits using flipflops and latches.	Guest Lecture	PO 1, PO 2	PSO 2

Prepared by:

Mrs. L Sruthi, Assistant Professor, ECE

HOD, CSE