INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL SYSTEM DESIGN**				
Course Code	AEC002				
Programme	B.Tech				
Semester	III	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Dr. K Nehru, Professor				
Course Faculty	Dr. Lalith Kumar Kaul, Professor Dr. P Munaswamy, Professor Mr. C Srihari, Assistant Professor				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
-	-	-	-

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital System Design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✔	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Presentation on real-world problems
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	3	Seminar
PO 9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary Settings.	2	Videos

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand, analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based systems of varying complexity.	2	Seminar
PSO 2	**Problem-Solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	-	-
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Formulate and solve problems involving number systems and operations related to them and generate different digital codes.
II	Describe and analyze functions of logic gates and optimize the logic functions using K -map and Quine - McClusky methods.
III	Demonstrate knowledge of combinational and sequential logic circuits elements like Adders, Multipliers, flip-flops and use them in the design of latches, counters, sequence detectors, and similar circuits.
IV	Design a simple finite state machine from a specification and be able to implement this in gates and edge triggered flip-flops.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC002.01	CLO 1	Understand number systems, binary addition and subtraction, 2"s complement representation and operations with this representation and understand the different binary codes.	PO 1	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC002.02	CLO 2	Illustrate the switching algebra theorems and apply them for reduction of Boolean function.	PO 1	2
AEC002.03	CLO 3	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	PO 1	3
AEC002.04	CLO 4	Discuss about digital logic gates and their properties, and implement logic gates using universal gates.	PO 1	3
AEC002.05	CLO 5	Evaluate functions using various types of minimizing algorithms like Boolean algebra.	PO 1	1
AEC002.06	CLO 6	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	PO 5	3
AEC002.07	CLO 7	Design Gate level minimization using K-Maps and realize the Boolean function using logic gates.	PO 5	3
AEC002.08	CLO 8	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	PO 5	1
AEC002.09	CLO 9	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.	PO 5	3
AEC002.10	CLO 10	Analyze and apply the design procedures of small sequential circuits to build the gated latches.	PO 5	2
AEC002.11	CLO 11	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	PO 5	2
AEC002.12	CLO 12	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 5	3
AEC002.13	CLO 13	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 5	2
AEC002.14	CLO 14	Understand and analyze the design of a finite state machine and implement Moore and mealy machine.	PO 5, PO 9	2
AEC002.15	CLO 15	Understand and analyze the merger chart methods like merger graphs, merger table for completely and incompletely specified machines.	PO 9	2
AEC002.16	CLO 16	Apply the concept of digital logic circuits to understand and analyze real time applications.	PO 9	1
AEC002.17	CLO 17	Acquire the knowledge and develop capability to succeed national and international level competitive examinations.	PO 5, PO 9	1.5

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3												3		
CLO 2	2												2		
CLO 3	3												1		
CLO 4	3														
CLO 5	1														
CLO 6					3										
CLO 7					3										
CLO 8					1										
CLO 9					3								2		
CLO 10					2								1		
CLO 11					2										
CLO 12					3										
CLO 13					2										
CLO 14					3				1				2		
CLO 15									2						
CLO 16									1						
CLO 17					1				2				2		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO5, PO 9	SEE Exams	PO 1, PO 5,PO 9	Assignments	PO 1, PO 5	Seminars	PO 1, PO 5
Laboratory Practices	PO 5	Student Viva	-	Mini Project	PO 9	Certification	-
Term Paper	PO 5						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

Unit-I	FUNDAMENTALS OF DIGITAL TECHNIQUES
Review of number systems: Decimal, binary, octal and hexa decimal, base conversion methods, complements of numbers; binary codes: Binary coded decimal, excess-3, gray codes, error detecting and error correcting codes.	
Unit-II	**BOOLEAN ALGEBRA AND THEOREMS**
Boolean algebra: Postulates and theorems; Logic gates and truth tables, representation of switching functions, sum of products and product of sums forms, karnaugh map representation, minimization using karnaugh map Quine - McClusky method of minimization.	
Unit-III	**DESIGN OF COMBINATIONALCIRCUITS**
Design of combinational circuits using conventional AND, OR, NOT, NAND, NOR and EX-OR gates. Adders and subtractors: Half adder, full adder, half subtractor, full subtractor. Parallel adder, serial adder, carry look ahead adder, binary coded decimal adder, 1"s complement subtractor, 2„s complement subtractor.	
Unit-IV	**SEQUENTIAL CIRCUITS**
Flip Flops: SR flip flop, JK flip flop, D flip flop, T flip flop, excitation tables, race around condition, master slave flip flop; Counters: Design of synchronous and asynchronous counters; Shift registers: Modes of operation, bidirectional shift registers, ring counters, Johnson counters.	
Unit-V	**CAPABILITIES AND MINIMIZATION OF SEQUENTIAL MACHINES**
Synchronous sequential circuits: State table, state diagram, state assignment, state minimization; Sequential circuits example: Sequence detectors, binary counters; Mealy and Moore machines: Capabilities and limitations of finite state machine, state equivalence and machine minimization of completely specified or incompletely specified machines, partition method, Merger table and graph method.	
Text Books:	
1. M. Morris Mano, Michael D. Ciletti, " Digital Design", Pearson Education, 3rd Edition, 2008. 2. Zvi. Kohavi, "Switching and Finite Automata Theory", Tata McGraw Hill, 3rd Edition, 2004. 3. John M. Yarbrough, "Digital logic applications and design", Thomson publications, 2nd Edition, 2006.	
Reference Books:	
1. Roth, "Fundamentals of Logic Design", Cengage learning, 5th Edition, 2004. 2. A. Anand Kumar,"Switching Theory and Logic Design", Prentice Hall of India, 1st Edition, 2014.	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Number systems, base conversion methods.	CLO 1	T1:1.5-1.7 R1:1.6-1.8
6-8	Complements of numbers, codes-binary codes, BCD code and its properties.	CLO 2	T1:1.7 R1:1.9
9-11	Unit distance code, alphanumeric codes, and error detecting and correcting codes	CLO 3	T1:1.7 R1:2.0
12-15	Basic theorems and its properties, switching functions, canonical and standard form.	CLO 4	T1:2.1-2.6 R1:2.3-2.5
16-18	Algebraic simplification of digital logic gates, properties of XOR gates.	CLO 5	T1:2.8 R1:2.6
19-21	Universal gates, Multilevel NAND/NOR realizations.	CLO 6	T1:3.7-3.8 R1:3.2-3.3

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
22-24	Tabular method.	CLO 7	T1:3.9 R1:4.0
25-32	Combinational design, arithmetic circuits- adders, substractors.	CLO 8	T1:4.1-4.9 R1:4.2-4.6
33-35	Serial adder, 1's complement substractor, 2's complement substractor.	CLO 9	T1:5.1-5.2 R1:4.7-4.8
36-38	Combinational and sequential circuits, the binary cell, the fundamentals of sequential machine operation.	CLO 10	T1:5.3-5.5 R1:5.0-5.2
39-42	Flip-flop, D-Latch Flip-flop, "Clocked T" Flip-flop, "Clocked JK "flip-flop.	CLO 11	T1:5.3-5.5 R1:5.3-5.4
43-45	Design of a clocked flip-flop conversion from one type of flip-flop to another.	CLO 12	T1:5.3-5.5 R1:5.5-5.7
46-48	Registers and counters.	CLO 13	T1:6.1-6.5 R1:6.1-6.3
49-51	Introduction, State diagrams, Analysis of synchronous sequential circuit	CLO 14	T1:6.6-6.8 R1:6.4-6.6
52-54	Approaches to the design of synchronous sequential finite state machines, design aspects State reduction, design steps, realization using flip-flop.	CLO 15	T1:7.1-7.2 R1:7.0-7.2
55-58	Finite State machine – Capabilities and limitations, mealy and Moore models.	CLO 16	T1:7.3-7.4 R1:7.3-7.5
59-63	Minimization of completely specified and incompletely specified sequential machines, partition techniques and merger chart methods – concept of minimal cover table.	CLO 17	T1:7.5-7.6 R1:7.7-7.8

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed Actions	Relevance With POs	Relevance With PSOs
1	Gate level Minimization.	Seminars	PO 1,PO 5	PSO 1
2	Design of combinational circuits using universal gates.	Seminars / NPTEL	PO 5,PO 9	PSO 1
3	Verilog programming for combinational and sequential circuits.	Guest Lectures	PO 5,PO 9	PSO 1

Prepared by:
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