DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

VIII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC507	ELECTIVE	3	-	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: Nil	Practical Classes: Nil				Total Classes: 45		

OBJECTIVES:

The course should enable the students to:

I. Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors

II. Learn the architectural differences between DSP and General purpose processor.

III. Learn about interfacing of serial & parallel communication devices to the processor.

IV. Implement the DSP & FFT algorithms.

COURSE OUTCOMES (COs):

CO 1: Understand the basics of Digital Signal Processing and transforms.

CO 2: Able to distinguish between the architectural features of General purpose processors and DSP processors.

CO 3: Understand the architectures of TMS320C54xx devices and Acquire knowledge about various addressing modes of DSP TMS320C54XX.

CO 4: Discuss about various memory and parallel I/O interfaces.

CO 5: Design and implement basic DSP algorithms.

COURSE LEARNING OUTCOMES (CLOs):

1. Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.
2. Understand the inter-relationship between DFT and various transforms.
3. Understand the IEE-754 floating point and source of errors in DSP implementations.
4. Understand the fast computation of DFT and appreciate the FFT Processing.
5. Understand the concept of multiplier and multiplier Accumulator.
6. Design SMID ,VLIW architectures.
7. Understand the modified bus structures and memory access in PDSPs.
8. Understand the special addressing modes in PDSPs.
9. Understand the architecture of TMS320C54XX DSPs.
10. Understand the addressing modes and memory space of TMS320C54XX DSPs.
11. Understand the various interrupts and pipeline operation of TMS320C54XX processors.
12. Analyze the Program control, instruction set and programming.
13. Understand the concept of on-chip Peripherals.

14. Understand the significance of memory space organization.
15. Analyze external bus interfacing signals.
16. Explain about parallel I/O interface, programmed I/O.
17. Understand the significance of Interrupts and Direct Memory Access.
18. Understand the basic concepts of convolution and correlation.
19. Compare the characteristics of IIR and FIR filters.
20. Analyze the concepts of interpolation and decimation filters.

UNIT -I	INTRODUCTION TO DIGITAL SIGNAL PROCESSING	Classes: 08

Introduction: Digital signal-processing system, discrete Fourier Transform (DFT) and fast Fourier transform (FFT), differences between DSP and other micro processor architectures; Number formats: Fixed point, floating point and block floating point formats, IEEE-754 floating point, dynamic range and precision, relation between data word size and instruction word size; Sources of error in DSP implementations: A/D conversion errors, DSP computational errors, D/A conversion errors, Q-notation.

UNIT – II	ARCHITECTURE OF PROGRAMMABLE DSPs	Classes: 10

Multiplier and multiplier accumulator, modified bus structures and memory access in PDSPs, multiple access memory, multiport memory, SIMD, VLIW architectures, pipelining, special addressing modes in PDSPs, on-chip peripherals.

UNIT – III	OVERVIEW OF TMS320C54XX PROCESSOR	Classes: 08

Architecture of TMS320C54XX DSPs, addressing modes, memory space of TMS320C54XX processors. Program control, instruction set and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation.

UNIT - IV	INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs	Classes: 10

Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA).

UNIT -V	IMPLEMENTATIONS OF BASIC DSP ALGORITHMS	Classes: 09

The Q-notation, convolution, correlation, FIR filters, IIR filters, interpolation filters, decimation filters, an FFT algorithm for DFT filters computation of the signal spectrum.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing Thomson Publications, 1st Edition, 2004.
2. Lapsley et al., DSP Processor Fundamentals, Architectures & Features‖, S. Chand & Co, 1 st Edition, 2000.
3. B. Ventakaramani, M. Bhaskar, Digital Signal Processors Architecture Programming and Applications‖, Tata McGraw-Hill, 1st Edition, 2006.

REFERENCES:

1. Jonatham Stein, Digital Signal Processing‖, John Wiley, 1st Edition, 2000.
2. Sen M. Kuo&WoonSergGan, Digital Signal Processors Architectures, Implementation and Application‖, Pearson

Practice Hall, 1st Edition, 2013.
3. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, A Practical Approach to Digital Signal Processing‖, New Age International, 1 st Edition, 2006.
4. Ifeachor E. C., Jervis B. W, Digital Signal Processing: A practical approach‖, Pearson Education, PHI/, 2nd Edition, 2002.
5. Peter Pirsch ,Architectures for Digital Signal Processing‖, John Weily, 1 st Edition, 2007.