INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**ELECTRONIC DEVICES AND CIRCUITS**				
Course Code	AEC001				
Programme	B.Tech				
Semester	III	ECE | EEE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Mr. V R Seshagiri Rao, Professor				
Course Faculty	Dr. P Ashok Babu, Professor Mr. B Naresh, Assistant Professor Mrs. G Mary Swarnalatha, Assistant Professor				

I. COURSE OVERVIEW:

This course provides the basic knowledge over the construction and functionality of the basic electronic devices such as diodes and transistors. It also provides the information about the uncontrollable and controllable electronic switches and the flow of current through these switches in different biasing conditions. This course is intended to describe the different configurations and modes of controllable switches and how these electronic devices can be configured to work as rectifiers, clippers, clampers, oscillators and amplifiers.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AHS006	I	Engineering Physics	4

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Electronic Devices and Circuits	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineeringfundamentals, and an engineering specialization to the solution of complex engineering problems.	2	Quiz
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complexengineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignments
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignments
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and researchmethods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Seminars

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Seminars and Assignments
PSO 2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Quiz and Assignments
PSO 3	**Successful career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Acquire knowledge of electrical characteristics of ideal and practical diodes under forward and reverse bias to analyze and design diode application circuits such as rectifiers and voltage regulators.
II	Utilize operational principles of bipolar junction transistors and field effect transistors to derive appropriate small-signal models and use them for the analysis of basic amplifier circuits.

The course should enable the students to:	
III	Perform DC analysis (algebraically and graphically using current voltage curves with super imposed load line) and design of CB, CE and CC transistor circuits.
IV	Compare and contrast different biasing and compensation techniques and functioning as amplifier.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC001.01	CLO 1	Understand and analyze diodes operation and their characteristics in order to design basic form circuits.	PO 1	3
AEC001.02	CLO 2	Explain the operation of Zener diode and its usage in voltage regulating application.	PO 1	2
AEC001.03	CLO 3	Explain the operational characteristics of various special purpose diodes such as zener diode, Tunnel diode, varactor diode and photo diode.	PO 1	2
AEC001.04	CLO 4	Understand the principle of operation and characteristics of silicon controlled rectifier and its application in power supply protection circuit.	PO 1 PO 4	2
AEC001.05	CLO 5	Explain half wave rectifier without and with different filters for the given specifications.	PO 1 PO 2	3
AEC001.06	CLO 6	Design full wave rectifier without filter and different filters for the given specifications.	PO 3	3
AEC001.07	CLO 7	Design and selection of appropriate filter to meet the requirements of voltage regulation and ripple factor	PO 3	3
AEC001.08	CLO 8	Write Use of diodes in typical circuits: rectifiers, regulated power supplies, limiting circuits.	PO 1	2
AEC001.09	CLO 9	Understand the different parameters of transistors such as depletion width and channel width for understanding the functioning and design of this component.	PO 1 PO 2	2
AEC001.10	CLO 10	Estimate the performance of BJT and UJT on the basis of their operation and working.	PO 1 PO 2	2
AEC001.11	CLO 11	Analyze various transistor configurations and asses merits and demerits for different applications.	PO 1	2
AEC001.12	CLO 12	Discuss the construction of MOSFET and steady the VI characteristics, as it is the prime component in VLSI technology.	PO 1	3
AEC001.13	CLO 13	Distinguish the constructional features and operation of FET and MOSFET and their applications	PO 1	2
AEC001.14	CLO 14	Develop the capability to analyze and design simple circuits containing non-linear elements such as transistors using	PO 3	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
		the concepts of load lines, operating points and incremental analysis.		
AEC001.15	CLO 15	Identify the various transistor biasing circuits and its usage in applications like amplifiers.	PO 1	3
AEC001.16	CLO 16	Explain basic circuits like dc and biasing circuits, small-signal ac circuits with emphasis on single-stage amplifiers.	PO 1	2
AEC001.17	CLO 17	Explain the role of temperature variations on the performance of the BJT, FET and MOSFET inorder to take necessary measures in design for stabilization.	PO 3 PO 4	3
AEC001.18	CLO 18	Discuss and Design small signal amplifier circuits applying the various biasing techniques.	PO 3	3
AEC001.19	CLO 19	Apply small-signal models to transistors and determine the voltage gain and input and output impedances.	PO 2 PO 3	3
AEC001.20	CLO 20	Analyze the performance of FETs on the basis of their operation and working.	PO 3	3
AEC001.21	CLO 21	Apply the concept of electronic devices and circuits to understand and analyze real time applications.	PO 4	2
AEC001.22	CLO 22	Acquire the knowledge and develop capability to succeed national and international level competitive examinations.	PO 4	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CLOs	POs												PSOs		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3												3		
CLO 2	2												1	3	
CLO 3	2												2		
CLO 4	2			2										3	
CLO 5	3	3												3	
CLO 6			3											2	
CLO 7			3											2	
CLO 8	2												3		
CLO 9	2	2											1		

CLOs	POs												PSOs		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 10	2	2												3	
CLO 11	2												2		
CLO 12	3													2	
CLO 13	2													2	
CLO 14			2										2		
CLO 15	3												3		
CLO 16	2												2		
CLO 17			3	3										2	
CLO 18			3											1	
CLO 19		3	3											1	
CLO 20			3										2		
CLO 21				2									1		
CLO 22				2											

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4	SEE Exams	PO 1, PO 2 PO 3, PO 4	Assignments	PO 2 PO 3	Seminars	PO 4
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	-						

XII. ASSESSMENT METHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS :

UNIT – I : SEMICONDUCTOR DIODES
P-N Junction Diode: Qualitative Theory of P-N Junction, P-N Junction as a Diode, Diode Equation, Volt-Ampere Characteristics, Temperature dependence of VI characteristic, Ideal versus Practical – Resistance levels (Static and Dynamic), Transition and Diffusion Capacitances, Diode Equivalent Circuits, Load Line Analysis, Breakdown Mechanisms in Semiconductor Diodes, Zener Diode Characteristics, Zener diode as a voltage regulator.

UNIT – II : SPECIAL ELECTRONIC DEVICES AND RECTIFIERS
Special purpose electronic devices: Principles of operation and characteristics of Silicon controlled rectifier, tunnel diode, varavtor diode, Photo diode; Half wave Rectifier, Full wave Rectifier, general filter considerations, Harmonic components in a Rectifier Circuit, Inductor Filters, Capacitor Filters, L-Section Filters,multiplt of L-C section , RC filter, Comparison of Filters.
UNIT – III : TRANSISTORS
Bipolar Junction Transistor and UJT: Transistor Construction, BJT Operation, minority carrier distribution and current components, Configurations, Characteristics, BJT specifications; Appications; Amplifier, switch. Field effect transistors: Types of FET, FET construction, symbol, principle of operation, V-I characteristics, FET parameters, FET as voltage variable resistor, comparison of BJT and FET; MOSFET construction and operation; Uni Junction Transistor: Symbol, Principle of operation, UJT Characteristics and applications.
UNIT – IV : BIASING AND COMPENSATION TECHNIQUES
Biasing and Compensation techniques: Operating Point, The DC and AC Load lines, types of biasing circuits, Bias Stability, Stabilization Factors, Stabilization against variations in VBE and β, Bias Compensation techniques, Thermal Runaway, Thermal Stability, biasing the FET and MOSFET.
UNIT – V : BJT AND FET AMPLIFIERS
BJT small signal analysis, BJT hybrid model, determination of h-parameters from transistor characteristics, Transistor amplifier, analysis using h-parameters; FET small signal model, FET as common source amplifier, , FET as common drain amplifier, , FET as common gate amplifier, generalized FET amplifier.
Textbooks:
1. J. Millman, C.C.Halkias and Satyabrata Jit, "Millman's Electronic Devices and Circuits", 2nd Edition, 1998, Tata McGraw Hill Publications. 2. J. Millman and Christos C. Halkias, "Integrated Electronics", International Student Edition , 2008, Tata McGraw Hill Publications. 3. David A. Bell, "Electronic Devices and Circuits", 5th Edition, Oxford University Press.
Reference Books:
1. R.L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuits", 9th Edition, 2006, PEI/PHI. 2. B.P.Singh, Rekha Singh, "Electronic Devices and Circuits", 2nd Edition, 2013, Pearson Publisher. 3. K. Lal Kishore, "Electronic Devices and Circuits", 2nd Edition, 2005,BS Publisher. 4. Anil K. Maini and Varsha Agarwal, "Electronic Devices and Circuits", 1stEdition, 2009, Wiley India Pvt. Ltd. 5. S. Salivahanan, N. Suresh Kumar and A. Vallavaraj, "Electronic Devices and Circuits", 2nd Edition, 2011, Tata McGraw Hill Publications.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	CLOs	Reference
1-2	Understand thefunctioning of diode	CLO 1	T1: 5.1
3-4	Examine the P-N junction diode under different biasing conditions	CLO 8	T1: 5.2
5	Derive the current equation	CLO 1	T1: 5.3
6-7	Examine the P-N junctiondiode under temperature conditions	CLO 1	T1: 5.6-5.7
8	Understand diode ideal and practical conditions	CLO 1	T1: 5.6 – 5.7

Lecture No.	Topics to be covered	CLOs	Reference
9	Understand diode load line	CLO 1	R5: 1.7
10-11	Solve the diode capacitance equations	CLO 1	T1: 5.8 -5.10
12	Understand breakdown mechanism	CLO 1	T1: 5.12 R5: 1.15
13	Model Zener diode as voltage regulator	CLO 2	T1: 6.15
14	Understand the operation Of tunnel diode.	CLO 3	T1:5.13-5.14 R5: 8.2
15	Understand the operationof SCR	CLO 4	R5: 8.5-8.6
16	Understand semiconductorPhoto diode.	CLO 3	R5: 8.5-8.6
17	Understand and analyzeP-N diode as rectifier	CLO 5	T1: 6.1-6.2
18-20	Understand and analyzeP-N diode as half wave rectifier.	CLO 5	T1: 6.1-6.2
21-23	Understand and analyzeP-N diode as full wave rectifier	CLO 6	T1: 6.3
24	Understand and analyze filters	CLO 6	T1: 6.7-6.8 T1: 6.10-6.13
25	Understand and analyze L section filters	CLO 7	T1: 6.10-6.13
26	Understand and analyze Pi section filters	CLO 6	T1: 6.10-6.13
27	Understand and analyze RC filters	CLO 7	T1: 6.7-6.8
28	Understand the constructionof bipolar transistor	CLO 9	T1: 7.1, 7.4
29	Understand the bipolar transistor	CLO 10	T1: 7.1
30	Understand the current componentsof bipolar transistor	CLO 9	T1: 7.2-7.3
31	Analyze CB characteristics	CLO 11	T1:7.7
32	Examine CE characteristics	CLO 11	T1: 7.8-7.10
33	Examine CC characteristics	CLO 11	T1: 7.12
34	Examine the BJT, BJT Applications	CLO 10	T1: 7.12
35	Understand the operationof FET transistor	CLO 13	R5:7.1-7.3
36	Understand FET construction	CLO 13	R5:7.4
37	Understand FET application	CLO 13	R5:7.7
38-39	Understand MOSFET operation	CLO 12	R5:7.9-7.16
40-41	Understand the operationof UJT.	CLO 10	T1: 12.12
42-43	Understand the Transistor biasing	CLO 16	T1: 8.1
44	Analyze load lines	CLO 14	R5: 4.2

Lecture No.	Topics to be covered	CLOs	Reference
45	Understand fixedbias	CLO 15	T1: 8.4
46	Understand emitter feedback circuit	CLO 15	T1:8.5
47-48	Analyze and design proper Voltage divide bias	CLO 15	T1:8.6
49-50	Understand bias stability	CLO 14	T1: 8.2 R5: 4.4
51	Understand compensation technique.	CLO 15	T1: 8.9
52	Examine thermal stability	CLO 17	T1: 8.12-8.13
53-54	Distinguish Hybrid model of BJT	CLO 16	T1: 10.6
55-56	Understand the operationof FET	CLO 20	T1: 12.1
57	Understand FET CD amplifier	CLO 20	T1: 12.2
58	Model the FET circuits	CLO 21	T1: 12.11
59	Understand application of FET	CLO 20	T1: 12.12
60	Understand comparison of transistors	CLO 21	T1: 12.12

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs	Relevance With PSOs
1	Design of AC to DC Converters	Seminars / NPTEL	PO 1, PO 2, PO 3	PSO 1
2	Design of amplifiers circuits	Seminars / Guest Lectures / NPTEL	PO 2,PO 3, PO 5	PSO 1
3	Design of electronic circuits on PCB boards.	Laboratory Practices	PO 1, PO 3,PO12	PSO 1

Prepared by:
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