INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE DESCRIPTOR

Course Title	**MICROPROCESSORS AND MICROCONTROLLERS**				
Course Code	AECB24				
Programme	B.Tech				
Semester	FIVE				
Course Type	CORE				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	2	1	3	-	-
Course Faculty	Ms. B Lakshmi Prasanna, Assistant Professor				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of microprocessors and microcontroller and their applications in detail. Subsequently the course covers important concepts like Semiconductor memory devices and systems, microcomputer architecture, assembly language programming, I/O programming, I/O interface design, I/O peripheral devices, data communication to write an assembly language programming for interfacing various I/O modules and make them to communicate.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AECB03	III	Digital Electronics

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microprocessors and Microcontrollers	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. **There could be a maximum of two sub divisions in a question.** The expected percentage of cognitive level of the questions is broadly based on the criteria given in Table: 1

Table 1: The expected percentage of cognitive level of questions in SEE

Percentage of Cognitive Level	Blooms Taxonomy Level
0%	Remember
60%	Understand
30%	Apply
10%	Analyze
0%	Evaluate
0%	Create

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 2), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (Table 3).

Table 2: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type

questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz –Online Examination:

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT):

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc. The AAT chosen for this course is given in table 3.

Table 3: Assessment pattern for AAT

5 Minutes Video	Assignment	Tech-talk	Seminar	Open Ended Experiment
20%	30%	30%	10%	10%

VI. COURSE OBJECTIVES:

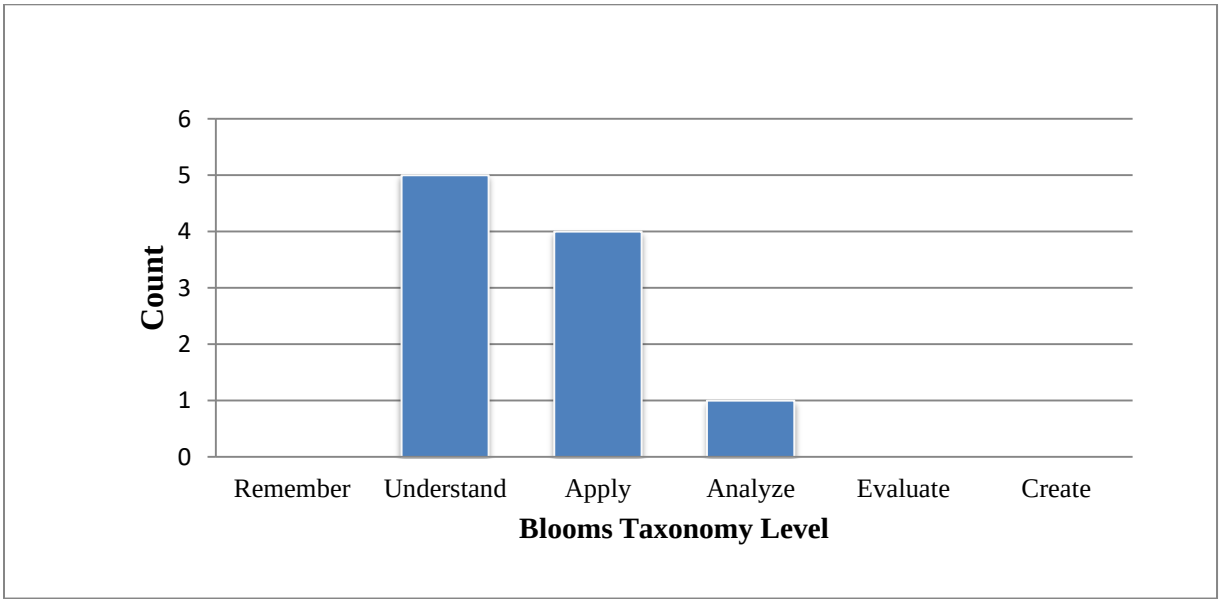
The students will try to learn:	
I	The architecture and operation of microprocessors and microcontrollers.
II	The programming and interfacing of Intel microprocessors, microcontrollers to design processor and controller based circuits.
III	The applications of microprocessors and microcontrollers in the field of Communications, Electronic measurement, control systems, Consumer electronics industry and other real-time systems.

VII. COURSE OUTCOMES:

After successful completion of the course, Students will be able to:		
CO No	**Course Outcomes**	**Knowledge Level (Bloom's Taxonomy)**
CO 1	**Outline** the internal architecture of 8085, 8086 and 8051 microcomputers to study their functionality.	Understand
CO 2	**Illustrate** the organization of registers and memory in 8086 for programming and memory allocation within processor.	Understand
CO 3	**Explain** various addressing modes and instruction set of target microprocessor and microcontroller useful for writing assembly language programs.	Understand
CO 4	**Distinguish** between minimum mode and maximum mode operation of 8086 microprocessor with timing diagrams.	Analyze

CO 5	**Interpret** the functionality of various types of interrupts and their structure for controlling the processor or controller and program execution flow.	Understand
CO 6	**Demonstrate** the internal architecture and various modes of operation of the devices used for interfacing memory and I/O devices with microprocessor.	Understand
CO 7	**Choose** an appropriate data transfer scheme and hardware to perform serial data transfer among the devices.	Apply
CO 8	**Make use of** 8051 microcontroller to perform Time/Counter operations in various applications.	Apply
CO 9	**Select** the suitable registers of 8051 microcontroller and program it to perform data conversion, interfacing with memory and I/O devices.	Apply
CO 10	**Build** necessary hardware and software interface using microcomputer based systems to provide solution for real world problems.	Apply

COURSE KNOWLEDGE COMPETENCY LEVELS



VIII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	CIE/SEE/AAT
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	AAT
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	AAT

Program Outcomes		Proficiency assessed by
PO 5	**Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern Engineering and IT tools including prediction and modeling to complex Engineering activities with an understanding of the limitations.	AAT

IX. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Proficiency assessed by
PSO 3	Gain the hands-on competency skills in PLC automation, process controllers, HMI and other computing tools necessary for entry level position to meet the requirements of the employer.	AAT

X. MAPPING OF EACH CO WITH PO(s), PSO(s):

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	√														
CO 2	√														
CO 3	√														
CO 4	√														
CO 5	√														
CO 6	√	√	√												√
CO 7	√	√	√		√										√
CO 8	√	√	√		√										√
CO 9	√	√	√		√										√
CO 10	√	√	√		√										√

XI. JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING

Course Outcomes	POs / PSOs	Justification for mapping (Students will be able to)	No. of key competencies
CO 1	**PO 1**	Outline (Knowledge) the internal architecture of 8085, 8086, 8051 microcomputers and **Understand their functionality** and identify the differences between processors by applying **principles of mathematics and science.**	2
CO 2	**PO 1**	Illustrate (Understand) the organization of registers and memory in 8086 for programming (Apply) and memory allocation within processor for **solving (complex)**	3

		engineering problems by **applying engineering fundamentals, engineering specialization**.	
CO 3	**PO 1**	Explain (Understand) various addressing modes and instruction set of target microprocessor and microcontroller useful for writing assembly language programs by applying **mathematics, science** and **engineering fundamentals** .	3
CO 4	**PO 1**	Distinguish (Analyze) between minimum mode and maximum mode operation of 8086 microprocessor with timing diagrams by applying **engineering fundamentals and engineering specialization**.	2
CO 5	**PO 1**	Interpret (Understand) the functionality of various types of interrupts and their structure for controlling the processor or controller and program execution flow by applying **mathematics, engineering fundamentals and engineering specialization.**	3
CO 6	**PO 1**	Demonstrate (Understand) the internal architecture and various modes of operation of the devices used for interfacing memory and I/O devices with microprocessor by applying **mathematics, engineering fundamentals and engineering specialization**.	3
	PO 2	Interpret the internal architecture and Identify various modes of operation for **information and data collection** of the devices used by **reviewing research literature** for interfacing memory and I/O devices **for experimental design** to solve **complex engineering problems** with microprocessor **for the solution of development using principles of natural sciences and engineering sciences**.	5
	PO 3	Make use of the internal architecture (Understand) and various modes of operation of the devices **for identifying a problem** and make interfacing between memory and I/O devices with microprocessor **for experimental design** to **meet specific needs with environmental considerations, to manage the design process** and **evaluate outcomes.**	5
	PSO 3	Demonstrate (knowledge) the proficiency in performing memory and I/O interfacing with microprocessor using modern tool necessary for **entry level position to meet the requirements of the employer.**	1
CO 7	**PO 1**	Choose (Apply) an appropriate data transfer scheme and hardware to perform serial data transfer among the devices by applying **mathematics, engineering fundamentals and engineering specialization**. .	3
	PO 2	**Identify** an appropriate data transfer scheme **(data) collection** and hardware for **model translation** and **analyze an experimental design** to perform serial data transfer among the devices **with an interpretation of results**.	5
	PO 3	Design proper data transfer scheme **to manage the design process** with **appropriate considerations** and hardware **design system components** for **designing the solutions on complex engineering problems** to perform serial data transfer among the devices **by applying the knowledge of techniques**, **for real time design issues.**	6

	PO 5	Make use of software tools to analyze the data transfer schemes between the processor and I/O devices by application of **modern tools.**	1
	PSO 3	Demonstrate (knowledge) the proficiency in performing serial data transfer among the device using modern tool necessary for **entry level position to meet the requirements of the employer.**	1
CO 8	**PO 1**	Interpret (Understand) the internal building blocks and registers of 8051 microcontroller used to perform timer and counter operations by applying **knowledge of mathematics**, **engineering fundamentals, engineering specialization.**	2
	PO 2	Explain the internal building blocks and **identify** registers of 8051 microcontroller by **analyzing complex engineering problems** used to perform Timer/Counter operations for **sustained conclusions** by applying **mathematics, natural sciences and Engineering sciences**.	5
	PO 3	Extend the internal building blocks and registers of 8051 microcontroller **find the solution for complex engineering problems** and perform timer and counter operations by **designing system components properly** and to **meet specific needs** of **societal and environmental aspects**	6
	PO 5	Make use of software tools to analyze the timer and counter operations using microcomputer system by application of **modern tools.**	1
	PS0 3	Demonstrate (knowledge) the proficiency in performing serial data transfer among the device using modern tool necessary for **entry level position to meet the requirements of the employer.**	1
CO 9	**PO 1**	Interpret (Understand) the internal building blocks and registers of 8051 microcontroller used to perform data conversion, interfacing of memory and I/O devices by applying **knowledge of mathematics**, **engineering fundamentals, engineering specialization.**	3
	PO 2	Explain the internal building blocks and **identify** registers of 8051 microcontroller by **analyzing complex engineering problems** used to perform data conversion, interfacing of memory and I/O devices for **sustained conclusions** by applying **mathematics, natural sciences and Engineering sciences**.	6
	PO 3	Extend the internal building blocks and registers of 8051 microcontroller **find the solution for complex engineering problems** and perform data conversion, interfacing of memory and I/O devices by **designing system components properly** and to **meet specific needs** of **societal and environmental aspects**	6
	PO 5	Make use of software tools to analyse the data conversion, memory and I/O interfacing using microcomputer system by application of **modern tools.**	1
	PSO 3	Demonstrate (knowledge) the proficiency in performing data conversion, memory and I/O interfacing using modern tool necessary for **entry level position to meet the requirements of the employer.**	1

CO 10	**PO 1**	Build (Apply) necessary hardware and software interface using microcomputer based systems to provide solution for real world problems by applying **knowledge of mathematics**, **engineering fundamentals, engineering specialization.**.	3
	PO 2	**Identify problem** and Choose necessary hardware and software interface **(information and data collection)** and conduct **experimental design** with **model translation** to provide **solution development** for real world problems **by interpreting results**	6
	PO 3	Organize necessary hardware and software interface **based on user needs and importance of considerations** for **innovative solutions, of the problem including all aspects to manage design process** , in microcomputer based systems **by applying different techniques**, **to achieve required sustained development, with legal requirements governing engineering activities, including personnel, health, safety, and risk issues.**	6
	PO 5	Make use of software and hardware tools to analyze real world applications developed using microcomputer system by application of **modern tools.**	1
	PSO 3	Demonstrate (knowledge) the proficiency in analyzing the real world applications developed around microcomputer system using modern tool necessary for **entry level position to meet the requirements of the employer.**	1

XII. NUMBER OF KEY COMPETENCIES FOR CO – (PO,PSO) MAPPING:

Course Outcomes	Program Outcomes / Number of Vital Features												PSO/ No. of Vital Features		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
	3	10	10	11	1	5	3	3	12	5	12	12	2	2	2
CO 1	2														
CO 2	3														
CO 3	2														
CO 4	3														
CO 5	3														
CO 6	3	5	5												1
CO 7	3	5	6		1										1
CO 8	2	5	6		1										1
CO 9	3	6	6		1										1
CO 10	3	6	6		1										1

XIII. PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO,PSO) MAPPING:

Course Outcomes	Program Outcomes / Number of Vital Features												PSO / No. of Vital Features		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
	3	10	10	11	1	5	3	3	12	5	12	12	2	1	2
CO 1	66.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 2	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 3	66.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 4	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 5	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 6	100.0	50.0	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0
CO 7	100.0	50.0	60.0	0.0	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0
CO 8	66.0	50.0	60.0	0.0	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0
CO 9	100.0	60.0	60.0	0.0	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0
CO 10	100.0	60.0	60.0	0.0	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	5.0	0.0	50.0

XIV. COURSE ARTICULATION MATRIX (CO - PO / PSO MAPPING):

COs and POs and COs and PSOs on the scale of 0 to 3, **0** being **no correlation**, **1** being the **low correlation**, **2** being **medium correlation** and **3** being **high correlation**.

0 – **0** ≤ C ≤ 5%– No correlation;
1 – 5 < C ≤ 40%– Low / Slight;
2 – 40 % < C < 60%– Moderate.
3 – 60% ≤ C < 100%– Substantial / High

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 6	3	2	2	-	-	-	-	-	-	-	-	-	-	-	2
CO 7	3	2	3	-	3	-	-	-	-	-	-	-	-	-	2
CO 8	2	2	3	-	3	-	-	-	-	-	-	-	-	-	2

CO 9	3	3	3	-	3	-	-	-	-	-	-	-	-	-	2
CO 10	3	3	3	-	3	-	-	-	-	-	-	-	-	-	2
TOTAL	27	12	14		12										10
AVERAGE	**3.0**	**1.0**	**2.0**		**1.0**										**1.0**

XV. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1,PSO 3	SEE Exams	PO 1, PSO 3	Assignments	PO 1,PO 2 PSO 3	Seminars	PO 1,PO 2, PO 3, PSO 3
Laboratory Practices	PO 3,PO 5	Student Viva	-	Mini Project	-	Certificatior	-
Term Paper	-						

XVI. ASSESSMENT METHODOLOGIES – INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XVII. SYLLABUS

MODULE-I	**8086 MICROPROCESSORS**
Register organization of 8086, Architecture, signal description of 8086, physical memory organization, general bus operation, I/O addressing capability, special purpose activities, Minimum mode, maximum mode of 8086 system and timings, machine language instruction formats, addressing mode of 8086, instruction set of 8086, assembler directives and operators.	
MODULE-II	**PROGRAMMING WITH 8086 MICROPROCESSOR**
Machine level programs, programming with an assembler, Assembly language programs, introduction to stack, stack structure of 8086/8088, interrupts and interrupt service routines. Interrupt cycle of 8086, non-mask able interrupt and mask able interrupts, interrupt programming.	
MODULE-III	**INTERFACING WITH 8086/880**
Semiconductor memory interfacing, dynamic RAM interfacing, interfacing i/o ports, PIO 8255 modes of operation of 8255, interfacing to D/A and A/D converters, stepper motor interfacing, control of high power devices using 8255. Programmable interrupt controller 8259A, the keyboard /display controller8279, programmable communication interface 8251 USART, DMA Controller 8257.	
MODULE-IV	**8051 MICROCONTROLLER**
8051 Microcontroller – Internal architecture and pin configuration, 8051 addressing modes, instruction set, Bit addressable features. I/O Port structures, assembly language programming using data transfer, arithmetic, logical and branch instructions.	

MODULE-V	SYSTEM DESIGN USING MICROCONTROLLER
8051 Timers/Counters, Serial data communication and its programming, 8051 interrupts, Interrupt vector table, Interrupt programming. Real world interfacing of 8051 with external memory, expansion of I/O ports, LCD, ADC, DAC, stepper motor interfacing.	
TEXT BOOKS:	
1 Ray A.K, Bhurchandi K.M, "Advanced Microprocessor and Peripherals", TMH, 2nd Edition, 2012 2 Muhammad Ali Mazidi, J.G. Mazidi, R.D McKinlay," The 8051 Microcontroller and Embeddedsystems using Assembly and C", Pearson education, 2nd Edition, 2009. 3 Douglas V. Hall, "Microprocessors and Interfacing Programming and Hardware", TMGH, 2nd Edition, 1994.	
REFERENCE BOOKS:	
1 Kenneth J. Ayala, "The 8051 Microcontroller", Thomson Learning, 3rd edition, 2005. 2 Manish K. Patel, "The 8051 Microcontroller Based Embedded Systems", McGraw Hill, 1st Edition, 2014. 3 Ajay V Deshmukh, "Microcontrollers", TATA McGraw Hill publications, 2nd Edition, 2012.	

XVIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	CO	Reference
1	Introduction: An over view of 8085	CO 1	R1: 1.1
2	Register organization of 8086	CO 2	T1: 1.1 R1:3.6
3	Architecture	CO 1	T1: 1.2 R1:3.9
4	signal description of 8086	CO 1	T1: 1.3
5	physical memory organization	CO 1	T1: 1.4 R1:3.8
5	general bus operation	CO 1	T1: 1.5
6	I/O addressing capability	CO 2	T1: 1.6
6	special purpose activities	CO 2	T1: 1.7
7	Minimum mode of 8086 system and timings	CO 4	T1: 1.8
8	maximum mode of 8086 system and timings	CO 4	T1: 1.9
9	machine language instruction formats	CO 3	T1: 2.1
10	addressing mode of 8086	CO 3	T1: 2.2 R1:4.3
11-13	instruction set of 8086,	CO 3	T1: 2.3 R1:5.1
14	Assembler directives and operators	CO 3	T1: 2.4

Lecture No.	Topics to be covered	CO	Reference
15	Machine level programs	CO 3	T1: 3.1
16	programming with an assembler	CO 3	T1: 3.3 R1:4.4
17-19	Assembly language programs	CO 3	T1: 3.4 R1:5.3,5.4
20	introduction to stack	CO 1	T1: 4.1 R1:6.2
20	stack structure of 8086/8088	CO 1	T1: 4.2 R1:6.2
21	interrupts and interrupt service routines	CO 5	T1: 4.3 R1:7.2,7.4
22	Interrupt cycle of 8086	CO 5	T1: 4.4
23	non-mask able interrupt and mask able interrupts	CO 5	T1: 4.5, 4.6
24	interrupt programming	CO 5	T1: 4.7 R1:7.11
25	Semiconductor memory interfacing	CO 6	T1: 5.1 R1:6.2
26	dynamic RAM interfacing	CO 6	T1: 5.2
27	interfacing i/o ports	CO 6	T1: 5.3
28-29	PIO 8255 modes of operation of 8255	CO 6	T1: 5.4 R1:12.2
30-31	Interfacing to D/A and A/D converters	CO 6	T1: 5.6, 5.7
32	Stepper motor interfacing	CO 6	T1: 5.8
33	Control of high power devices using 8255.	CO 6	T1: 5.9
34-35	Programmable interrupt controller 8259A	CO 6	T1: 6.2 R1:11.9
36	the keyboard /display controller8279	CO 6	T1:6.3
37-38	programmable communication interface 8251 USART	CO 6	T1: 6.4 R1:12.2
39-40	DMA Controller 8257	CO 6	T1: 7.1
41	8051 Microcontroller – Internal architecture	CO 1	T1: 17.2 R2:2.1
42	pin configuration	CO 1	T1: 17.3 R2:11.1,11.2
43	8051 addressing modes	CO 3	T1: 17.7 R2:4.2
44-45	instruction set	CO 3	T1: 17.8 R2:5,6,7
46	Bit addressable features	CO 9	R2:6.1
46	I/O Port structures	CO 9	R2:13.1

Lecture No.	Topics to be covered	CO	Reference
47-48	Assembly language programming using data transfer, arithmetic, logical and branch instructions.	CO 3	R2:12
49-50	8051 Timers/Counters	CO 8	R2:14
51-52	Serial data communication and its programming	CO 5	R2:15
53	8051 interrupts	CO 5	R2:16.2
54	Interrupt vector table	CO 5	R2:16.3
54	Interrupt programming	CO 5	R2:16.4
55	Real world interfacing of 8051 with external memory	CO 10	R2:21.1
55	Expansion of I/O ports	CO 9	R2:13.1
56	LCD	CO 9	R2:18.3
56	ADC	CO 9	R2:19.1
57	DAC	CO 9	R2:19.2
58	Stepper motor interfacing.	CO 9	R2:20.3

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