COMPUTER ORGANIZATION

V Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC010	Core	3	1	-	4	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

COURSE OBJECTIVES:

The course should enable the students to:

1. Understand the basic structure and operation of a digital computer.
2. Understand the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
3. Interpret the different types of control and the concept of pipelining.
4. To study the different ways of communicating with I/O devices and standard I/O interfaces and RISC and CISC processors.
5. To study the hierarchical memory system including cache memories and virtual memory.

COURSE OUTCOMES(COs):

CO 1: Ability to understand the concepts of associated with the computer system design and data representation.
CO 2: Explore the concepts associated with the fixed point arithmetic operations and algorithms.
CO 3: Understand the concepts of Control design of a computer.
CO 4: Ability to learn the concepts associated with the memory organization.
CO 5: Explore the concepts of System Organization including types of interrupts and processors.

COURSE LEARNING OUTCOMES(CLOs):

1. Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer..
2. Understand the concepts associated with the computer organization.
3. Describe various data representations and explain how arithmetic and logical operations are performed by computers.
4. Understand instruction types, addressing modes and their formats in the assembly language programs.
5. Describe the implementation of fixed point and floating point addition, subtraction operations.
6. Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).
7. Describe the pipeline processing concept with multiple functional units.
8. Understand the concept of the modified booth’s algorithm
9. Understand the connections among the circuits and the functionalities in the hardwired control unit.
10. Describe the design of control unit with address sequencing and microprogramming Concepts.
11. Describe the concepts CPU control unit, Pipeline control, instruction pipeline.
12. Understand the functionality of super scalar processing and Nano programming.
13. Understand the concept of memory hierarchy and different typed of memory chips.
14. Describe the concepts of magnetic surface recording, optical memories
15. Understand the cache and virtual memory concept in memory organization.
16. Describe the hardware organization of associate memory and understand the read and write operations.
17. Understand the various bus control interfaces and system control interfaces.
18. Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).
19. Understand the functionally of RISC and CISC processors.
20. Describe the concepts of superscalar and vector processor.

UNIT-I	INTRODUCTION	Classes: 08
Introduction Computing and computers, evolution of computers, VLSI Era, System design, register level, processor level, CPU organization, data representation, fixed-point numbers, floating point numbers, instruction formats, instruction types, addressing modes.		
UNIT-II	**DATA PATH DESIGN**	**Classes: 09**
Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division, Combinational and Sequential ALUs, Carry look ahead adder, Robertson algorithm, booth's algorithm, non restoring division algorithm, Floating Point Arithmetic, Coprocessor, Pipeline Processing, Pipeline Design, Modified booth's Algorithm.		
UNIT-III	**CONTROL DESIGN**	**Classes: 09**
Hardwired control, micro programmed control, multiplier control unit, CPU control unit. Pipeline control, instruction pipelines, pipeline performance, superscalar processing, nano programming.		
UNIT-IV	**MEMORY ORGANIZATION**	**Classes: 10**
Random access memories, serial access memories, RAM interfaces, magnetic surface recording, optical memories, multilevel memories, cache & virtual memory, memory allocation, associative memory.		
UNIT-V	**SYSTEM ORGANIZATION**	**Classes: 09**
Communication methods, buses, bus control, bus interfacing, bus arbitration, IO and system control, IO interface circuits, handshaking, DMA and interrupts, vectored interrupts, PCI interrupts, pipeline interrupts, IOP organization, operation systems, multiprocessors, fault tolerance, RISC and CISC processors, superscalar and vector processor.		

Text Books:

1. John P. Hayes, _Computer architecture and Organization', Tata McGraw-Hill, 3rd Edition, 1998.
2. V Carl Hamacher, Zvonko G. Varanesic, Safat G. Zaky, ―Computer Organization‖, Tata McGraw-Hill Inc, 5th Edition, 1996

Reference Books:

1. Morris Mano, ―Computer System Architecture‖, Prentice-Hall of India, 2000.
2. Paraami, ―Computer Architecture‖, BEH R002, Oxford Press.

Web References:

1. https://www.tutorialspoint.com/computer_organization/index.asp
2. https://nptel.ac.in/courses/106103068/
3. http://faculty.etsu.edu/tarnoff/ntes2150.html

E-Text Books:

1. https://books.google.co.in/books/about/Computer_Organization_And_Architecture.html?id=ERaDDqxMCKkC
2. http://www.a-zshiksha.com/forum/viewtopic.php?f=133&t=61511