MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING

I Semester: M.Tech. (ES)										
Course Code		Category	Hours / Week C			Credits	Ma	Maximum Marks		
BESB02		Core	L	Т	Р	С	CIA	SEE	Total	
			3	-	-	3	30	70	100	
Contact Classes: 45		Tutorial Classes: Nil	Practical Classes: Nil				Total Classes: 45			
OBJECT The cours 1. Comp ember II. Ident III. Dever COURSE CO 1: An CO 2: Un CO 3: Stu CO 4: Ide CO 5: Un COURSE 1. Unde mode 2. Study Bit-B 3. Discu 4. Exam Excep 5. Discu 6. Unde Intern 7. Descu 8. Study 9. Unde 10. Descu 11. Study 12. Unde 13. Study 14. Unde addre 15. Descu perip	IVES: se should enable pare and select A dded application ify and characte lop small applic COUTCOMES alyze the charact derstand the varies derstand the varies derstand the trive CLEARNING CLEARNING CLEARNING and Operations and Operations iss the Unaligne ine the various ptions iss the Supervise restand the Basic cupt Latency. ribe the LPC 1777 the features of restand the conce ribe the Program the features of restand the Introop the features of restand the Introop the VLIW arch restand the Introop the VLIW arch restand the Introop the the Code Col- herals, Processon	le the students to: ARM processor core based S ns. rize architecture of Program rations by utilizing the ARM (COS): teristics of ARM Cortex-M3 ious Exceptions and Interru of LPC 17xx microcontrolle the characteristics Program IS320C6000 series DSP Pro- OUTCOMES (CLOS): RM Cortex-M3 processor: A nd Interrupts, Reset Sequence Set, Unified Assembler Land d and Exclusive Transfers. Exceptions, Types, Priority or and Pendable Service Call c Configuration, SYSTICK 7 xx microcontroller- Internal ADC, UART and other seri- tepts of PWM, RTC, WDT mable DSP (P-DSP) Proce architectural structure of P- duction to TI DSP processon intecture and TMS320C6000 duction to Instruction level a netic, logical operations. omposer Studio for applicat r benchmarking.	SoC with mable I f process pts in Co ers based mmable ocessor a Applicati- ce. nguage, Vector II, Neste Timer, In I memory ial interf ssors: Ha DSP- M r family. 0 series, architect ion deve	n several DSP Pro- sor core sor. ortex-M on Cort DSP Pro- rchitectu ions, Pro- Memory , Bus In Tables, d Vector nterrupt y, GPIO aces. arvard a fAC unit architecture ure of C	l feature cessors and DSI 3 proces ex-M3 p ocessors ares. ogrammi 7 Maps, terfaces. Interrup red Inter Sequend s, Timer rchitectu , Barrel ture stud 6000 fai t for dig	s/peripherals P processor t sor. processor. ing model – 1 Memory Acc t Inputs and rupt Control ces, Exits, Ta rs. ure, Multi po shifters. dy, data path mily, Assem ital signal pro-	based based platfi Registers, cess Attrib Pending b ler. ail Chainin rt memory s, cross pa bly Instruct ocessing, c	on requir orm Operation utes, Perr ehavior, I g, g, ths. tions mer on chip	ements of n missions, Fault mory	
ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and										
Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.										
Unit -II	EXCEPTION	S AND INTERRUPTS						Cla	isses: 09	
Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.										

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Unit -III	LPC 17XX MICROCONTROLLER							
LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC.								
UART and	l other serial interfaces, PWM, RTC, WDT.							
Unit -IV	PROGRAMMABLE DSP (P-DSP) PROCESSORS	Classes: 09						
Programm	able DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure	of P-DSP-						
MAC unit, Barrel shifters, Introduction to TI DSP processor family.								
Unit -V	VLIW ARCHITECTURE	Classes: 09						
VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking								
Text Books:								
1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 3rd Edition, 2014.								
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2 nd Edition, 2011.								
Referenc	e Books:							
1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing".								
Morgan Kaufman Publications,								
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education.								
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley Publications.								
Web References:								
1. http://www.arm.com								
2. http://nptel.ac.in/video.php?subjectId=112101099								
5. https://developer.arm.com > docs								
E-Text Books:								
1. https://university.ti.com								
2. http://www.everythingvtu.wordpress.com								

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