INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION

Course Name	:	**FPGA ARCHITECURE AND APPLICATION**			
Course Code	:	**BES005**			
Regulation	:	**R16**			
Course Structure	:	Lectures	Tutorials	Practicals	Credits
		3	-	-	3
Branch	:	**Electronics and Communication Engineering**			
Academic Year	:	**2017– 2018**			
Course Faculty	:	**Dr. V. Vijay, Professor, E.C.E**			

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of FPGA architectures and its requirements. Subsequently the course covers architectural design of CPLD architectures. As we progress with the course students will be familiarized with the programming models as well as protocols which govern the sensor network and its applications in real world.

II. PREREQUISITES:

Level	Credits	Periods/Week	Prerequisites
PG	3	3	Embedded WSN

III. MARKS DISTRIBUTION:

Sessional Marks	University End Exam Marks	Total Marks
Midterm Test There shall be two midterm examinations. Each midterm examination consists of essay paper and assignment. The essay paper is for 25 marks of 60 minutes duration and shall contain 4 questions. The student has to answer 2 questions, each carrying 5 marks. First midterm examination shall be conducted for the first two and half units of syllabus and second midterm examination shall be conducted for the remaining portion. Five marks are marked for assignments. There shall be two assignments in every theory course. Assignments are usually issued at the time of commencement of the semester. These are of problem solving in nature with critical thinking. Marks shall be awarded considering the average of two midterm tests in each course.	70	100

IV. EVALUATION SCHEME:

S.NO.	Component	Duration	Marks
1	I Mid Examination	120 minutes	25
2	I Assignment	-	05
3	II Mid Examination	120 minutes	25
4	II Assignment	-	05
5	External Examination	180 minutes	70

V. COURSE OBJECTIVES:

At the end of the course, the students will be able to:

I. Understand the architecture of various FPGA and CPLD.

II. Design and implementation ASIC targeting to FPGA/CPLD.

III. Understand different types of programming technologies and logic devices.

VI. COURSE OUTCOMES:

After completing this course the student must demonstrate the knowledge and ability to:

1. Understand the concept of programming logic devices and its applications.
2. Acquire knowledge of various programming methods in FPGA.
3. Design antifuse FPGA based architectures.
4. Familiarize with SRAM based FPGA architectures.
5. Design CPLD and FPGA architectures for real time applications.

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program outcomes		Level	Proficiency assessed by
PO1	**Engineering Knowledge** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems	H	Assignments, Tutorials
PO2	**Problem Analysis** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	S	Assignments

PO3	**Design/Development of Solutions** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	H	Mini projects
PO4	**Conduct Investigations of Complex Problems** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions	H	Projects
PO5	**Modern Tool Usage** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	S	Projects
PO6	**The Engineer And Society** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice	N	--
PO7	**Environment and sustainability** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development	S	Assignments
PO8	**Ethics** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice	S	Oral Discussions
PO9	**Individual and Team Work** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings	N	--
PO10	**Communication** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions	S	PresentationS
PO11	**Project management and finance** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments	S	Seminars Discussions
PO12	**Life-long learning**	H	Development

	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change		of Prototype, Mini Projects

N=None S=Supportive H=Highly Related

VIII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	H	Lectures and Assignments
PSO2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	S	Tutorials
PSO3	**Successful career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	S	Seminars and Projects

IX. SYLLABUS:

UNIT – I

INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES:- Introduction, simple programmable logic devices: Read only memories; Programmable logic arrays, Programmable array logic, Programmable logic devices/Generic array logic; Complex programmable logic devices: Architecture of Xilinx cool runner XCR3064XL CPLD, CPLD implementation of a parallel adder with accumulation.

UNIT – II

FIELD PROGRAMMABLE GATE ARRAYS:- Organization of FPGAs, FPGA programming technologies and Programmable logic block architectures, programmable interconnects, programmable I/O blocks in FPGAs, dedicated specialized components of FPGAs and applications of FPGAs.

UNIT – III

SRAM PROGRAMMABLE FPGAS:- Introduction, programming technology, device architecture, the Xilinx XC2000, XC3000 and XC4000 architectures.

UNIT – IV

ANTIFUSE PROGRAMMED FPGAS:- Introduction, programming technology, device architecture, the Actel ACT1, ACT2 and ACT3 architectures.

UNIT – V

DESIGN APPLICATIONS:- General design issues, counter examples, fast video controller and position tracker for a robot manipulator, fast DMA controller, designing counters with ACT devices, designing adders and accumulators with the ACT architecture.

Text Books:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition, 1stEditon, 1994.
2. Charles H. Roth Jr, Lizy Kurian John, "Digital Systems Design", Cengage Learning, 2ndEdition, 2012.

References:

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India, 1stEdition, 2008.
2. Pak K. Chan/Samiha Mourad, "Digital Design Using Field Programmable Gate Arrays", Pearson Low

   Price Edition, 1999.
3. Ian Grout, "Digital Systems Design with FPGAs and CPLDs, Elsevier, Newnes, 1st Edition, 2008.
4. Wayne Wolf, "FPGA based System Design", Prentice Hall, Modern Semiconductor Design Series, 2004.

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following course learning outcomes (CLO):

Lecture No.	CLO	UNIT	Learning Objective	Topics to be covered	Reference
			I Spell		
1-2	1	I	**Understanding** the basic concept of logic devices	Introduction, simple programmable logic devices	Textbook 1
3-4	2		**Familiarization** to architecture of read only memories and logic arrays	Read only memories; Programmable logic arrays	Textbook 1
5-6	3		**Design** the programmable logic devices	Programmable array logic, Programmable logic devices/Generic array logic	Textbook 1
7-8	4		**Study** of complex programmable logic device and its features	Complex programmable logic devices: Architecture of Xilinx cool runner XCR3064XL CPLD	Textbook 1
9	5		**Design** the parallel adder using CPLD architectures	CPLD implementation of a parallel adder with accumulation.	Textbook 1
10-11	6	II	**Examine** the various function blocks in FPGA	Organization of FPGAs	Textbook 1
12-13	7		**List** the programming technology and its features	FPGA programming technologies	Textbook 1

14	8		**Discuss** the various principles involved in the design of programmable logic block architectures	Programmable logic block architectures	Textbook 1
15-16	9		**Understand** the needs of programmable interconnects	programmable interconnects	Textbook 1
17-18	10		**Describe** the functions of programmable I/O blocks in FPGA	programmable I/O blocks in FPGAs	Textbook 1
19	11	III	**Describe** the programming of SRAM FPGA	Introduction	Textbook 1
20-21	12		**Define** the programming technology and Analyze device architecture	programming technology and device architecture	Textbook 1
22-23	13		**Study** the features of Xilinx XC2000 architecture	Xilinx XC2000 architecture	Textbook 1
24-25	14		**Understand** the concepts of Xilinx XC3000 architecture	Xilinx XC3000 architecture	Textbook 1
26-27	15		**Study** the features of Xilinx XC4000 architecture	Xilinx XC4000 architecture	Textbook 1
Lecture No.	**CLO**	**UNIT**	**Learning Objective**	**Topics to be covered**	**Reference**
II Spell					
28	16	IV	**Describe** the programming of antifuse FPGA	Introduction	Textbook 1
29-30	17		**Define** the programming technology and Analyze device architecture	Programming technology	Textbook 1
31-32	18		**Study** the features of ACTEL act1 architecture	ACTEL ACT 1 architecture	Textbook 1
33-34	19		**Understand** the concepts of ACTEL ACT2 architecture	ACTEL ACT 2 architecture	Textbook 1
35-36	20		**Study** the features of ACTEL act3 architecture	ACTEL ACT 3 architecture	Textbook 1
37-38	21	V	**Study** the design issues and design of counter	General design issues, counter examples	Textbook 1
39-41	22		**Implement** robot for position tracking and analyze the features of DMA controller	fast video controller and position tracker for a robot manipulator, Fast DMA controller,	Textbook 1
42-43	23		**Analyze** the performance of counters using ACT devices	Designing counters with ACT devices	Textbook 1
44-45	24		**Design** of data path units using ACT architecture	Designing adders and accumulators with the ACT architecture	Textbook 1

XI. MAPPING OF COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	H							S				H		S	S
2		S					S			S			H	S	
3				H				S			S		H	S	

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XII. MAPPING COURSE OUTCOMES LEADING TO ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	H		H					S			S	H		S	S
2	H				S		S				S		H	S	
3		S			S			S				H	H	S	
4	H			H			S	S		S	S			S	
5	H	S	H		S								H	S	

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HEAD OF THE DEPARTMENT,

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