INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION FORM

Course Name	:	**VLSI Design**			
Course Code	:	**A60432**			
Regulation	:	**R15**			
Course Structure	:	**Lectures**	**Tutorials**	**Practicals**	**Credits**
		4	**1**	**-**	**4**
Class	:	**III B. Tech II Semester**			
Branch	:	**Electronics and Communication Engineering**			
Academic Year	:	**2017– 2018**			
Course Coordinator	:	**Dr. V. R. Seshagiri Rao, Professor, ECE.**			
Course Faculty	:	**Dr. V. R. Seshagiri Rao, Professor, ECE** **Dr. V. Vijay, Professor, ECE** **Mr. D Khalandar Basha, Assistant Professor,ECE** **Ms. U. Dhanalakshmi, Assistant Professor,ECE**			

I. COURSE OVERVIEW

VLSI design course gives the knowledge about the fabrication of NMOS, PMOS, CMOS and their application in the present electronics world. The present course gives knowledge about different processes used for fabrication of an IC. The electrical properties of MOS transistor and analysis of CMOS, BiCMOS inverters is carried out. This course gives detail study on design rules, stick diagrams, logic gates, types of delays, fan-in, fan-out which effects the action of a MOS. It also gives information on data path subsystem and array subsystems, and several PLD's like PLA, PAL, CPLD and FPGA's. We also came to know about the CMOS testing principles both at system level and chip level.

II. PREREQUISITE(S)

Level	Credits	Periods/Week	Prerequisites
UG	4	4	Electronic Devices and circuits. Switching Theory and Logic Design

III. MARKS DISTRIBUTION

Sessional Marks	University End Exam Marks	Total Marks
Mid Semester Test There shall be 2 midterm examinations. Each midterm examination consists of subjective test and objective type tests. The subjective test is for 10 marks, with duration of 1 hour. Subjective test of each midterm exam shall contain 4 questions. The student has to answer any 2 questions, each carrying 5 marks. The objective test is for 10 marks, with duration of 20 minutes. It consists of 10	75	100

Sessional Marks	University End Exam Marks	Total Marks
multiple choice and 10 objective type questions. The student has to answer all the questions and each carries half mark. First midterm examination shall be conducted for the first 2½ units of syllabus and second midterm examination shall be conducted for the remaining 2½ units. Five marks are marked for assignments. There shall be two assignments in every theory course. Marks shall be awarded considering the average of two assignments in each course reason whatsoever, will get zero marks.		

IV. EVALUATION SCHEME:

S.NO	Component	Duration	Marks
	I Mid Examination	80 minutes	20
	I Assignment	-	05
	II Mid Examination	80 minutes	20
	II Assignment	-	05
	External Examination	3 hours	75

V. COURSE OBJECTIVES:

At the end of the course, the students will be able to:

I. Give exposure to different steps involved in fabrication of ICs using MOS/BiCMOS/CMOS transistors.

II. Explain electrical properties of MOS and BiCMOS devices to analyze the behaviour of inverters designed with various load.

III. Give exposure to the design rules to be followed to draw the layout of any logic circuits.

IV. Provide concept to different logic gates using CMOS inverter and analyze their characteristics.

V. Provide design concepts to design building blocks of data path of any system using gates.

VI. Understand basic PLDs and testing of CMOS circuits.

VI. COURSE OUTCOMES:

After completing this course the student must demonstrate the knowledge and ability to:

1. Discuss about the fabrication process of ICs by different Metal Oxide Semiconductor (MOS) technologies and explain the various electrical properties of MOS transistors.
2. Choose an appropriate inverter depending on specifications required for a circuit.
3. Design the stick diagrams and layout of any logic circuits and illustrate the different design rules for layout design.
4. Explain different switch logic and alternate gate circuits.
5. Design of various subsystems like shifters, adders, comparators, multipliers detectors and counters.

6. Design simple array of memories using MOS transistors and can understand design of large Memories.
7. Develop programmable logic gates using PLA, PAL design approaches.
8. Develop programmable logic gates using CPLD and FPGA.
9. Know the necessity of testing a chip and the design strategies for test.
10. Know the chip level and system level testing methodologies.

VII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program outcomes		Level	Proficiency assessed by
PO1	**Engineering Knowledge** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems	S	Assignments
PO2	**Problem Analysis** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	S	Assignments
PO3	**Design/Development of Solutions** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	H	Practice Sessions
PO4	**Conduct Investigations of Complex Problems** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions	S	Design Exercises
PO5	**Modern Tool Usage** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	H	Design Exercises Seminars, Paper Presentations
PO6	**The Engineer And Society** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice	N	--
PO7	**Environment and sustainability** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development	N	--
PO8	**Ethics** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice	N	--
PO9	**Individual and Team Work** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings	H	Projects

PO10	**Communication** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions	S	Document Preparation and Presentation
PO11	**Project management and finance** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments	H	Seminars Discussions
PO12	**Life-long learning** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change	S	Development of Prototype, Mini Projects

N-None S-Supportive H-Highly Related

VIII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		**Level**	**Proficiency assessed by**
PSO1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	H	Lectures and Assignments
PSO2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	S	Tutorials
PSO3	**Successful career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	S	Seminars and Projects

N-None S-Supportive H-Highly Related

IX. SYLLABUS:

UNIT – I

INTRODUCTION: Introduction to IC technology-MOS, PMOS, NMOS, CMOS and BiCMOS Technologies.

BASIC ELECTRICAL PROPERTIES: Basic electrical properties of MOS and BiCMOS circuits: Ids- Vds relationships, MOS transistor threshold voltage, gm, gds, figure of merit wo , pass transistor, NMOS inverter, Various pull-ups, CMOS inverter analysis and design, BiCMOS inverters.

UNIT – II

VLSI CIRCUIT DESIGN PROCESSES: VLSI design flow, MOS layers, Stick diagrams, Design Rules and Layout, 2 um CMOS design rules for wires, Contacts and Transistors, Layout diagrams for NMOS and CMOS inverters and gates, Scaling of MOS circuits .

UNIT – III
GATE LEVEL DESIGN: Logic gates and other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitances, Fan-in and fan-out, Choice of layers.

UNIT – IV
DATA PATH SUB SYSTEMS: Sub system design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One detectors, Counters.
ARRAY SUBSYSTEMS: SRAM, DRAM, ROM, Serial Access Memories, Content Addressable Memory

UNIT – V
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN: PLAs, FPGAs, CPLDs, Standard cells, Programmable Array Logic, Design Approach, Parameters influencing low power design.
CMOS TESTING: CMOS Testing, Need for testing, Test principles, Design strategies for test, Chip level test techniques, System-level test techniques, Layout design for improved testability.

Text Books:
1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2. VLSI DESIGN - K. Lal Kishore, V.S.V Prabhakar, I.K International, 2009.
3. CMOS VLSI Design- Neil H.E Weste, David Harris, AyanBanerjee, Pearson Education, 1999.

Reference Books:
1. CMOS logic circuit design- John P. Uyemura, Springer, 2007.
2. Modern VLSI Design – Wayne Wolf, Pearson Education, 3rd Edition, 1997.
3. Introduction to VLSI-Mead and convey, BS publications, 2010

X. COURSE PLAN:

At the end of the course, the students are able to achieve the following course learning outcomes (CLO):

Lecture No.	Course learning outcomes	Topics to be covered	Text Book/ Reference
1-2	Discuss and memorize the IC generations, importance of VLSI To know fabrication of PMOS.	Introduction to IC Technology – MOS, PMOS	T1-1.1,1.2, 1.3,1.4
3-4	Describe fabrication of NMOS.	NMOS technology	T1-1.7
5-7	Describe fabrication of CMOS.	CMOS technologies	T1-1.8
8-9	Describe fabrication of Bi CMOS.	Bi CMOS technologies	T1-1.10
10-11	Identify the threshold voltage concept and Basic Electrical Properties	Basic Electrical Properties of MOS and Bi-CMOS Circuits	T1-2.1
12-13	Depending on V_{GS} I_{ds}-V_{ds} relations are derived.	Ids-Vds relationships, MOS transistor threshold Voltage	T1-2.2
14	Illustrate about the pass transistor,w_o	gm, gds, figure of merit wo, Pass transistor	T1-2.4,2.5
15	Illustrate various pull up.	Various pull-ups,	T1-2.7,2.8
16-17	Identify why we are preferring CMOS technology.	CMOS Inverter analysis and design, Bi-CMOS Inverters	T1-2.10,2.12.3
18	Describe the design flow.	Design Flow, MOS Layers	T1-3.1

19-20	Discuss stick diagram representation and illustrate the concept of stick diagram representation.	Stick Diagrams, Design Rules and Layout	T1-3.2
21-22	Examine the concept of layout and study required rules.	2 um CMOS Design rules for wires, Contacts and Transistors	T1-3.3
23-24	Discuss the construction of study layout rules for different processes and to learn how to draw layouts.	Layout Diagrams for NMOS and CMOS Inverters and Gates	T1-3.3.1
25	Discuss and memorize the scaling and effects of scaling. Identify the limitations of scaling	Scaling of MOS circuits	T1-3.4
26-27	Analyse gate design by CMOS and nMOS logic.	Logic Gates and Other complex gates, Switch logic	T1-3.7
28-30	Illustrate gate design and distinguish between CMOS and nMOS logic.	Alternate gate circuits, Time Delays	T1-3.7,3.8
31-32	Discuss driving large Capacitive Loads, Wiring Capacitances	Driving large Capacitive Loads, Wiring Capacitances	T1-4.8
33	Describe about Fan-in and fan-out, Choice of layers	Fan-in and fan-out, Choice of layers	T1-4.7
34-36	Design Shifters, Adders	Subsystem Design, Shifters, Adders	T3-11.8
37-38	Design ALUs, Multipliers, Parity generators	ALUs, Multipliers, Parity generators	T3-11.9
39-41	Design Comparators, Zero/One Detectors, Counters	Comparators, Zero/One Detectors, Counters	T3-11.4
42-44	Design memories SRAM, DRAM, ROM	SRAM, DRAM, ROM	T3-12.2,12.3,12.4
45-48	Design of serial access memories, content addressable memory	Serial access memories, content addressable memory	T3-12.5
49-52	Design of PLAs, FPGAs, CPLDs	PLAs, FPGAs, CPLDs	T3-12.7
53	Mention advantages of Programmable Array Logic	Standard Cells, Programmable Array Logic	R4
54-55	Illustrate parameters influencing low power design	Design Approach, parameters influencing low	T3-13.3
56-57	Demonstrate the need for testing.	CMOS Testing, Need for testing, Test Principles	T3-15.1
58-60	To illustrate the different test techniques To acquaint with the chip level testing techniques.	Design Strategies for test, Chip level Test Techniques	T3-15.4
61-63	To Discuss with the system level testing techniques.	System-level Test Techniques, Layout Design for improved Testability	T3-15.5

XI. MAPPING COURSE OBJECTIVES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUCOMES:

Course Objectives	Program Outcomes												Program Specific Outcomes		
	PO 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
I.	S	H	H			S			S				H		
II.	H		S						H				S		
III.	S	H	S			H	S		S		S		S		
IV.	H		S						H					S	
V.	S	S	S		S						H	S			S
VI.		S			H							S			S

S-Supportive **H-Highly Related**

XII. MAPPING COURSE OUTCOMES LEADING TO ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1.	H		S		S						H	S	H		
2.			S								S	H	H		
3.	H		S		S				H		H		S		
4.	S		S		H							S	S		
5.	S				S						H	S	H		
6.	S		S		H									H	
7.	H				S				H		S	S		S	
8.	S		H		H				H					S	
9.	H		S		H						S				S
10.												S			S

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