INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

INFORMATION TECHNOLOGY

COURSE DESCRIPTOR

Course Title	**MICROPROCESSORS AND INTERFACING**				
Course Code	AECB55				
Programme	B.Tech				
Semester	FIVE				
Course Type	Open Elective - I				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Course Faculty	Ms. B Lakshmi Prasanna, Assistant Professor				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of microprocessors and microcontroller and their applications in detail. Subsequently the course covers important concepts like Semiconductor memory devices and systems, microcomputer architecture, assembly language programming, I/O programming, I/O interface design, I/O peripheral devices, data communication to write an assembly language programming for interfacing various I/O modules and make them to communicate, and also includes introduction to the advance processors including RISC based processors.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AECB05	III	Analog and Digital Electronics
B.Tech	ACSB07	IV	Computer Organization and Architecture

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microprocessors and Interfacing	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. **There could be a maximum of two sub divisions in a question.** The expected percentage of cognitive level of the questions is broadly based on the criteria given in Table: 1

Table 1: The expected percentage of cognitive level of questions in SEE

Percentage of Cognitive Level	Blooms Taxonomy Level
0%	Remember
60%	Understand
30%	Apply
10%	Analyze
0%	Evaluate
0%	Create

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 2), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (Table 3).

Table 2: Assessment pattern for CIA

Component	Theory			Total Marks
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type

questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz –Online Examination:

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT):

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc. The AAT chosen for this course is given in table 3.

Table 3: Assessment pattern for AAT

5 Minutes Video	Assignment	Tech-talk	Seminar	Open Ended Experiment
20%	30%	30%	10%	10%

VI. COURSE OBJECTIVES :

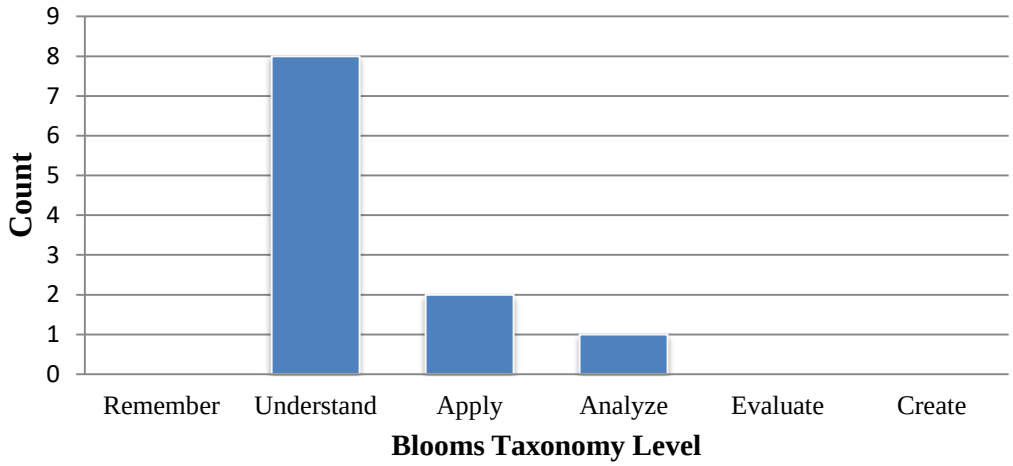
The students will try to learn:	
I	The architecture and operation of microprocessors and microcontrollers.
II	The programming and interfacing of Intel microprocessors, microcontrollers to design processor and controller based circuits.
III	The applications of microprocessors and microcontrollers in the field of Communications, Electronic measurement, control systems, Consumer electronics industry and other real-time systems.

VII. COURSE OUTCOMES :

After successful completion of the course, Students will be able to:		
CO No	**Course Outcomes**	**Knowledge Level (Bloom's Taxonomy)**
CO 1	**Outline** the internal architecture of 8085, 8086 and 8051 microcomputers to study the functionality.	Understand
CO 2	**Illustrate** the organization of registers and memory in 8086 for programming and memory allocation within processor.	Understand
CO 3	**Explain** various addressing modes and instruction set of target microprocessor and microcontroller useful for writing assembly language programs.	Understand
CO 4	**Distinguish** between minimum mode and maximum mode operation of 8086 microprocessor with timing diagrams.	Analyze

CO 5	**Interpret** the functionality of various types of interrupts and their structure for controlling the processor or controller and program execution flow.	Understand
CO 6	**Demonstrate** the internal architecture and various modes of operation of the devices used for interfacing memory and I/O devices with microprocessor.	Understand
CO 7	**Choose** an appropriate data transfer scheme and hardware to perform serial data transfer among the devices.	Apply
CO 8	**Outline** the salient features of 80286, 80386 and RISC processors in relation to basic 8086 microprocessor.	Understand
CO 9	**Illustrate** the paging operation and segmentation of advanced microprocessors for memory management.	Understand
CO 10	**Interpret** the internal building blocks and registers of 8051 microcontroller used to perform serial data transfer, timer operation, interfacing of memory and I/O devices.	Understand
CO 11	**Build** necessary hardware and software interface using microcomputer based systems to provide solution for real world problems.	Apply

COURSE KNOWLEDGE COMPETENCY LEVELS



VIII. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes		Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to solution of complex engineering problems.	CIE/SEE/AAT
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	AAT
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate	AAT

Program Outcomes		Proficiency assessed by
	consideration for the public health and safety, and the cultural, societal, and environmental considerations.	

IX. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Proficiency assessed by
PSO1	Design next-generation computer systems, networking devices, search engines, soft computing and intelligent systems, web browsers, and knowledge discovery tools.	AAT

X. MAPPING OF EACH CO WITH PO(s), PSO(s):

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO 1	√														
CO 2	√														
CO 3	√														
CO 4	√														
CO 5	√														
CO 6	√	√	√										√		
CO 7	√	√	√										√		
CO 8	√														
CO 9	√														
CO 10	√	√	√										√		
CO 11	√	√	√										√		

XI. JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING

Course Outcomes	POs / PSOs	Justification for mapping (Students will be able to)	No. of key competencies
CO 1	PO 1	Outline (Knowledge) the internal architecture of 8085, 8086, 8051 microcomputers and **Understand their functionality** and identify the differences between processors by applying **principles of mathematics and science.**	2
CO 2	PO 1	Illustrate (Understand) the organization of registers and memory in 8086 for programming (Apply) and memory allocation within processor for **solving (complex)**	3

		engineering problems by **applying engineering fundamentals, engineering specialization**.	
CO 3	**PO 1**	Explain (Understand) various addressing modes and instruction set of target microprocessor and microcontroller useful for writing assembly language programs by applying **mathematics, science** and **engineering fundamentals** .	3
CO 4	**PO 1**	Distinguish (Analyze) between minimum mode and maximum mode operation of 8086 microprocessor with timing diagrams by applying **engineering fundamentals and engineering specialization**.	2
CO 5	**PO 1**	Interpret (Understand) the functionality of various types of interrupts and their structure for controlling the processor or controller and program execution flow by applying **mathematics, engineering fundamentals and engineering specialization.**	3
CO 6	**PO 1**	Demonstrate (Understand) the internal architecture and various modes of operation of the devices used for interfacing memory and I/O devices with microprocessor by applying **mathematics, engineering fundamentals and engineering specialization**.	3
	PO 2	Interpret the internal architecture and Identify various modes of operation for **information and data collection** of the devices used by **reviewing research literature** for interfacing memory and I/O devices **for experimental design** to solve **complex engineering problems** with microprocessor **for the solution of development using principles of natural sciences and engineering sciences**.	5
	PO 3	Make use of the internal architecture (Understand) and various modes of operation of the devices **for identifying a problem** and make interfacing between memory and I/O devices with microprocessor **for experimental design** to **meet specific needs with environmental considerations, to manage the design process** and **evaluate outcomes.**	5
	PSO 1	Demonstrate (Understand) the internal architecture and various modes of operation of the devices used for interfacing memory and I/O devices with microprocessor for understanding how **design next generation computer systems.**	1
CO 7	**PO 1**	Choose (Apply) an appropriate data transfer scheme and hardware to perform serial data transfer among the devices by applying **mathematics, engineering fundamentals and engineering specialization**. .	3
	PO 2	**Identify** an appropriate data transfer scheme **(data) collection** and hardware for **model translation** and **analyze an experimental design** to perform serial data transfer among the devices **with an interpretation of results**.	5
	PO 3	Design proper data transfer scheme **to manage the design process** with **appropriate considerations** and hardware **design system components** for **designing the solutions on complex engineering problems** to perform serial data transfer among the devices **by applying the knowledge of techniques**, **for real time design issues.**	6

	PSO 1	Choose (Apply) an appropriate data transfer scheme and hardware to perform serial data transfer among the devices by using **networking devices**.	1
CO 8	**PO 1**	Outline (Understand) the salient features of 80286, 80386 and RISC processors in relation to basic 8086 microprocessor by applying **engineering fundamentals and engineering specialization.**	2
CO 9	**PO 1**	Illustrate (Understand) the paging operation and segmentation of advanced microprocessors for memory management by applying **knowledge of mathematics** and **engineering fundamentals**.	2
CO 10	**PO 1**	Interpret (Understand) the internal building blocks and registers of 8051 microcontroller used to perform serial data transfer, timer operation, interfacing of memory and I/O devices by applying **knowledge of mathematics**, **engineering fundamentals, engineering specialization.**	3
	PO 2	Explain the internal building blocks and **identify, with an system identification** registers of 8051 microcontroller **to collect the data, for an experimental design** by **analyzing complex engineering problems** used to perform serial data transfer, timer operation, interfacing of memory and I/O devices **to implement the design** for **sustained results**.	6
	PO 3	Extend the internal building blocks and registers of 8051 microcontroller **based on user needs and importance of considerations**, **for the innovative solutions**, **of the problem including all aspects to manage design process**, and perform serial data transfer, timer operation, interfacing of memory and I/O devices by **applying different techniques to achieve required sustainable development.**	6
	PSO 1	Make use of microcontroller to perform serial data transfer, timer operation, interfacing of memory and I/O devices and develop devices in **next generation computers**.	1
CO 11	**PO 1**	Build (Apply) necessary hardware and software interface using microcomputer based systems to provide solution for real world problems by applying **knowledge of mathematics**, **engineering fundamentals, engineering specialization.**	3
	PO 2	**Identify problem** and Choose necessary hardware and software interface **(information and data collection)** and conduct **experimental design** with **model translation** to provide **solution development** for real world problems **by interpreting results**	6
	PO 3	Organize necessary hardware and software interface **based on user needs and importance of considerations** for **innovative solutions, of the problem including all aspects to manage design process** , in microcomputer based systems **by applying different techniques**, **to achieve required sustained development, with legal requirements governing engineering activities, including personnel, health, safety, and risk issues.**	6

	PSO 1	Make use of **necessary** Microprocessors and Microcontrollers to provide **computer** based solutions for real world problems.	1

XII. NUMBER OF KEY COMPETENCIES FOR CO – (PO,PSO) MAPPING:

Course Outcomes	Program Outcomes/ Number of Vital Features												PSO / No. of Vital Features		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
	3	10	10	11	1	5	3	3	12	5	12	12	2	2	2
CO 1	2														
CO 2	3														
CO 3	3														
CO 4	2														
CO 5	3														
CO 6	3	5	5										1		
CO 7	3	5	6										1		
CO 8	2														
CO 9	3														
CO 10	3	6	6										1		
CO 11	3	6	6										1		

XIII. PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO,PSO) MAPPING:

Course Outcomes	Program Outcomes / Number of Vital Features												PSOs / No. of Vital Features		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
	3	10	10	11	1	5	3	3	12	5	12	12	2	1	2
CO 1	66.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 2	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 3	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 4	66.0	0.0	00.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	10.0	0.0
CO 5	100.0	00.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 6	100.0	50.0	50.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0	0.0	0.0
CO 7	100.0	50.0	60.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0	0.0	0.0

CO 8	66.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 9	100.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 10	100.0	60.0	60.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0	0.0	0.0
CO 11	100.0	60.0	60.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	50.0	0.0	0.0

XIV. COURSE ARTICULATION MATRIX (CO - PO / PSO MAPPING):

COs and POs and COs and PSOs on the scale of 0 to 3, **0** being **no correlation**, **1** being the **low correlation**, **2** being **medium correlation** and **3** being **high correlation**.

0 – **0** ≤ C ≤ 5%– No correlation;
1 – 5 < C ≤ 40%– Low / Slight;
2 – 40 % < C < 60% – Moderate.
3 – 60% ≤ C < 100%– Substantial / High

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO 1	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 2	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 3	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 4	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 5	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 6	3	2	2	-	-	-	-	-	-	-	-	-	2	-	-
CO 7	3	2	2	-	-	-	-	-	-	-	-	-	2	-	-
CO 8	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 9	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO 10	3	2	2	-	-	-	-	-	-	-	-	-	2	-	-
CO 11	3	2	2	-	-	-	-	-	-	-	-	-	2	-	-
TOTAL	33	8	8										8		
AVERAGE	**3.0**	**1.0**	**1.0**										**1.0**		

XV. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1,PSO 1	SEE Exams	PO 1,PSO 1	Assignments	PO 1,PO 2 PSO 1	Seminars	PO 1,PO 2, PO 3, PSO 1
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certificatior	-
Term Paper	-						

XVI. ASSESSMENT METHODOLOGIES – INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XVII. SYLLABUS

MODULE-I	INTRODUCTION TO 8 BIT AND 16 BIT MICROPROCESSOR
An over view of 8085, Architecture of 8086 Microprocessor, register organization of 8086, 8086 flag register. Addressing modes of 8086, Instruction set of 8086. Assembler directives, procedures, and macros. Assembly language programs involving logical, Branch & Call instructions, sorting, evaluation of arithmetic expressions, string manipulation.	
MODULE-II	**OPERATION OF 8086 AND INTERRUPTS**
Pin diagram of 8086-Minimum mode and maximum mode of operation with Timing diagrams. Interrupt structure of 8086: Vector interrupt table, Interrupt service routines. Introduction to DOS and BIOS interrupts.	
MODULE-III	**INTERFACING WITH 8086**
Memory interfacing to 8086 (Static RAM & EPROM). Need for DMA, DMA data transfer Method, Interfacing with 8237/8257. 8259 PIC Architecture and interfacing cascading of interrupt controller and its importance. Serial data transfer schemes: Asynchronous and Synchronous data transfer schemes. 8251 USART architecture and interfacing. TTL to RS 232C and RS232C to TTL conversion.	
MODULE-IV	**ADVANCED MICRO PROCESSORS**
Introduction to 80286, Salient Features of 80386, Real and Protected Mode Segmentation & Paging, Salient Features of Pentium, Branch Prediction, and Overview of RISC Processors.	
MODULE-V	**8051 MICROCONTROLLER ARCHITECTURE**
Microcontroller Architecture, Register set of 8051, Modes of timer operation, Serial port operation, Interrupt structure of 8051, Memory and I/O interfacing with 8051.	
TEXT BOOKS:	
1 A.K.Ray and K.M.Bhurchandi, ―Advanced Microprocessor and Peripherals‖, TMH, 2000. 2 Deshmukh, Micro Controllers‖, Tata McGraw Hill Edition, TMH, 2000	
REFERENCE BOOKS:	
1 Douglas U, ―Micro Processors & Interfacing‖, Hall, 2007. 2 By Liu, GA Gibson, ―Micro Computer System 8086/8088 Family Architecture, Programming and Design‖, PHI, 2nd Edition, 2007.	

XVIII. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	CO	Reference
1	An over view of 8085	CO 1	R1: 1.1
2	Architecture of 8086 Microprocessor	CO 1	T1: 1.2 R1:1.3

Lecture No.	Topics to be covered	CO	Reference
3	register organization of 8086	CO 2	T1: 1.1 R1:1.4
4	8086 flag register	CO 2	T1: 1.1 R1:1.4
5-6	Addressing modes of 8086	CO 3	T1: 2.2 R1:1.6
7-8	Instruction set of 8086	CO 3	T1: 2.3 R1:1.5
9	Assembler directives	CO 3	T1: 2.4 R1: 1.8
10	Procedures and macros	CO 3	T1: 4.10 R1:1.9
11	Assembly language programs involving logical, Branch & Call instructions	CO3	T1: 3.4 R1:2.5
12	Sorting and evaluation of arithmetic expressions	CO3	T1: 3.4 R1:2.5
13	string manipulation	CO3	T1: 3.4 R1:2.5
14	Pin diagram of 8086	CO4	T1: 1.3 R1:1.2
15	Minimum mode operation with Timing diagrams	CO4	T1: 1.8 R1:2.1
16	maximum mode of operation with Timing diagrams	CO4	T1: 1.9 R1:2.1
17	Interrupt structure of 8086	CO5	T1: 4.3 R1: 3.1
18	Vector interrupt table and Interrupt service routines,	CO5	T1: 4.3 R1:3.2
19	Introduction to DOS and BIOS interrupts	CO5	T1: 4.3 R1:3.2
20	Memory interfacing to 8086 (Static RAM & EPROM).	CO6	T1: 5.1 R1:4.3
21	Need for DMA, DMA data transfer Method	CO6	T1: 7.2 R1:4.1
22	Interfacing with 8237/8257	CO6	T1: 7.1,7.3 R1:4.2
23-24	8259 PIC Architecture and interfacing	CO6	T1: 6.2 R1:5.2
25	cascading of interrupt controller and its importance	CO6	T1: 6.2 R1: 5.2
26	Serial data transfer schemes: Asynchronous and Synchronous data transfer schemes	CO7	T1: 6.4 R1:6.1
27-28	8251 USART architecture and interfacing	CO7	T1: 6.4 R1:6.2
29	TTL to RS 232C and RS232C to TTL conversion	CO7	T1: 6.4 R1:6.8
30	Introduction to 80286, Salient Features of 80386	CO8	T1: 9.1,10.1 R1:8.2
31	Real and Protected Mode	CO8	T1: 9.4,9.5 R1:8.4
32	Segmentation	CO9	T1: 10.8 R1:8.5

Lecture No.	Topics to be covered	CO	Reference
33	Paging	CO9	T1: 10.9 R1: 8.6
34	Salient Features of Pentium	CO9	T1: 12.2 R1:9.2
35	Branch Prediction	CO9	T1: 11.4 R1:9.4
36	Overview of RISC Processors	CO9	T1:13.1 R1:9.8
37-38	8051 Microcontroller Architecture	CO10	T1: 17.2 R1:10.2
39-40	Register set of 8051	CO10	T1: 17.4 R1:10.3
41	Modes of timer operation	CO10	T1: 17.5 R1:10.5
42-43	Serial port operation	CO10	T1: 17.6 R1:10.6
44-45	Interrupt structure of 8051	CO10	T1: 17.7 R1:10.8
46-47	Memory and I/O interfacing with 8051	CO10	T1: 17.6 R1:10.9

Prepared by:
Ms. B Lakshmi Prasanna, Assistant Professor **HOD, ECE**