

# **INSTITUTE OF AERONAUTICAL ENGINEERING**

(Autonomous) Dundigal, Hyderabad -500 043

# **INFORMATION TECHNOLOGY**

#### **COURSE DESCRIPTOR**

Course Title	MICR	MICROPROCESSORS INTERFACING AND APPLICATIONS								
Course Code	AEC02	AEC023								
Programme	B.Tech	B.Tech								
Semester	VI	VI IT								
Course Type	Core	Core								
Regulation	IARE -	- R16								
			Theory		Practio	cal				
Course Structure	Lectu	ires	Tutorials	Credits	Laboratory	Credits				
	3		1	4	3	2				
Chief Coordinator	Mrs. G	Bha	vana, Assistant P	rofessor , ECE						
Course Faculty	Mrs. G	Mrs. G Bhavana, Assistant Professor, ECE								

#### I. COURSE OVERVIEW:

The course will make them learn the basic theory of microprocessor and their applications in detail. Subsequently the course covers important concepts like how to write an assembly language programming. They will learn to write an assembly language programming for interfacing various I/O modules. They will learn to design different advance architectures to design a new communication interfaces.

#### **II.** COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	ACS004	III	Computer Organization and Architecture	4
UG	AEC020	III	Digital Logic Design	4

#### **III. MARKS DISTRIBUTION:**

Subject	SEE Examination	CIA Examination	Total Marks	
Microprocessors Interfacing and Applications	70 Marks	30 Marks	100	

~	Chalk & Talk	~	Quiz	~	Assignments	×	MOOCs		
~	LCD / PPT	~	Seminars	×	Mini Project	×	Videos		
×	Open Ended Experiments								

#### IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

#### V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

**Semester End Examination (SEE):** The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

#### **Continuous Internal Assessment (CIA):**

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Component		Total Marks			
Type of Assessment	CIE Exam	Quiz / AAT	– Total Marks		
CIA Marks	25	05	30		

Table 1: Assessment pattern for CIA

#### **Continuous Internal Examination (CIE):**

Two CIE exams shall be conducted at the end of the 8<sup>th</sup> and 16<sup>th</sup> week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

#### Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

#### VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	<b>Engineering knowledge</b> : Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Quiz
PO 2	<b>Problem analysis</b> : Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignments
PO 4	<b>Conduct investigations of complex problems</b> : Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Seminars

**3** = High; **2** = Medium; **1** = Low

#### VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes (PSOs)	Strength	Proficiency assessed by
PSO 1	<b>Professional Skills:</b> The ability to research, understand and implement computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient analysis and design of computer-based systems of varying complexity.	2	Seminars and Assignments
PSO 2		2	Quiz and Assignments
PSO 3	<b>Successful Career and Entrepreneurship:</b> The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies	-	-

**3** = High; **2** = Medium; **1** = Low

#### VIII. COURSE OBJECTIVES (COs):

The co	The course should enable the students to:									
Ι	Understand the basic concepts of microprocessors and develop the architectures of 8085 and 8086.									
II	Analyze and develop assembly language programming for 8086 microprocessor.									
III	Develop various interfacing modules by using assembly language programming.									
IV	Understand and know the basic concepts of advance micro processor architectures like 80386 and 80486.									

#### IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC023.01	CLO 1	Understand the internal Architecture of 8086	PO 1	3
		microprocessor and explain various modes of		

		operation of 8086.		
AEC023.02	CLO 2	Differentiate between 8085 and 8086	PO 1	3
AEC023.03	CLO 2	microprocessors architectures and its functionalities. Distinguish between RISC and CISC architecture	PO 1	2
AEC025.05	CLO 3	c	POI	3
AEC023.04	CLO 4	based microprocessors.	PO 2	2
AEC025.04	CLO 4	Explain various addressing modes and instruction set present in 8086 microprocessor.	PO 2	2
AEC023.05	CLO 5	Ability to understand and apply the fundamentals of	PO 2	2
ALC025.05		assembly level programming of microprocessors.	102	2
AEC023.06	CLO 6	Analyze and develop low level languages like ALP	PO 2	2
ALC025.00	CLOU	in 8086 Microprocessor systems for real time	102	2
		applications.		
AEC023.07	CLO 7	Describe in detail about the concept of interrupt,	PO 2	2
112025.07	CLO /	types of interrupts and ISR present in 8086	102	2
		microprocessor.		
AEC023.08	CLO 8	Understand the concept of memory organization in	PO 1	3
		processors which helps in various system designing		-
		aspects.		
AEC023.09	CLO 9	Identify the importance and significance of serial	PO 1	3
		communication protocols in 8086 microprocessor.		
AEC023.10	CLO 10		PO 2	2
		and interrupt sub routines in 8086 microprocessor.		
AEC023.11	CLO 11	Discuss the interfacing diagram of I/O devices with	PO 4	1
		keyboard, 7-segment display, LCD and DAC to		
		ADC.		
AEC023.12	CLO 12	Develop and design the interfacing circuit diagram	PO 1	3
		of 8251 with 8086 processor.		
AEC023.13	CLO 13		PO 1	3
		asynchronous serial data transfer schemes in 8086.		
AEC023.14	CLO 14	Explain the advance architectures of PIC and also	PO 1	3
		the importance of interfacing a interrupt controller in		
		PIC.		
AEC023.15	CLO 15	Understand basic architecture of 16 bit and 32 bit	PO 2	2
		microprocessors with the help of multitasking and		
		addressing modes.		
AEC023.15	CLO 16	Analyze the various advanced microprocessors	PO 1	2
		internal architectures for 80X86 by paging and		
		technical features.		

3 = High; 2 = Medium; 1 = Low

#### X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning		Program Outcomes (POs)										Program Specific Outcomes (PSOs)			
Outcomes (CLOs)	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	2												2	2	
CLO 2	3												1		

CLO 3										3		
									 	 5		
CLO 4		2								1		
CLO 5		2										
CLO 6		3									3	
CLO 7		2									2	
CLO 8	3									2		
CLO 9	2										2	
CLO 10		2										
CLO 11				2								
CLO 12	3											
CLO 13	2									1		
CLO 14	3											
CLO 15		2								2	2	
CLO 16		2								1		
	3 = High; 2 = Medium; 1 = Low											

#### XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1	SEE Exams	PO 1	Assignments	PO 2	Seminars	PO 4
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 4						

#### XII. ASSESSMENT METHODOLOGIES - INDIRECT

~	Early Semester Feedback	>	End Semester OBE Feedback	
×	Assessment of Mini Projects by Experts			

## XIII. SYLLABUS

Unit-I	OVERVIEW OF 8086 MICROPROCESSOR				
	Introduction to 8085 microprocessor. RISC and CISC processors, architecture of 8086 microprocessor, special functions of general purpose register, 8086 flag register and function of 8086 flags, addressing				
	8086, instruction set of 8086, assembler directives.				
Unit-II	8086 ASSEMBLY LANGUAGE PROGRAMMING				
Assembly	Minimum mode and maximum mode of operation, timing diagram, Assembly language programs: Assembly language programs involving logical, branch and call instructions, sorting, evaluation of arithmetic expressions, string manipulation.				

Unit-III	8255 PROGRAMMABLE PERIPHERAL INTERFACE (PPI)				
Various modes of 8255 operation and interfacing to 8086; Interfacing keyboard, displays, 8279 Stepper motor and actuators, digital to analog and analog to digital converter interfacing. Interrupt structure of 8086: Interrupt structure of 8086, Vector interrupt table, interrupt service routines; Introduction to DOS and BIOS interrupts, 8259 PIC architecture and interfacing cascading of interrupt controller and its importance.					
Unit-IV	SERIAL DATA TRANSFER SCHEMES				
to RS 232	nous and synchronous data transfer schemes, 8251 USART architecture and interfacing; TTL 2C and RS232C to TTL conversion; Sample program of serial data transfer; Introduction to d serial communications standards, USB.				
Unit-V	ADVANCED MICROPROCESSORS:				
memory a	80286 Microprocessor: Architecture, registers (Real/Protected mode), privilege levels, descriptor cache, memory access in GDT and LDT, multitasking, addressing modes; Flag register 80386: Architecture, register organization, memory access in protected mode, paging; 80486: Only the technical features.				
Text Boo	ks:				
<ol> <li>A.K</li> <li>Educa</li> <li>Saval</li> </ol>	Hall, "Microprocessors and Interfacing", Tata McGraw-Hill Education, 3rd Edition 2013. Ray, K. M. Bhurchandani, "Advanced Microprocessors and Peripherals" Tata McGraw-Hill ation, 2nd Edition, 2006. iya M. T, "8086 Programming and Advance Processor Architecture", Wiley India Pvt., 1st on, 2012.				
Reference	e Books:				
	nthil Kumar, M. Saravanan, S. Jeevanathan, S. K. Shah, "Microprocessors and Interfacing", ed University, let Edition, 2012				

# Oxford University, 1st Edition, 2012. 2. Lyla B. Das, "The x86 Microprocessors", Pearson India, 2nd Edition, 2014.

## **XIV. COURSE PLAN:**

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Basic understanding of 8085 and 8086 microprocessors architectures and its functionalities.	CLO 1	T2:1.2
6-10	Able to understand the importance of addressing modes and the instruction set of the processor which is used for programming.	CLO 4	T2:2.2
11-15	Analyze the importance of the instruction set of the processor which is used for programming.	CLO 4	T2:2.3
16-20	Discuss about the assembly language programming and of 8086 microprocessor.	CLO 5	T2:3.2
21-25	Understand the internal Architecture and different modes of operation of popular 8086 microprocessors.	CLO 2	T2:5.5
26-28	Ability to understand and apply the fundamentals of assembly level programming of microprocessors.	CLO 6	T2:3.3
29-30	Explain sorting and evaluation concepts of 8086 microprocessor.	CLO 12	T2:2.2
31-35	Ability to interface the external peripherals and I/O devices and program the 8086 microprocessor using 8255.	CLO 14	T2:5.1
36-40	Understand the concepts of interrupt and interrupt sub routines in 8086 microprocessor.	CLO 10	T2:4.3
41-44	Identify the significance of serial communication in 8086. Develop the interfacing of 8251 with 8086 processor.	CLO 13	T2:6.1
45-52	Analyze and understand the Interfacing of RS-232C and high speed buses.	CLO 15	R2:5.1

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
53-58	Understand and analyze the various advanced microprocessors internal architectures such as 80X86.	CLO 16	R2:5.3

## XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. N0	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	ALP for Microprocessors like 8086 and 80x86	Seminars / NPTEL/Assig nments	PO 1, PO 2	PSO 1
2	Interfacing IO devices to various types of Microprocessors	Seminars / NPTEL	PO 2, PO 4	PSO 1
3	Programming of all microprocessors by using ALP	Guest Lectures	PO 1, PO 2	PSO 2

**Prepared by:** Mrs. G Bhavana, Assistant Professor.

HOD, IT