INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**PULSE AND DIGITAL CIRCUITS**				
Course Code	AEC006				
Programme	B.Tech				
Semester	IV	ECE			
Course Type	Foundation				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Mr. B Naresh, Assistant Professor				
Course Faculty	Ms. J Swetha, Assistant professor Ms. N Anusha, Assistant professor Mr. S Lakshmana Chary, Assistant professor Mr. B Naresh, Assistant professor				

I. COURSE OVERVIEW:

The course will make them learn the basic concepts of linear and non linear wave shaping circuits with their design and applications in detail. It provides the analysis and applications of different multivibrator circuits and they will be able to design multivibrator circuits. This course intended to describe the basic operating principle, sampling gates and time base generator circuits. They learn the applications of sweep circuits and multivibrators in synchronization methods, and analysis of logic families. It provides a platform for advanced courses like Linear Integrated Circuits and VLSI design. Greater Emphasis is placed on the use of multivibrators and logic families.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC001	III	Electronic Devices and Circuits	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Pulse and Digital Circuits	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):
Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	2	Lectures, Assignments
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignments
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Lab related Exercises
PO 12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	3	Seminars

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	1	Seminar
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	-	-
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Be proficient in the use of linear and non linear wave shaping circuits for sinusoidal, pulse and ramp inputs.
II	Construct various multivibrators using transistors, and design sweep circuits and sampling gates.
III	Evaluate the methods to achieve frequency synchronisation and division using uni-junction transistors, multivibrators and symmetric circuits.
IV	Realize logic gates using diodes and transistors and distinguish between various logic families.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC006.01	CLO 1	Understand the response of high pass RC and low pass RC circuits to different non sinusoidal inputs with different time constants and identify RC circuit's applications.	PO 1 PO 2	2
AEC006.02	CLO 2	Understand the various clipper circuits using switching components like diodes, transistors and design various clipper circuits with and without reference voltages.	PO 1 PO 2	2
AEC006.03	CLO 3	Formulate clamping circuit theorem and design practical clamping circuits by understanding the different diode clamper circuits.	PO 1	3
AEC006.04	CLO 4	Illustrate the Bistable multi with various triggering methods and apply design procedures to different bistable multivibrator circuits.	PO 5	2
AEC006.05	CLO 5	Evaluate triggering points, hysteresis width of Schmitt trigger circuit and also design practical Schmitt trigger circuit.	PO 2	2
AEC006.06	CLO 6	Analyze the Monostable, Astable multivibrator circuits with applications and evaluate time, frequency parameters.	PO 5	3
AEC006.07	CLO 7	Understand the different types of sampling gates with operating principles using diodes, transistors and also evaluate various parameters of sampling gates.	PO 1	3
AEC006.08	CLO 8	Implement different methods to generate time base waveforms using various sweep circuits like Bootstrap and Miller circuits.	PO 1	2
AEC006.09	CLO 9	Apply the various time base generator circuits in applications like cathode ray oscilloscope and television circuits.	PO 1	2
AEC006.10	CLO 10	Understand the concept of frequency division, synchronization and pulse synchronization of various Relaxation circuits.	PO 1	3
AEC006.11	CLO 11	Analyze the frequency division with sweep circuits and various relaxation circuits like Astable multi, Monostable multi circuits.	PO 1	1
AEC006.12	CLO 12	Implement the synchronization of different sweep circuits with symmetrical signals and sinusoidal signals.	PO 5	1
AEC006.13	CLO 13	Understand and analyze the different bipolar, unipolar logic families like DTL, RTL, DCTL, TTL, MOS and CMOS.	PO 1 PO 12	2
AEC006.14	CLO 14	Understand the specifications of logic families such as propagation delay, fan in, fan out, noise immunity and compare various logic families.	PO 1	3
AEC006.15	CLO 15	Understand and analyze the tri state logic and interfacing of transistor transistor logic and complementary metal oxide semi conductor logic families.	PO 1	3

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X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CLOs	POs												PSOs		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2											1		
CLO 2	2	3											1		
CLO 3	3												1		
CLO 4					2										
CLO 5		2											3		
CLO 6					3										
CLO 7	3														
CLO 8	2														
CLO 9	2												1		
CLO 10	3												1		
CLO 11	1														
CLO 12					1										
CLO 13	2											3			
CLO 14	3												1		
CLO 15	3														

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO 1, PO 2, PO 5, PO 12	SEE Exams	PO 1, PO 2, PO 5, PO 12	Assignments	PO 1, PO 2	Seminars	PO 12
Laboratory Practices	PO 5	Student Viva	-	Mini Project	-	Certification	-
Term Paper	-						

XII. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS:

Unit-I	WAVE SHAPING CIRCUITS
Linear wave shaping circuits: High pass RC and low pass RC circuits, response to impulse and pulse inputs with different time constants, high pass RC circuit as a differentiator, low pass RC circuit as an integrator, switching characteristics of diode; Non-linear wave shaping circuits: Clipping circuits, diode clippers, shunt clippers, series clippers, clipping at two independent levels; Clamping circuits: Clamping theorem.	
Unit-II	**MULTIVIBRATORS**
Multivibrators: Introduction, classification; Bistable multivibrator: Fixed bias, self bias, unsymmetrical triggering, symmetrical triggering; Schmitt trigger: Upper trigger point, lower trigger point, hysteresis, applications of Schmitt trigger; Monostable multivibrator: Collector coupled, triggering of monostable Multivibrator. Astable multivibrator: Collector coupled, voltage to frequency converter.	
Unit-III	**SAMPLING GATES AND TIME BASE GENERATORS**
Sampling gates: basic operating principle of sampling gate, uni and bi directional sampling gates. Time base generators: General features of a time base signal; Methods of generating a time base waveform: Exponential sweep circuits, sweep circuit using uni junction transistor, Miller sweep circuit and Bootstrap sweep circuit. Bootstrap sweep circuit.	
Unit-IV	**SYNCHRONIZATION AND FREQUENCY DIVISION**
Synchronization and frequency division: Pulse synchronization of relaxation devices, frequency division with sweep circuits, other astable relaxation circuits, synchronization of astable multivibrator, monostable relaxation circuits as dividers, stability of relaxation dividers; Synchronization of a sweep circuit with symmetrical signals: Sinusoidal synchronization signals and sine wave frequency division with a sweep circuit.	
Unit-V	**DIGITAL LOGIC FAMILIES**
Bipolar logic families: RTL, DTL, DCTL, HTL, TTL, ECL, MOS, and CMOS logic families, tristate logic; Interfacing of CMOS and TTL families.	
Text Books:	
1. Anand Kumar, "Pulse and Digital Circuits, PHI learning", 2nd Edition,2005. 2. David A.Bell,"Solid State Pulse Circuits",PHI learing,4th Edition. 3. David J.Comer,"Digital Logic State Machine Design",Oxford UniversityPress,3rd Edition,2008.	
Reference Books:	
1. Ronald J.Tocci,"Fundamentals of Pulse and Digital Circuits", PHI learning,3rd Edition,2008. 2. Millman J.Taub, "Pulse,Digital and Switching Waveforms",Tata McGrawHill,2nd Edition ,2007.	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	CLOs	Reference
1-7	Understand the response of high pass RC and low pass RC, circuits with step, pulse and square inputs.	CLO 1	T1-1.1 to 1.4
8	Understand the diode switching times.	CLO 2	T1-3.1 to 3.3
9-12	Understand the clipper circuits with reference levels using diode.	CLO 2	T1-2.1
13-16	Understand the diode clamper circuits and formulate clamping circuit theorem.	CLO 3	T1–2.2 R2-8.1
17-20	Discuss the Bistable multi with triggering methods.	CLO 4	T1-4.1 to 4.9
21-24	Evaluate triggering points, hysteresis width of Schmitt trigger circuit.	CLO 5	T1- 4.10

Lecture No	Topics to be covered	CLOs	Reference
25-28	Understand the Monostable multi circuits with applications.	CLO 6	T1-4.11 to 4.14
29-31	Understand the Astable multi circuits and evaluate time, frequency parameters.	CLO 6	T1-4.15 to 4.17
32-36	Discuss the different types of sampling gates using diodes, transistors.	CLO 7	T1-7.1 to 7.9 R2-17.1
37-41	Illustrate the different methods to generate time base waveforms using sweep circuits.	CLO 8	T1-5.1 to 5.7
42-43	Understand the bootstrap and miller sweep circuits and applications.	CLO 8 CLO 9	T1-5.8 to 5.11
44-46	Understand the concept of frequency division and synchronization.	CLO 10	T1-6.1 to 6.2 R2-19.1
47-49	Understand the frequency division with sweep circuits and various relaxation circuits.	CLO 11	T1-6.3 to 6.5
50-51	Illustrate the synchronization of different sweep circuits with symmetrical signals and sinusoidal signals	CLO 12	T1-6.6
52-55	Understand and analyze the different bipolar logic families.	CLO 13	T1-9.3 to 9.7
56-57	Explain the specifications of logic families, and compare various logic families.	CLO 14	T1-9.1
58-60	Understand and analyze the tri state logic and interfacing of logic families.	CLO 15	T1-9.3

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs	Relevance With PSOs
1	Design oscillators using multivirator.	Seminars	PO 1	PSO 1
2	Analyze how the frequency synchronization is applicable to real time applications.	Seminars / NPTEL	PO 2	PSO 1
3	Encourage students to solve real time applications and prepare towards competitive examinations.	NPTEL	PO 2	PSO 1

Prepared by:
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