## DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

Course Code         Category         Hours / Week         Credits         Maximum Marks           AEC507         PE-III         I         T         P         C         CIA         SEE         Total           AEC507         PE-III         3         -         -         3         30         70         100           Contact Classes: 45         Tutorial Classes: Nil         Practical Classes: Nil         Total Classes: 45           COURSE OBJECTIVES:         Students will try to learn:         I         The architectures of digital signal processors and design aspects of digital signal processing algorithms.         I         The memory and external input/output peripheral interface with programmable DSP processor.           III         The realization of digital filters and fast fourier transform algorithms of the signal spectrum on host DSP processor.         IV         The programming skills using code composer studio environment for TMS320C54XX processor.           IV         The programming skills using code composer studio environment for TMS320C54XX processor.         CO1         Explain the floating point and fixed-point arithmetic number representation systems for processors gi signal in digital signal processors.         CO3         Summarize the benefits of programmable digital signal processors using single instruction multiple data and very large instruction word architectures.           CO         2         Comparet the architectural features of general-purpose proc	VII Semester: ECE											
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control systems, communication, instrumentation and medicine.		-	•••	· ·			·		as such	u0		

UNIT -I	INTRODUCTION TO DIGITAL SIGNAL PROCESSING	Classes: 08						
Introduction: Digital signal-processing system, discrete Fourier Transform (DFT) and fast Fourier transform (FFT), differences between DSP and other micro processor architectures; Number formats: Fixed point, floating point and block floating point formats, IEEE-754 floating point, dynamic range and precision, relation between data word size and instruction word size; Sources of error in DSP implementations: A/D conversion errors, DSP computational errors, D/A conversion errors, Q-notation.								
UNIT – II	ARCHITECTURE OF PROGRAMMABLE DSPs	Classes: 10						
Multiplier and multiplier accumulator, modified bus structures and memory access in PDSPs, multiple access memory, multiport memory, SIMD, VLIW architectures, pipelining, special addressing modes in PDSPs, on-chip peripherals.								
UNIT – III	OVERVIEW OF TMS320C54XX PROCESSOR	Classes: 08						
Architecture of TMS320C54XX DSPs, addressing modes, memory space of TMS320C54XX processors. Program control, instruction set and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation.								
UNIT - IV	INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs	Classes: 10						
Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA).								
UNIT -V	IMPLEMENTATIONS OF BASIC DSP ALGORITHMS	Classes: 09						
The Q-notation, convolution, correlation, FIR filters, IIR filters, interpolation filters, decimation filters, an FFT algorithm for DFT filters computation of the signal spectrum.								
TEXT BOOKS:								
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