DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

VII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC507	PE-III	3	-	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: Nil	Practical Classes: Nil				Total Classes: 45		

COURSE OBJECTIVES:

Students will try to learn:

I The architectures of digital signal processors and design aspects of digital signal processing algorithms.

II The memory and external input/output peripheral interface with programmable DSP processor.

III The realization of digital filters and fast fourier transform algorithms of the signal spectrum on host DSP processor.

IV The programming skills using code composer studio environment for TMS320C54XX processor.

COURSE OUTCOMES:

After successful completion of the course, Students will be able to:

CO 1 **Explain** the floating point and fixed-point arithmetic number representation systems for processing signal in digital signal processor.

CO 2 **Compare** the architectural features of general-purpose processors and digital signal processors.

CO 3 **Summarize** the benefits of programmable digital signal processors using single instruction multiple data and very large instruction word architectures.

CO 4 **Demonstrate** serial and parallel communication devices interfacing programmable digital signal processors for data transmission and reception.

CO 5 **Explain** addressing modes of programmable digital signal processors for fast data transfer to / from registers and memory.

CO 6 **Illustrate** the concepts of programmable digital signal processors with control instructions, interrupts and pipeline operations.

CO 7 **Make use of** memory and input/output peripherals to interface the programmable DSP devices for increasing time response of a system.

CO 8 **Analyze** IIR and FIR Filters on programmable digital signal processors using Q15 Format.

CO 9 **Apply** the concepts of multi-rate digital signal processing for interpolation and decimation operations.

CO 10 **Compute** decimation-in time - FFT and decimation-in-frequency - FFT for reducing computational complexity of DFT.

CO 11 **Use** the instruction sets of TMS320C54XX processor for implementing assembly language programs.

CO 12 **Implement** the applications of digital signal processors in a wide spectrum of areas such as control systems, communication, instrumentation and medicine.

UNIT -I	INTRODUCTION TO DIGITAL SIGNAL PROCESSING	Classes: 08
Introduction: Digital signal-processing system, discrete Fourier Transform (DFT) and fast Fourier transform (FFT), differences between DSP and other micro processor architectures; Number formats: Fixed point, floating point and block floating point formats, IEEE-754 floating point, dynamic range and precision, relation between data word size and instruction word size; Sources of error in DSP implementations: A/D conversion errors, DSP computational errors, D/A conversion errors, Q-notation.		
UNIT – II	**ARCHITECTURE OF PROGRAMMABLE DSPs**	**Classes: 10**
Multiplier and multiplier accumulator, modified bus structures and memory access in PDSPs, multiple access memory, multiport memory, SIMD, VLIW architectures, pipelining, special addressing modes in PDSPs, on-chip peripherals.		
UNIT – III	**OVERVIEW OF TMS320C54XX PROCESSOR**	**Classes: 08**
Architecture of TMS320C54XX DSPs, addressing modes, memory space of TMS320C54XX processors. Program control, instruction set and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation.		
UNIT - IV	**INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs**	**Classes: 10**
Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA).		
UNIT -V	**IMPLEMENTATIONS OF BASIC DSP ALGORITHMS**	**Classes: 09**
The Q-notation, convolution, correlation, FIR filters, IIR filters, interpolation filters, decimation filters, an FFT algorithm for DFT filters computation of the signal spectrum.		

TEXT BOOKS:

1. Avatar Singh and S. Srinivasan, Digital Signal Processing Thomson Publications, 1st Edition, 2004.
2. Lapsley et al., DSP Processor Fundamentals, Architectures & Features‖, S. Chand & Co, 1st Edition, 2000.
3. B. Ventakaramani, M. Bhaskar, Digital Signal Processors Architecture Programming and Applications‖, Tata McGraw-Hill, 1st Edition, 2006.

REFERENCES:

1. Jonatham Stein, Digital Signal Processing‖, John Wiley, 1st Edition, 2000.
2. Sen M. Kuo&WoonSergGan, Digital Signal Processors Architectures, Implementation and Application‖, Pearson Practice Hall, 1st Edition, 2013.
3. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, A Practical Approach to Digital Signal Processing‖, New Age International, 1st Edition, 2006.
4. Ifeachor E. C., Jervis B. W, Digital Signal Processing: A practical approach‖, Pearson Education, PHI/, 2nd Edition, 2002.
5. Peter Pirsch, Architectures for Digital Signal Processing‖, John Weily, 1st Edition, 2007.