VLSI DESIGN

VI Semester: ECE								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
AEC017	**Core**	3	1	-	4	30	70	100
Contact Classes: 48	**Tutorial Classes: 10**	**Practical Classes: Nil**				**Total Classes: 60**		

COURSE OBJECTIVES:

Students will try to learn:	
I	The Principles of hierarchical VLSI design from the metal oxide semiconductor transistor up to the system level and impact of scaling trends on the device parameters and fabrication.
II	The Data path subsystems incorporating into a VLSI chip with contemporary techniques for achieving high-speed, low-power and low area overhead.
III	The Chip design through a practical approach using advanced modern tools such as vivado and cadence for front end & back end.

COURSE OUTCOMES (COs):

CO No	**Course Outcomes**	**Knowledge Level (Bloom's Taxonomy)**
CO 1	**Describe** the MOSFET fundamentals & latest trends in the technology in line with forecast made by Moore for computing the parameters with constant or combined scaling models.	Understand
CO 2	**Examine the conditions for optimum performance of inverters using the** volt-ampere and threshold voltage characteristics of MOSFETS	Analyze
CO 3	**Explain** the oxidation, diffusion, ion implantation & lithography processes for pmos, nmos, cmos and BiCMOS transistors fabrication.	Understand
CO 4	**Illustrate** complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays.	Understand
CO 5	**Build** the stick diagrams, layouts of MOS circuits using lambda, absolute and Euler physical design rules.	Apply
CO 6	**Summarize** the reliability issues in interconnects, latching and electro migration for formulating remedial measurements to increase lifetime.	Understand
CO 7	**Compare** static and dynamic CMOS logic circuits in terms of power consumption and speed of operation.	Analyze
CO 8	**Distinguish** the structure, implementation approaches for full custom and semicustom design on the basis of speed, cost, reconfiguration and time to market parameters.	Understand
CO 9	**Outline** the role of Programmable logic devices such as PLA, PAL, PROM, FPGA and CPLD for realization of complex boolean functions	Understand
CO 10	**Develop** data path subsystems such as shifters, adders, multipliers, ALUs, parity generators, counters and comparators using stick diagrams and layouts.	Apply

CO 11	**Summarize** working principle of memory units and its peripheral circuitry using different models.	Understand
CO 12	**Construct** simulation, synthesis and design verification of logic circuits **using the key elements of VLSI design flow.**	Create

Syllabus:

UNIT-I	**MOSFETS**	**Classes: 08**
\Fundamentals of MOSFETs; Weak & strong inversion conditions; Threshold voltage concept in MOSFETs; Current - voltage characteristics of a MOSFET; MOSFET parasitics; Trends & projections in VLSI design & technology; Scaling in MOS devices; Effects in scaling of MOS devices; BiCMOS technologies; CMOS nanotechnology.		
UNIT-II	**VLSI DESIGN STYLES**	**Classes: 09**
NMOS, PMOS and CMOS fabrication Flow; Noise Margin; Inverter Threshold Voltage; NMOS inverter design and characteristics; CMOS inverter design and properties; Delay and power dissipation; Parallel & series equivalent circuits; Pass transistor; Various pull ups; Bi-CMOS inverters		
UNIT-III	**VLSI PHYSICAL DESIGN**	**Classes: 09**
Stick Diagrams; Physical design rules: 2 µm and lambda CMOS design rules for wires, contacts and transistors; Layout design; Euler's rule for physical design. VLSI Interconnects; Reliability issues in CMOS VLSI; Latching; Electromigration.		
UNIT-IV	**LOGIC DESIGN AND IMPLEMENTATION STRATEGIES**	**Classes: 09**
Gate Level Design: Complex gates; Switch logic; Transmission gates; Static and dynamic CMOS design; Time delays; Driving large capacitive loads; Wiring capacitances; Fan-in and Fan-out; Choice of layers implementation strategies full custom and semi custom design; Standard cell design and cell libraries; Programmable logic devices; CPLDs; FPGA building block architectures; FPGA interconnect routing procedures; Speed and area tradeoff.		
UNIT-V	**SUB SYSTEM DESIGN**	**Classes: 10**
Data Path Sub Systems: Sub system design; Shifters; Adders; ALUs; Multipliers; Parity generators; Comparators; Zero/one detectors; Counters Array Subsystems: SRAM; DRAM; ROM; Serial access Memories; Static and dynamic latches and registers; Timing issues; Clock strategies; Low power memory Circuits; Synchronous and asynchronous circuit design.		
Text Books:		
1. A. Pucknell, Kamran Eshraghian, "BASIC VLSI Design," Third Edition, Prentice Hall of India, 2007. ISBN: 978-81-203-0986-9 2. R. Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation," Wiley-IEEE Press, USA, 2005. ISBN: 978-0-470-88132-3 3. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective," Second Edition, Phi Learning, 2009. ISBN: 9788120322578		
Reference Books:		
1. N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley, 1993. ISBN: 978-81-317-1942-8 2. M.J. Smith, "Application Specific Integrated Circuits", Addisson Wesley, First edition, 1997. ISBN-13: 978-0321602756 3. John P. Uyemura, "CMOS Logic Circuit Design," Springer, USA, 2007. ISBN: 0-7923-8452-0		